Hitachi

POWER MOS-FET

DATA BOOK 1-15A

HITACHI

POWER MOS FET DATA BOOK

- GENERAL INFORMATION
- DATA SHEETS
- APPLICATION NOTE
- CROSS REFERENCE

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INDEX

POWER MOS FET

1. Introduction 11
2. Structures and Features 11
3. Product Line Up and Application 15
3.1. Line Up & Typical Characteristics 15
3.2. Application of Power MOS FET 26
4. Precautions in Handling 28
4.1. Lead Arrangement 28
4.2. Avoiding Measurement of Breakdown Voltage VGSS 28
4.3. Observation of ID-VDS Characteristics 28
4.4. How to Prevent Usual Oscillation 28
4.5. Prevention for Drain-Case Power MOS FET 29
4.6. Beware of Voltage Spikes (Drain Source) 29
4.7. Pay Attention to Circuit Layout 34
4.8. Current Dispersion at Parallel Connection 34
5. Characteristics of Power MOS FET 38
5.1. Output Characteristics 38
5.2. Frequency Response Characteristics 38
5.3. Switching Characteristics 39
5.4. Input Dynamic Characteristics 43
5.5. Area of Safe Operation (ASO) 49
5.5.1. Forward Bias ASO 49
5.5.2. Reverse Bias ASO 50
5.6. Temperature Characteristics 51
5.7. Source-Drain Diode Characteristics 52
5.7.1. Precautions in Handling the Built-In Diode 55
5.8. Design of High Breakdown Voltage Operation 56
5.9. Analysis of Oscillation in Source Follower Circuits 59
6. Discontinued Power Mos Fet and Replacement 60
6.1. Maintenance Part 60
6.2. Discontinuation Plan 60
6.3. Discontinued Products 60
6.4. HPAK S Series Replacement by TO3, TO3P 61
7. Standard Outline Dimensions 62
8. Insulation Spacer and Washer 64
9. Nomenclature of Transistors 65
10. Technical Symbols and its Definitions 66

DATA SHEETS
S SERIES, D SERIES

– 2SJ48 73
– 2SJ49 73
– 2SJ50 73
– 2SJ55 76
– 2SJ56 76
– 2SJ56H 79
– 2SJ76 81
– 2SJ77 81
– 2SJ78 81
– 22J79 81
– 2SJ102 83
– 2SJ113 86
– 2SJ114 89
– 2SJ116 92
– 2SJ117 95
– 2SJ118 98
– 2SJ119 98
– 2SJ120L 101
– 2SJ120S 101
– SJ122 104
– 2SJ127 107
– 2SJ130L 111
– 2SJ130S 111
– 2SJ160 115
– 2SJ161 115
– 2SJ162 115
– 2SK133 118
– 2SK134 118
– 2SK135 118
– 2SK175 121
– 2SK176 121
– 2SK176H 124
– 2SK213 126
– 2SK214 126
– 2SK215 126
– 2SK216 126
– 2SK220H 128
– 2SK221H 128
– 2SK258H 130
– 2SK259H 132
– 2SK260H 132
– 2SK294 134
– 2SK295 134
– 2SK296 137
– 2SK298 140
– 2SK299 140
– 2SK308 143
– 2SK310 146

– 2SK311 146
– 2SK312 149
– 2SK313 149
– 2SK317 152
– 2SK318 154
– 2SK319 156
– 2SK320 156
– 2SK346 159
– 2SK349 162
– 2SK350 162
– 2SK351 165
– 2SK375L 168
– 2SK375S 168
– 2SK382 171
– 2SK383 174
– 2SK384L 177
– 2SK384S 177
– 2SK399 180
– 2SK400 183
– 2SK401 186
– 2SK408 189
– 2SK409 189
– 2SK410 192
– 2SK412 195
– 2SK413 198
– 2SK414 198
– 2SK415 201
– 2SK416L 204
– 2SK416S 204
– 2SK428 207
– 2SK429L 210
– 2SK429S 210
– 2SK430L 213
– 2SK430S 213
– 2SK440 216
– 2SK511 219
– 2SK512 222
– 2SK513 225
– 2SK534 228
– 2SK619 231
– 2SK646 240
– 2SK1056 250
– 2SK1057 250
– 2SK1058 250

DII SERIES

– 2SK549 253
– 2SK551 257
– 2SK552 261
– 2SK553 261

– 2SK554 265
– 2SK555 265
– 2SK556 269
– 2SK557 269
– 2SK559 273
– 2SK560 273
– 2SK579L 277
– 2SK579S 277
– 2SK580L 277
– 2SK580S 277
– 2SK600 281
– 2SK622 285
– 2SK623 289
– 2SK641 293
– 2SK642 293
– 2SK682 297
– 2SK683 297
– 2SK684 301
– 2SK685 305
– 2SK695 309
– 2SK696 313
– 2SK740 317
– 2SK741 321

DIII SERIES

– 2SK970 325
– 2SK971 329
– 2SK972 333
– 2SK973L 336
– 2SK973S 336
– 2SK974L 340
– 2SK974S 340
– 2SK975 344
– 2SK1093 347
– 2SK1094 351
– 2SK1095 355

POWER MOS FET MODULES

– PM45502C 359
– PM50502C 364
– PM45302F 369
– PM50302F 374
– PF0008 379

NEW PRODUCTS

DII SERIES

– 2SK1199 (HS76117) 383
– 2SK1200 (HS78137) 387
– 2SK1201 (78149) 391
– 2SK1202 (78139) 392
– 2SK1203 (HS78141) 393
– 2SK1204 (78143) 397

DIII-H SERIES

– 2SK1151 398
– 2SK1152 398
– 2SK1153 400
– 2SK1154 400
– 2SK1155 404
– 2SK1156 404
– 2SK1157 408
– 2SK1158 408
– 2SK1159 412
– 2SK1160 412
– 2SK1161 416
– 2SK1162 416
– 2SK1163 420
– 2SK1164 420
– 2SK1165 424
– 2SK1166 424
– 2SK1167 428
– 2SK1168 428
– 2SK1169 432
– 2SK1170 432

POWER MOS FET ARRAYS

– HF9913 (4AK15) 436
– HF9915 (4AK16) 438
– HF9917 440

POWER MOS FET MODULE

– PF0010 442
– PF0011 445

APPLICATION NOTE 449

POWER MOS FET CROSS REFERENCE LIST 509

THIS DATABOOK ALSO CONTAINS PRELIMINARY INFORMATIONS ON NEW PRODUCTS. SPECIFICATION AND INFORMATION CONTAINED HEREIN ARE SUBJECT TO CHANGE WITHOUT NOTICE

GENERAL INFORMATION

- INTRODUCTION
- STRUCTURE & FEATURES
- LINE UP & APPLICATIONS
- CPRECAUTIONS IN HANDLING
- HARACTERISTICS OF POWER MOSFET
- STANDARD OUTLINE DIMENSIONS
- INSULATION SPACER & WASHER
- NOMENCLATURE OF TRANSISTORS
- TECHNICAL SYMBOLS & DEFINITIONS

1. INTRODUCTION

In 1977, HITACHI was the first in the world to develop and mass-produce 100 Watt Complementary Power MOS FETs. Since then, Power MOS FETs have been used in a variety of fields as an ideal power device with high switching speed and high resistance to electrically induced failure. HITACHI Power MOS FET technology has consistently advanced in the areas of on-resistance, voltage and current handling capability and packaging.

At the beginning POWER-MOS-FET had the disadvantage related to RDS(on), but during the last years HITACHI improved the electrical characteristics by using advanced technologies. The result is todays very low RDS(on) characteristic similar to bipolar transistors.

POWER MOS FET FEATURES:

A. Excellent frequency response and high switching speed. (No carrier storage effects.)
B. High resistance to electrical destruction. (No current concentration effects.)
C. Easy parallel connection for higher power applications.
D. Minimum drive power. (Voltage controlled device.)

There are two basic Power MOS FET structures: Vertical Type and Lateral Type. The advantages of Vertical Types are: a) Drain Case and b) low on-resistance and low loss. Advantages of Lateral Types are: a) Source Case, b) high resistance to electrical destruciton, and c) high frequency response. HITACHI has both types to meet various requirements. The Vertical Types are called "D Series", and the Lateral Types are called "S Series".

Power MOS FETs show extreme advantages, not only in new fields where conventional power devices are inadequate, but also in existing fields where conventional devices are already in use.

Hitachi has now about 130 types with different characteristics including

- HIGH FREQUENCY
- HIGH BREAKDOWN VOLTAGE
- LOW POWER LOSS

POWER-MOS FET

2. STRUCTURE & FEATURES

Hitachi has two types of Power MOS FETs, D Series (vertical structure) and S Series (lateral structure), as shown in Fig. 2-1 and Fig. 2-2. Although there are some differences in their characteristics, both have the following advantages.

- Good frequency response and high switching speed due to absence of carrier storage effect.
- Free from current concentration, and hence have high resistance to destruction.
- Require a very low driving power as they are voltage controlled devices.

To understand the structure and features of Power MOS FETs, we would like to show the N-channel MOS FET.

Fig. 2-3 shows the N-channel MOS FET structure. This is called an MOS structure, because the current control gate region is made of three layers, Metal, Oxide and Silicon. The charged particles (electrons, here) are produced from Source and flow to and out of Drain.

When a positive voltage is applied to the gate electrode, in proportion to it, a depletion layer will be produced on the silicon surface beneath the gate. Then negative charges (electrons) will appear on it, which cause the silicon surface to be inverted from P type substrate to N type layer. This inverted layer is channel.

When a voltage is applied between Drain and

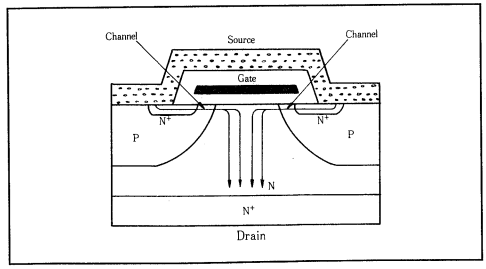


Fig. 2-1 Structure of D series (Vertical type) (N channel)

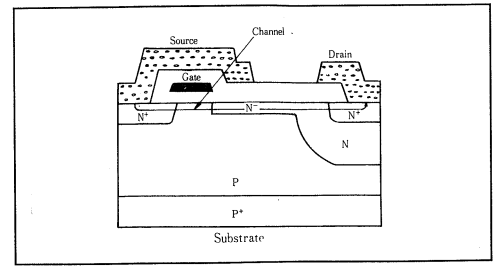


Fig. 2-2 Structure of S series (Lateral type) (N channel)

Source, electrons in the channel will move to the Drain, which means that the drain current flows.

There are two types of FETs, depletion type (normally ON type) and enhancement type (normally OFF type). In the case of depletion type FETs, drain current flows even if the gate voltage is 0V, in contrast to enhancement type FETs. Hitachi Power MOS FETs are all enhancement type (normally OFF type).

The gate voltage at which the drain current begins to flow is gate cut-off voltage V_{GS} (off). (Fig. 2-4).

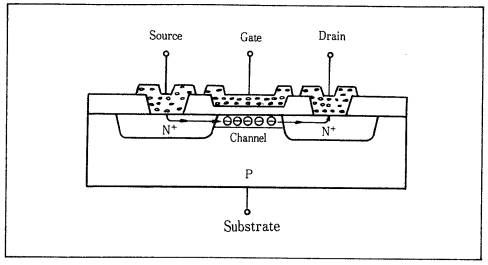


Fig. 2-3 Basic Structure of MOS FET (Lateral type)

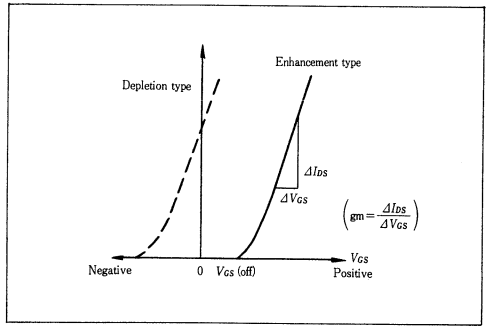


Fig. 2-4 Transfer Characteristics

Normally, there is a quadratic correlation between I_{DS} and V_{GS}. The slope of its curve gives the mutual conductance $g_m (=\frac{\Delta I_{DS}}{\Delta V_{GS}})$, that shows amplification factor.

Breakdown voltage of the drain varies with the structure between the N^+region of the drain and the gate electrode, as shown in Fig. 2-3. There is only a thin oxide film between the N^+ region and the gate electrode, so the field gradient will be high. This makes it difficult to achieve high drain to gate breakdown voltage, limited to 20 ~ 30V in typical MOS FETs.

By widening the space between the N^+ region of the drain and the gate electrode, and easing the electric field concentration, we can make the breakdown voltage larger.

There are two fabrication methods used to make the breakdown voltage higher, one is D series (vertical structure) and the other is S series (lateral structure). We would like to further explain about their structures and features, with Fig. 2-1 and Fig. 2-2.

● D Series (vertical structure)

In D series the drain (N^+) is placed beneath the silicon substrate. The gate electrode covers over the N region between P channels, to ease the electric field concentration beneath the gate. The electrons flow out of the source and reach to the N region through the P channels horizontally. On the surface of the N region, there is an accumulation layer of N^+ produced by the positive voltage applied to the gate electrode. Therefore, the electrons are attracted to the accumulation layer, to flow to the drain through the N region vertically.

Consequently, the D series is referred to as a vertical structure. In this structure, the case is connected to the drain.

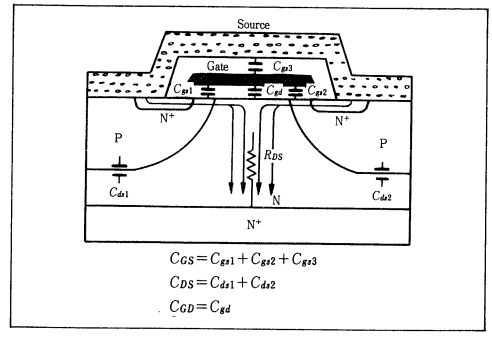


Fig. 2-5 Structure of D series (Vertical type) (N channel)

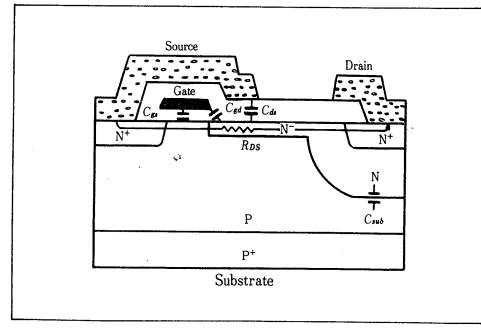


Fig. 2-6 Structure of S series (Lateral type) (N channel)

In the D series the channel (N region) is placed in the silicon, and the size of one unit can

be smaller than that of S series. This enables the switching ON resistance of D series to be smaller than that of S series with the same voltage and the same chip size.

Electrostatic capacitances are the junction capacitances and the MOS capacitances as shown in Fig. 2-5.

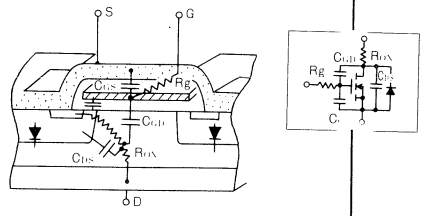
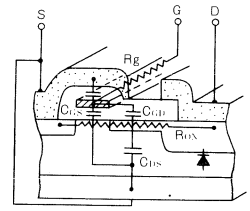
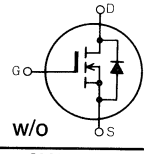
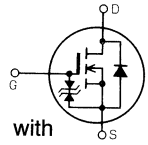
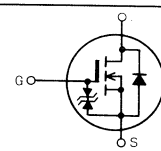
Here, the capacitance between the drain and the gate, C_{GD}, is relatively large, so in the source earth circuit, C_{GD}'s effects to the input capacitance (C_{iss}), to the output capacitance (C_{oss}) and to the feedback capacitance (C_{rss}) should be considered.

The gate electrode is made of polysilicon, which has long been used effectively in CMOS LSI. Polysilicon resistance is about 100 times larger than that of metals. When using it for the gate electrode, we lower the gate resistance by using a mesh gate pattern, and by connecting the polysilicon gate and the metal electrode effectively. To find the switching time of the vertical structure, more complicated operation analysis is required, because the feed back capacitance (C_{gd}) is large and the voltage dependence of the drain resistance is large. The input capacitance can't be determined simply by the time constant of the gate resistance. This will be further explained in the switching characteristics, paragraph 5.3.

● S Series (lateral structure)

In S series, the drain (N^+ region) is placed on the surface of the silicon. The region between the drain (N^+) and P channel is an N region

Table 2-1 Equivalent Circuits and Features, Parameters

STRUCTURE / ITEM		VERTICAL TYPE: D SERIES	VERTICAL TYPE: D II, D III Series	OFFSET GATE TYPE: S SERIES
EQUIVALENT CICUIT				
GATE PROTECTION		 w/o	 with	 with
FEATURE (RELATIVE COMPARISON)	Rg	SMALL (2.5Ω)	←	LARGE (22Ω) 2)
	Ciss 3)	LARGE (4100pF)	LARGE (4300pF)	SMALL (800pF)
	Crss	LARGE (50pF) 5)	LARGE (70pF) 5)	SMALL (15pF) 4)
	Ron	SMALL (0.60Ω)	SMALL (0.4Ω)	LARGE (2.2Ω)
	|Yfs|	LARGE (2.5S)	LARGE (8.0S)	SMALL (1.0S)
	fc	LOW (3MHz)	←	HIGH (7MHz) 6)
APPLICATION		HIGH SPEED POWER SWITCH		HIGH FREQU. POWER AMPLIFIER

Note 1) ( )The value in brackets is a relative comparsion at the same chip size between D, D II ab S-series. Condition is VDSS = 400V
2) However, it is able to be decreased by 2 digits with metal-gate.
3) Test conditions: VDS = 0, VGS = 10V, f = 1MHz
4) Slightly depens on Drain voltage
5) Heavily depens on Drain voltage
6) However, it is able to be increased by 1 digit with metal-gate.
7) General comment regarding protection circuit: The integrated gate-source diode is not a perfect ESD protection. Hitachi recommends to handle the Power-Mos-Fet under antistatic condition during shipment, testing and soldering and other production conditions.

produced by ion implantation, and it makes the strength of the electrostatic field even. Moreover, the source electrode is extended to cover a part of the N region, working as a field plate to prevent electrostatic field concentration around the gate. The electrons flow out of the source and reach to the drain through the P channel and the N region laterally. This is why the S series is called a lateral structure.

The substrate is connected to the source electrode, and the case to the source.

The feed back capacitance (C_{rss}) is indicated as C_{gd} in Fig. 2-6. The source field plate is extended above the N region, so the C_{gd} is shielded by the field plate and the capacitance of the N region (C_{ds}). This results in a very small value of feed back capacitance (C_{rss}).

From the view points of chip and package, the S series is very suitable for high frequency use, because the input and the output leads are separated electrically. Like in the D series, we usually use polysilicon for the gate electrode. Moreover, we can provide devices with metal gates for very high speed. In the polysilicon gate FET, the frequency limit is determined by the time constant of the input capacitance and the gate resistance. In the metal gate FET, it is determined by the lead inductances of the gate and the source, because the gate resistance is very small.

Table 2-1 shows the small signal equivalent circuit and the vertical characteristics of D, D II, D III series und S series.

3. LINE-UP AND APPLICATIONS

3.1. LINE UP & TYPICAL CHARACTERISTICS

This chapter shows the products sorted by main characteristics, using VDS(V) and ID(A) parameters. Refer to table 3-1 for D- and table 3-2 for S-family types. Detailed line-up is splitted into table 3-3 and table 3-4 for D- and S-family. Those are the first HITACHI POWER MOSFET products. Table 3-5 is for DII and 3-6 for DIII, the latest developed family.

● Table 3.1 D Series Line Up

ID(A) / VDS(V)	0.3	1[1.5]	2	3[4]	5	6	7	8	10[11]	12			15[20]	25[27]	30	40	50
40			□2SK416(0.5) □2SJ120(1.5)														
60		+[2SK975](0.3)	□2SK973(0.25)	□2SK974(0.15)	▲2SK346(0.3) ▲2SJ102(0.3)				▲2SK428(0.1) ▲2SJ122(0.15) ▲2SK549(0.1) ▲2SK970(0.12) ▼2SK1093(0.12)				▲2SK971(0.055) ▼2SK1094(0.055) ▲[HS76084]Pch* ▼[HS76086]Pch* ▲HS76080Pch ▼HS76082 Pch	▲2SK600(0.04) ▲2SK972 (0.03) ▼2SK1095(0.03) ▲[HS76099](0.02)* ▼[HS76101](0.02)		●HS78125(0.015)*	
80					▲2SK294(0.4)												
100				□2SK429(0.5) □HS72027(0.3)*	▲2SK295(0.4)				▲2SK383(0.15) ●2SK399(0.2) ●2SJ113(0.25)				▲[HS76121](0.07)* ▼[HS76123](0.07)*		●HS76147(0.05)*	●HS78145(0.025)*	
120									○2SK308(0.2) ▲2SK551(0.15) ▲2SJ127(0.2) ▼HS76127(0.15)*								
140								●2SK413(0.4) ●2SJ118(0.4)									
150				□2SK430(0.8)					▲2SK740(0.12)				●[2SK622](0.06)				
160								●2SK414(0.4) ●2SJ119(0.4)									
200						▲2SK440(0.4)		●2SK400(0.5) ●2SJ114(0.6)									
250	■2SK511(30)						▲2SK741(0.3)		○2SK401(0.3) ●2SK412(0.3)				●2SK1135(0.16) ●[2SK623](0.12)				
300		▲2SK296(2.5) □2SK375(2.5) □2SJ130(6.0)															
400			▲2SJ117(5.0)	▲2SK310(2.5)	▲2SK319(1.1)			○2SK298(1.1) ○2SJ116(1.8)	●2SK349(0.67)	○2SK312(0.67)							
450		□[2SK579](0.5) □[2SK1151(3.5)*		▲2SK311(2.5) ▼[HS76129](1.0)* ▲2SK1153(2.0)*	▲2SK320(1.1) ▲2SK552(1.0) ▲2SK1155(1.0)*		▲2SK554(0.6) ▲2SK1157(0.6)*	○2SK299(1.1) ▲2SK1159(0.55)*	●2SK350(0.67) ●2SK641(0.6) ●2SK1161(0.6)* ●[2SK1163](0.55)*	○2SK313(0.67) ●2SK556(0.40) ●2SK682(0.40) ●2SK1165(0.40)*			●2SK559(0.25) ○2SK1063(0.25) ●2SK1167(0.25)* ●[2SK1169](0.20)*		◇PM45302F(0.13)		◇PM45502C(0.06)
500	□2SK384(25)	□[2SK580](4.0)* □[2SK1152](4.0)*	▲2SK382(2.5)	▼[HS76129A](1.2)* ▲2SK1154(2.2)*	▲2SK553(1.2) ▲2SK1156(1.2)*		▲2SK555(0.7) ▲2SK1158(0.7)*	▲2SK1160(0.6)*	●2SK642(0.7) ●2SK1162(0.7)* ●[2SK1164](0.6)*	○2SK512(0.55) ●2SK557(0.45) ●2SK683(0.45) ●2SK1166(0.45)*			●2SK560(0.30) ○2SK1064(0.30) ●2SK1168(0.30)* ●[2SK1170](0.22)*		◇PM50302F(0.15)		◇PM50502C(0.09)
800				▲2SK513(5.0) ●2SK415(5.0)	○2SK351(1.7) ●2SK534(3.0) ●2SK695(2.0)		●2SK684(1.0)										
900			▲2SK1199(5.0)*	●2SK1200(5.5)* ▲[2SK1201](4.0)*	●2SK1202(3.0)*	●2SK1203(2.0)*		●2SK1204(1.2)*									
1000				●2SK696(3.0)	●2SK685(1.5) ●2SK1205(1.5)*												
1200				○[2SK646](3.0)													

Note 1) ( ): $R_{DS(on)}$ typ. (Ω)
——: DII SERIES
▭: DIII-F SERIES
(INCLUDES FAST RECOVERY DIODE)

----- : NEW DEVICE DIII SERIES
* : UNDER DEVELOPMENT
SPEC. MAY BE CHANGED

NOTE 2) □: DPACK
■: TO-126
▼: TO-220FM
●: TO-3P
○: TO 3
+: TO-92M
▲: TO-220AB
◇: MODULE

NOTE 3) DPACK. AVAILABILITY WITH LONG LEADS Ⓛ, Ⓢ
WITH SHORT LEADS FOR SMD TECHNOLOGY

Table 3-2 S Series Line Up

V_{DS}(V) \ I_D(A)	0.3	0.5	2	4	5	7	8
70	■2SK619(6)						
120						○2SK133(1.0) ○2SJ48(1.0) ●2SK1056(1.0) ●2SJ160(1.0)	
140		▲2SK213(8) ▲2SJ76(10)				○2SK134(1.0) ○2SJ49(1.0) ●2SK1057(1.0) ●2SJ161(1.0)	
160		▲2SK214(8) ▲2SJ77(10)				○2SK135(1.0) ○2SJ50(1.0) ●2SK1058(1.0) ●2SJ162(1.0)	○2SK220Ⓗ(1.0)
180		▲2SK215(8) ▲2SJ78(10)	▲2SK408(7) ▲2SK409(7)	▽2SK318(1.9)			○2SK175(1.0) ○2SJ55(1.0) ▽2SK317(0.95) ▽2SK410(1.2)
200		▲2SK216(8) ▲2SJ79(10)					○2SK176(1.0) ○2SJ56(1.0) ○2SK221Ⓗ(1.0)
250							○2SK258Ⓗ(0.8)
350					○2SK259Ⓗ(2.5)		
400					○2SK260Ⓗ(2.5)		

NOTE 1) ( ): $R_{DS(on)}$ typ.

NOTE 2) PACKAGES:
▲: TO-220AB ■ TO-126
○: TO-3 ● TO-3P
▽: RFPAK

Table 3-3 Typical Characteristics of Power MOS FET D Series

Package	Type Number		Absolute Max. Ratings				Electrical Characteristics (typ.)						
	N-ch	P-ch	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}* (W)	$R_{DS(on)}$ Ω typ.	$R_{DS(on)}$ Ω max.	$\|y_{fs}\|$ (S)**	t_{on} (ns)	t_{off} (ns)	C_{iss} (pF)	f_c (MHz)
DPAK	2SK416	2SJ120	40	±20	2	10	0.5/1.2	0.8/1.5	0.4/0.25	25/35	35/40	170/150	25
	2SK429	—	100		3	20	0.5	0.7	0.9	35	50	280	5
	2SK430	—	150				0.8	1.0				260	
	2SK375	—	300		1	10	2.5	4.0	0.4	20	70	140	10
	2SK384	—	500		0.3	10	25	50	0.1	20	20	70	40
TO-126	2SK511	—	250	±9	0.3	8	30	50	0.08	—	—	20	250
TO-220AB	2SK346	2SJ102	60	±20	5	30	0.3	0.4	0.9	40/60	70/100	350/660	7
	2SK428	2SJ122			10	50	0.1/0.15	0.15/0.2	2.2	60/80	120/200	900/1200	3
	2SK294	—	80		5	30	0.4	0.56	0.8	40	70	450	5
	2SK295	—	100										
	2SK383	—			10	50	0.15	0.18	2.8	60	150	1100	4
	2SK440	—	200		6	40	0.4	0.5	1.8	40	110	750	3
	2SK296	—	300		1	30	2.5	4.0	0.4	20	70	140	10
	2SK310	2SJ117	400		3/2	40	2.5/5.0	4/7	1.0/0.7	25/35	70/80	440/520	10
	2SK311	—	450		3		2.5	4.0	1.0	25	70	440	10
	2SK319	—	400		5	50	1.1	1.83	1.5	50	120	800	5
	2SK320	—	450										
	2SK382	—	500		2	30	2.5	4.0	0.7	25	70	440	10
	2SK513	—	800		3	60	5.0	6.0	0.7	50	120	470	5
TO-3P	2SK399	2SJ113	100	±20	10	100	0.2/0.25	0.25/0.35	2.0	50/70	110/160	800/1100	3
	2SK413	2SJ118	140		8		0.4	0.5	2.0/1.8	50/70	110/160	800/1050	3
	2SK414	2SJ119	160										
	2SK400	2SJ114	200				0.5/0.6	0.7/0.8	1.8	40/50	110/160	750/1000	3
	2SK412	—	250		10		0.3	0.4	2.5	65	180	1400	3
	2SK349	—	400		10		0.67	0.9	2.5	70	200	1500	3
	2SK350	—	450										
	2SK415	—	800		3	80	5.0	6.0	0.7	50	120	470	5
	2SK534	—			5	100	3.0	4.0	1.2	75	220	850	4
TO-3	2SK308	—	120	±20	10	100	0.2	0.3	2.8	60	160	1130	4
	2SK401	—	250				0.3	0.4	2.5	65	180	1400	3
	2SK298	2SJ116	400		8	100/125	1.1/1.75	1.75/2.25	1.7/1.6	50/60	120/220	800/1400	5/3
	2SK299	—	450			100	1.1	1.75	1.7	50	120	800	5
	2SK312	—	400		12	125	0.67	0.9	2.5	70	200	1500	3
	2SK313	—	450										
	2SK512	—	500				0.55	0.65	3.5	75	300	1800	–
	2SK351	—	800		5	125	1.7	3.0	2.0	100	300	1900	2
	2SK646	—	1200		4	125	3.0	4.0	1.3	80	350	2000	–

Note *: Value AT $T_c = 25°C$

**: Testcondition $V_{DS} \geqq I_D \times R_{DS(on)}$, $I_D = \frac{1}{2} I_{Dmax.(DC)}$

Table 3-4 Typical Characteristics of Power MOS FET S Series

Package	Type Number		Absolute Max. Ratings				Electrical Characteristics (typ.)						
	N-ch	P-ch	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}** (W)	$R_{DS(on)}$ Ω typ.	$R_{DS(on)}$ Ω max.	$\|y_{fs}\|$ (S)***	t_{on} (ns)	t_{off} (ns)	C_{iss} (pF)	fc (MHz)
TO-220AB	2SK213	2SJ76	140*	±15	0.5	30	8/10	—	0.15/0.1	20	30	90/120	40/30
	2SK214	2SJ77	160*										
	2SK215	2SJ78	180*										
	2SK408, 409	—	180*	±20	2.0	30	7	9	0.3	—	—	100	200
	2SK216	2SJ79	200*	±15	0.5	30	8/10	—	0.15/0.1	20	30	90/120	40/30
TO-126	2SK619	—	70	$^{+9}_{-6}$	0.3	10	—	50	0.13	—	—	10	—
TO-3	2SK133	2SJ48	120*	±14	7	100	1.0	1.7	1	180/230	60/110	600/900	3/2
	2SK134	2SJ49	140*										
	2SK135	2SJ50	160*										
	2SK175	2SJ55	180*	±20	8	125	1.0	1.7	1	250/230	90/120	800/1200	2/1
	2SK176	2SJ56	200*										
	2SK176Ⓗ	2SJ56Ⓗ	200							60	200		
	2SK220Ⓗ	—	160	±20	8	100	1.0	1.5	0.9	25	45	600	5Ω
	2SK221Ⓗ	—	200										
	2SK258Ⓗ	—	250		8	125	0.8	1.1	1.3	25	140	800	7
	2SK259Ⓗ	—	350		5	125	2.5	3.0	1.0	25	140	800	7
	2SK260Ⓗ	—	400										
TO-3P	2SK1056	2SJ160	120*	±15	7	100	1.0	1.7	1	180/230	60/110	600/900	3/2
	2SK1057	2SJ161	140*										
	2SK1058	2SJ162	160*										
RFPAK	2SK317	—	180	±20	8	120	0.95	1.25	1.25	—	—	600	300
	2SK318	—			4	70	1.9	2.5	0.6			300	
	2SK410	—			8	120	1.2	1.5	1.25	—	—	440	350

Note * : V_{DSX}
** : Value at T_C = 25° C
***: Test Conditions $V_{DS} > I_D \times R_{DS(on)}$, $I_D = I_{Dmax}$(DC)

● Power MOS FET DII Series

Characteristics of DII New Series

Hitachi achieved development of high-performance new Power MOS FET DII series by original technique. 15 types of DII series in the below table are going to be in production. DII series have the following features;

- high gain (g_m is 2 ~ 3 times higher than that of current D series.)
- low On Resistance (R_{on} is 30 ~ 50% lower than that of current D series.)

The maximum rated current can be driven by low input voltage: 7~8V do to high g_m. Driving power needs only 1/3 ~ 1/4 of that of current D series (at V_{GS}=10 ~ 15V) so that this series gives more energy saving in the circuit.

Table 3-5 Typical Characteristics of Power MOS FET DII Series

Package	Type Number		Absolute Max. Ratings				Electrical Characteristics (typ.)					
							$R_{DS(on)}$ Ω		$\|y_{fs}\|$	t_{on}	t_{off}	C_{iss}
	N-ch	P-ch	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}* (W)	typ.	max.	(S)**	(ns)	(ns)	(pF)
DPAK	—	2SJ130	300	±20	1	20	6.0	8.5	0.4	35	60	235
	2SK579	—	450	±15	1.5	20	3.5	5.5	1.0	28	48	260
	2SK580	—	500				4.0	6.0				
TO-220AB	2SK549	—	60	±15	10	50	0.1	0.15	5.0	55	100	700
	2SK600	—	60		25	75	0.04	0.055	15	130	195	2000
	2SK551	2SJ127	120		10	50	0.15/0.2	0.2/0.25	5/5	55/110	100/240	730/1450
	2SK740	—	150	±20	10	50	0.12	0.15	7.0	70	110	1200
	2SK741	—	250		7		0.4	0.55	4.5	50	120	820
	2SK552	—	450	±15	5	50	1.0	1.4	4.0	45	115	820
	2SK553	—	500				1.2	1.5				
	2SK554	—	450		7	60	0.6	0.85	6.5	65	155	1300
	2SK555	—	500				0.7	1.0				
	(2SK1199)	—	900	±20	2	50	5.0	7.0	1.0	70	115	490
TO-220FM	(HS76127)	—	120	±20	10	25	0.15	0.2	5.0	55	100	730
	(HS76129)	—	450		4	25	1.0	1.4	4.0	45	115	820
	(HS76129A)	—	500				1.2	1.5				
TO-3P	2SK622	—	150	±20	20	120	0.06	0.075	15	225	360	2200
	2SK1135	—	250		15	100	0.16	0.22	8.5	155	190	1600
	2SK623	—			20	120	0.12	0.15	12	225	360	2000
	2SK641	—	450	±15	10		0.6	0.8	7.0	65	155	1300
	2SK642	—	500				0.7	1.0				
	2SK556	—	450		12		0.40	0.55	10	110	230	2050
	2SK557	—	500				0.45	0.6				
	2SK682	—	450	±20	12	100	0.40	0.55	10	110	230	2050
	2SK683	—	500				0.45	0.6				
	2SK559	—	450	±15	15		0.25	0.36	13	145	320	2950
	2SK560	—	500				0.3	0.4				
	2SK695	—	800	±20	5		2.0	3.0	2.5	175	240	1150
	2SK684	—			7		1.0	1.5	4.0	250	440	1830
	(2SK1200)	—	900	±20	3	80	5.5	7.0	1.0	75	120	490
	(2SK1201)	—			4	100	4.0	5.5	1.7	105	155	620
	(2SK1202)	—			5		3.0	4.0	2.4	135	195	880
	(2SK1203)	—			6		2.0	3.0	2.5	150	230	1150
	(2SK1204)	—			8	120	1.2	1.6	4.0	230	430	1800
	2SK696	—	1000	±20	3	100	3.0	4.0	2.4	145	250	1170
	2SK685	—			5		1.5	2.0	3.5	265	450	1900
	(2SK1205)	—			6		1.5	2.0	3.5	250	440	1800
TO-3	2SK1063	—	450	±20	15	125	0.25	0.36	13	145	320	2950
	2SK1064	—	500				0.3	0.4				

Note ( ) : Under Development
* : Value at T_C = 25° C
** : Test Conditions $V_{DS} \geq I_D \times R_{DS(on)}$, $I_D = I_{Dmax(DC)}$
□ : High Speed trr diode version (t_{rr} = 100 ~ 150ns)

• POWER-MOSFET D III-L Series

Feature of low break down voltage D III-series is low $R_{DS(on)}$ resistance. This serie succeeds to reduce the $R_{DS(on)}$ about 1/2 compared to D II-series under the condition same chip size. Additional feature is provided by low voltage operation at 4V gate voltage.

So D III-types can be driven from 5 V TTL level (Logic IC, μP etc.), Logic level compatibility. Application is especially in low voltage power switches like DC/DC converters and in solenoid relays as well as in other actuator applications requesting low power loss.

Table 3-6 Typical Characteristics of Power-MOS FET D III-L Series

Package	Type No.	Absolute Max. Ratings				Electrical Characteristics							
	N-ch	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch} (W)	4V $R_{DS(on)}$ (Ω) typ.	4V $R_{DS(on)}$ (Ω) max.	10V $R_{DS(on)}$ (Ω) typ	10V $R_{DS(on)}$ (Ω) max.	$\|y_{fs}\|$ (S) typ.	t_{on}(ns) typ.	t_{off}(ns) typ.	C_{iss}(pF) typ.
TO-92M	2SK975	60	±20	1.5	0.9	0.4	0.55	0.3	0.4	1.5	15	80	140
DPAK	2SK973	60	±20	2	10*	0.4	0.5	0.25	0.35	2.0	19	120	240
	2SK974	60	±20	3	20*	0.2	0.25	0.15	0.18	4.0	30	255	400
TO-220AB	2SK970	60	±20	10	30*	0.17	0.22	0.12	0.15	6.0	60	220	240
	2SK971	60	±20	15	40*	0.075	0.095	0.055	0.65	12	80	300	860
	2SK972	60	±20	25	50*	0.05	0.06	0.033	0.04	20 0	145	450	1400
TO-220FM	2SK1093	60	±20	10	20*	0.17	0.22	0.12	0.15	6.0	60	220	400
	2SK1094	60	±20	15	25*	0.075	0.095	0.055	0.065	12	80	300	860
	2SK1095	60	±20	25	30*	0.05	0.06	0.033	0.04	20	145	450	1400

Note *: Value at $T_C = 25°C$

Testconditions: $R_{DS(on)}$ $V_{GS} = 4V, 10V$ $I_D = 1/2\ I_{Dmax}(DC)$

$|y_{fs}|$ $V_{DS} = 10V$ $I_D = 1/2\ I_{Dmax}(DC)$

D III-H Series (Preliminary Specification)

By using very advancaed MOS-IC technique Hitachi succeded in developing high voltage D III-series.
The key features are:

1. $R_{DS(on)}$ is 15% less than D II-Series
2. Ciss is reduced by 30% compared to D II-Series. This results in reduced driver loss during driving.
3. Switching time tf is 30 % shorter than D II-Series. This enables the user to design smaller systems because of reduced switching loss.
4. $V_{GSS} = \pm 30V$, $V_{GS(off)} = 2\text{-}3V$
   These very improved values allow to design a simple driving circuit and also high frequency parallel switching operation.

Table 3-7 Typical Characteristics of Power-MOS FET D III-H Series

Package	Type No.	Absolute Max. Ratings				Electrical Characteristics					
	N-ch	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}* (W)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	$\lvert y_{fs} \rvert$ (S)** typ.	t_{on}(ns) typ.	t_{off}(ns) typ.	C_{iss}(pF) typ.
DPAK	(2SK1151)	450	±30	1.5	20	3.5	5.5	1.0	20	35	160
	(2SK1152)	500				4.0	6.0				
TO-220AB	(2SK1153)	450	±30	3	30	2.0	2.8	2.5	27	50	330
	(2SK1154)	500				2.2	3.0				
	(2SK1155)	450		5	50	1.0	1.4	4.0	35	80	640
	(2SK1156)	500				1.2	1.5				
	(2SK1157)	450		7	60	0.6	0.8	6.5	70	135	1050
	(2SK1158)	500				0.7	0.9				
	(2SK1159)	450		8		0.55	0.7	7.5	80	185	1300
	(2SK1160)	500				0.6	0.8				
TO-3P	(2SK1161)	450	±30	10	100	0.6	0.8	7.0	75	135	1050
	(2SK1162)	500				0.7	0.9				
	(2SK1163)	450		11		0.55	0.7	8.0	85	190	1300
	(2SK1164)	500				0.6	0.8				
	(2SK1165)	450		12		0.4	0.55	10	90	180	1450
	(2SK1166)	500				0.45	0.60				
	(2SK1167)	450		15		0.25	0.36	13	140	220	2050
	(2SK1168)	500				0.3	0.4				
	(2SK1169)	450		20	120	0.2	0.25	16	185	320	2900
	(2SK1170)	500				0.22	0.27				

Notes ( ) : Under development, datas can be changed
*: Value at $T_C = 25°C$
**: Testconditions: $V_{DS} \geq I_D \times R_{DS(on)}$, $I_D = 1/2\ I_{Dmax}(DC)$

● Power MOS FET Module

Nowadays, high power transistors tend to be in module package especially in the field of motor control. On the other hand, power MOS FETs, because of their superior response, has begun to be applied to robots and manufacturing machines to improve their performance. In order to meet these requirements Hitachi has developed power MOS FET module. Table 3-8, 9, 10 shows their typical characteristics.

TABLE 3-8 Typical Characteristics of Power MOS FET Modules

Package	Number	Absolute Maximum Ratings				Electric Characteristics					
		V_{DSS} (V)	V_{GSS} (V)	I_D* (A)	Pch** (W)	R_{ds}(on) (Ω) typ	R_{ds}(on) (Ω) max	$\|y_{fs}\|$ (S)	t_{on} (ns)	t_{off} (ns)	t_{rr} (ns)
F	PM45203F	450	±20	30	200	0.13	0.2	25	580	900	200
	PM50302F	500				0.15	0.2				
C	PM45502C	450	±20	50	300	0.08	0.12	40	850	1400	200
	PM50502C	500				0.09	0.12				

Note 1) ▭ : D II-F_i Includes Fast Recovery Diode
* Per one transistor
** Value at T_c=25°C
2) Internal equivalent circuit:

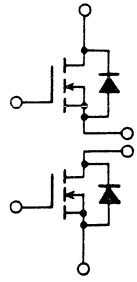


TABLE 3-9 Typical Characteristics of Power MOS FET High Frequency Modules

		Absolute Max. Ratings			Electrical Characteristics (typ.)				
Package	Type Number	V_{dd} (V)	V_{APC} (V)	Pin (mW)	I_D (A)	P_{out} (W)	η_T (%)	f (MHz)	
PFPAK	PF008	17	±8	30	3.0	9	40	865~890	V_{DD} = 13.8V Pin = 10mW
	PF0010	17	8	20	3.0	6*	40	820~850	V_{DD} = 12.5V Pin = 2mW
	PF0011 (HS7938)	17	8	20	3.0	6*	40	890~915	V_{DD} = 12.5V Pin = 2mW

Note * Pout at APC control

Another module of a fully molded package, the 10 pin SIL (**S**ingle **I**n **L**ine), used to house four logic level D III dice in one package for the ultimate high density packing.

TABLE 3-10 D III-L Series SIL x 4 Arrays

Development Number	ABSOLUTE MAX				ELECTRICAL PARAMETERS				
	VDSS (V)	VGSS (V)	ID (A)	PD (W)	10V RDS (on) (Ω)		VGS (off) (V)		t_{rr} (ns)
					TYP	MAX	MIN	MAX	TYP
HF9913 (4AK15)	60	±20	7	28	0.055	0.055	1	2	125
HF9915 (4AK16)	60	±20	5	28	0.12	0.15	1	2	70
HF9917	60	±20	2.5	28	0.25	0.35	1	2	70

INTERNAL EQUIVALENT CIRCUIT

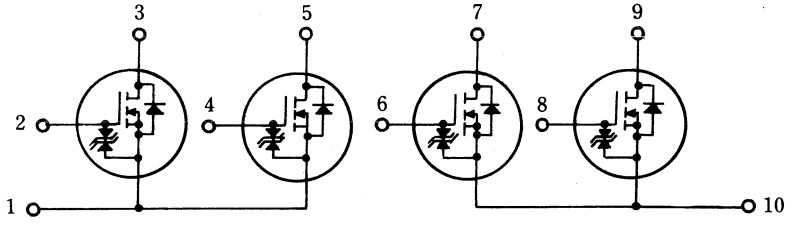
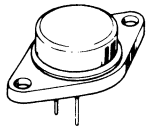
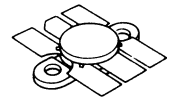
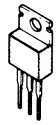
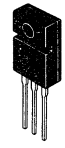
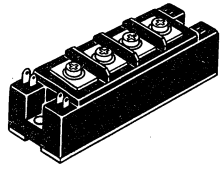
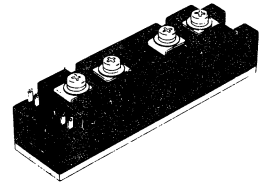


Table 3 – 11 Package Variatons

POWER MOS FET

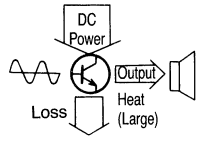
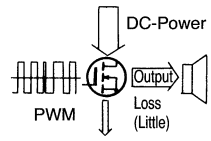
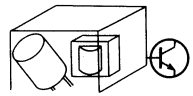
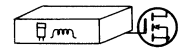
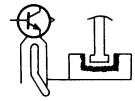
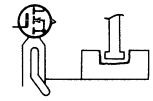
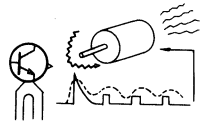
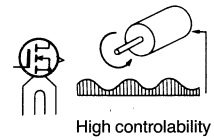
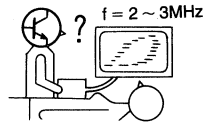
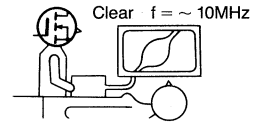
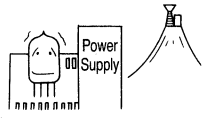
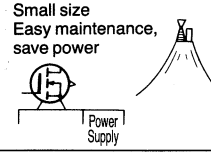
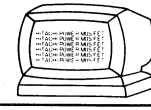
Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)
TO-3	120~800	5~ 30	0.2~3.0	TO-126	250	0.3	30
							
TO-3P	100~800	3 ~ 20	0.06~5.0	RFPAK	180	4 , 8	0.95~1.9
							
TO-220	40~800	1~25	0.03~5	TO-220FM	60~500	4~25	0 .03~1.2
							
DPAK	40~500	0.3~3.0	0.15~25	TO-92M	60	1.5	0.3
							

POWER MOS FET MODULES

Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)
F	450~500	30	0.13~0.15	C	450~500	50	0.08~0.09
							

3.2 Application of Power MOS FET

Table 3-11 shows the applications and recomend types of each power MOS FET.

Applications	Features		Function	
	Bipolar Transistor	Power MOS FET		
Audio output			Linear power amplifier	
			PWM-amplifier	
High speed power switching	f = 20 ~ 50kHz 	f = 100 ~ 500kHz (small size light wight) 	switch-ing power supply	AC 100V
				AC 200V
			DC/DC con-verter	Input DC 9~24V
				Input 48V
	f = 1 ~ 20kHz 	f = 200 ~ 500kHz 	Arcing machine Laser processing welding	
Motor control	f = 1 ~ 2kHz 	f = 20 ~ 30kHz  High controlability	Robot (Servomotor)	
			OA equipment (stepper motor printer head motor)	
			Inverter	
Ultrasonic-application			Ultrosonic diagnostic system Fish-finder	
Telecomuni-cation equipment			Medium and short waves	
			FM · VHF Band	
			Portable Telephon	
Others (Tubes & Display)	Videoband 10 ~ 20MHz 	Videoband 40 ~ 80MHz  high Reso-lution	Tube, Display	
			Coildrive	
			Relay, analog switch Lamp driver	

1) ( ): Under dev. 2) Underlined appl. are pictured examples 3) (FM) TO-220 fully molded package

Type Number							
TO-92M	DPAK	TO-126	TO-220AB[3]	TO-3P	TO-3	RFPAK	Module
			2SK214 2SJ77 2SK216 2SJ79	2SK1057 2SJ161 2SK400 2SJ114	2SK134 2SJ49 2SK175 2SJ55		
			2SK428 2SJ122 2SK551 2SJ127 2SK1094(FM) (HS76086)(FM)	2SK399 2SJ113 2SK413 2SJ118 2SK400 2SJ114			
	2SK579 2SK580 (2SK1151) (2SK1152)		2SK552 2SK554 (2SK1153) (2SK1159)	2SK556 2SK559 (2SK1165) (2SK1169)	2SK299 2SK313 2SK1063 2SK1064		
			2SK513 (2SK1199)	2SK684 2SK685 2SK695 (2SK1200)			
2SK975	2SK973 2SK974 2SK430 (HS72027)		2SK740 2SK551 2SK971 2SK972	2SK622 (HS78147) (HS78145)			
			2SK440 2SK741	2SK412 2SK623 2SK1135	2SK401		
				2SK557 2SK560 2SK682 2SK683 (2SK1168) (2SK1170)	2SK351 2SK1063 2SK1064		PM45302F PM45502C
			2SK383	2SK414 2SJ119 2SK412 2SK622 2SK623	2SK308 2SK401		
2SK975	2SK973 2SK974		2SK551 2SJ127 2SK1093(FM) (HS78082)(FM) 2SK1094(FM) (HS78086)(FM) 2SK1095(FM)	2SK413 2SK118 2SK400 2SJ114 (HS78145) (HS78147)			
				2SK682 2SK683 2SK685			PM45302F PM50302F PM45502C PM50502C
	2SK375 2SK579 2SK580 2SJ130 (2SK1151) (2SK1152)		2SK310 2SK311 2SK382 2SJ117 (2SK1153) (2SK1154)				
			2SK408 2SK409		2SK176 2SK221(H) 2SK258(H) 2SK260(H)	2SK410	
						2SK317 2SK318 2SK410	
							PF0008 PF0010
		2SK511 2SK619		2SK685	2SK646		
	2SK416 2SJ120						
	2SK384 2SK580		2SK972 2SK1095(FM)				

4. PRECAUTIONS IN HANDLING

Precautions in handling and quick check methods of Power MOS FET are described here.

4.1 Lead Arrangement

As shown in Table 4-1, the pin arrangement is different between D-series and S-series.

Table 4-1 Lead Arrangement

Package		Lead Arrangement					
		D Series			S Series		
		1	2	3	1	2	3
DPAK		Gate	Drain (Flange)	Source	—	—	—
TO-126		Source	Drain (Flange)	Gate	—	—	—
TO-220AB		Gate	Drain (Flange)	Source	Gate	Source (Flange)	Drain
TO-220FM		Gate	Drain	Source	—	—	—
TO-3P		Gate	Drain (Flange)	Source	Gate	Source (Flange)	Drain
TO-3		Gate	Source	Drain (Case)	Gate	Drain	Source (Case)
RF PAK		—	—	—	Source	Drain	Gate

4.2 Avoiding Measurement of Breakdown Voltage V_{GSS}

Avoid measuring V_{GSS} (gate to source breakdown voltage). At breakdown, negative resistance characteristics are generated, leading to oscillation and destruction.

4.3 Observation of I_D-V_{DS} Characteristics

When the I_D-V_{DS} characteristics (source common output characteristics) are observed, oscillation may be caused depending on the type of curve tracer used (input capacity and resistance differs). This can lead to destruction of the device. Oscillation can be prevented effectively by connecting an external series resistance of about 10kΩ to the gate.

When drawing an I_D-V_{DS} curve on an X-Y recorder, also, oscillation can be prevented by connecting the external series resistance of about 10kΩ to the gate or by inserting a capacitor of about 0.5μF between the gate and the source.

4.4 How to Prevent Usual Oscillation

In performing circuits experimentally, it is recommended to connect a resistance of 100Ω~2kΩ to the gate in series, to prevent unusual oscillation, until you get used to handling.

In using the device as a source follower, it is recommended to insert a 100μF capacitor between the drain and the ground, to prevent unusual oscillation.

4.5 Preventions When Handling Drain Case Power MOS FETs

Hitachi Power MOS FET D-series is not Gate-Protected. When Handling Power MOS FETs, to escape from damage or destruction by static charge, it is good practice to adopt the following procedures whenever possible.

(1) When handling power MOS FETs, the man should be grounded. And Power MOS FETs should be handled by the package, not by the leads. An example of grounding ring is shown in Fig. 4-1.

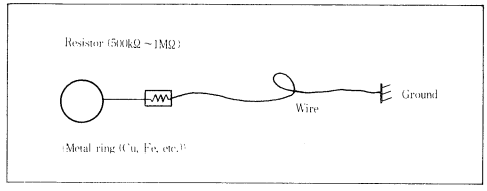


Fig. 4-1 To prevent from electric shock, insert resistor close to ring

(2) When handling or installing Power MOS FETs into circuits, should use metal plates that it grounded on Work Stations.

(3) When testing Power MOS FETs, Test Circuit (Curve tracer, etc.) should be grounded.

(4) When using soldering irons, soldering irons should be grounded. (It's better to use battery operated soldering irons.)

(5) When shipping in circuit boards, they should be placed in antistatic bags, unless the gate and the source are connected by resistors or inductors.

(6) Power MOS FETs should be placed not in plastic cases or bags, but in antistatic bags, conductive foam, or aluminum foil.

4.6 Beware of (Drain-Source) Voltage Spikes Induced by High Speed Switching

When power MOS FET is used for switching, negative switching device may change to be inductive load.

In this case, transient voltage spike will be produced by the inductance in the circuit when the device is switched off, since Power MOS FET is very fast.

Precaution of drain-source voltage spikes is described here.

Fig. 4-2 (a) shows switching operation about inductive load without clamp diode.

In this case, there is the fear of permanent device distortion if transient voltage determined by Ldi/dt increase more than its dielectric resistance.

Fig. 4-2 (b) shows the circuit with clamp diode.

In practical circuit, inductance by circuit layout is always present even though load is clamped. This inductance exists in the circuit layout between the anode of clamping diode and the drain of Power MOS FET and the layout up to power supply.

If the switching operation is applied at high speed and high level of current, there is danger of device distortion by applied voltage spike more than its dielectric resistance, even though you intend to clamp the voltage spike tightly.

Since the more the current flows, the more voltage spike increases, the confirmation of voltage waveform by high-speeded oscilloscope is required in the worst condition of supply voltage and negative current practically.

The improving methods about voltage spike is specified to the next item.

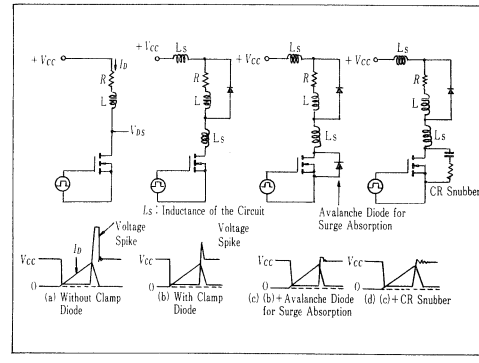


Fig. 4-2 Inductive Load Switching Circuit

(1) Circuit layout is made as short as possible, in order to control the rate of residual inductance to a minimum.
(Current loop area is reduced to a minimum using twisted pair wire as the lead of power supply.)

(2) Voltage spike is absorbed by connection of avalanche diode for surge absorption at the bottom the drain-source terminal. (Fig. 4-2 (c)).

(3) CR snubber is connected between source and drain as to limit the peak voltage. (Fig. 4-2 (d)).

(4) Voltage spike is also controlled by the gate-drive condition. The relation between gate-drive condition and voltage spike is shown in Fig. 4-3 and Fig. 4-4.

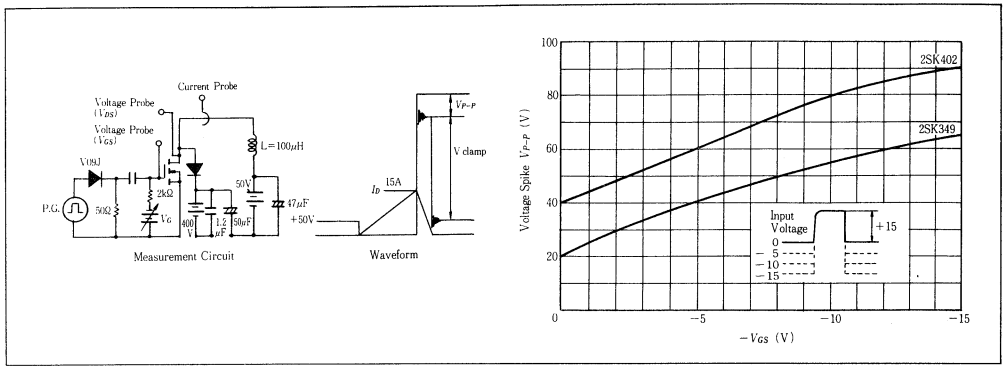


Fig. 4-3 Gate Bias Condition vs. Voltage Spike

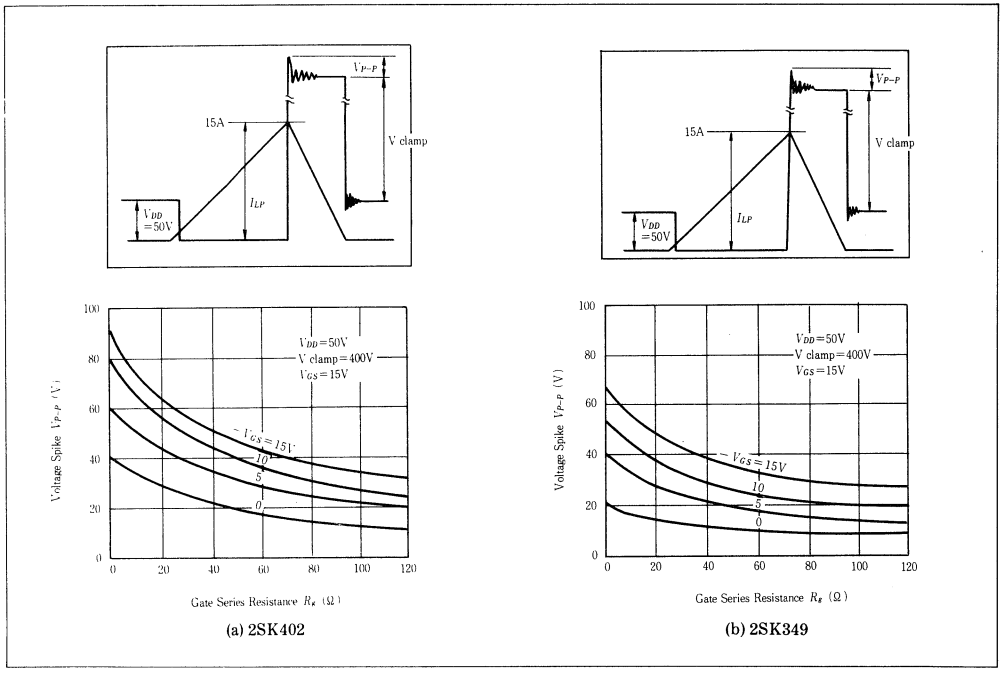


Fig. 4-4 Gate Series Resistance vs. Voltage Spike

Another application which is also required the caution in voltage spike is for motor control circuit.

Fig. 4-5 shows the basic motor control circuit and Fig. 4-6, its waveform at operation.

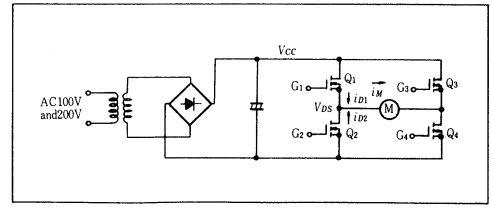
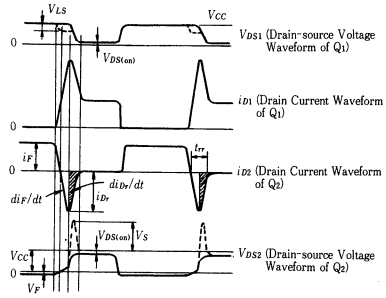


Fig. 4-5 Typical Motor Control Circuit



<Description>

i_F: Forward Current of Q_2 Built-in Diode

V_F: Forward Voltage Drop of Q_2 Built-in Diode

$V_{DS\,(on)}$: Drain-Source Saturation Voltage of Q_2

t_{rr}: Reverse Recovery Time of Q_2 Built-in Diode

V_{LS}: Voltage Drop with Current Inductance L_S

i_{Dr}: Reverse Recovery Current of Q_2 Built-in Diode (Depends on the Drive Signal Source Impedance d_{iF}/dt of Q_1, Circuit Inductance L_S, Supply Voltage V_{CC}, and Electric Charge Q_{rr} (or t_{rr}) in the Built-in Diode)

V_S: Spike voltage (Depends on the Inductance L_S, i_{Dr}, and di_{Dr}/dt of the Circuit)

Fig. 4-6 Waveform for the Motor Control Operation

Fig. 4-6 shows the waveform that Q_4 is keep on switch-ON during Q_1 chopping, controlling Q_2 and Q_3 switch-OFF, Q_1 and Q_4 switch-ON in the circuit, Fig. 4-5.

Voltage spike producing process is explained by this waveform, gate drive signal is put into G_1, then Q_1 is switched on and i_{D1} flows. When Q_1 current, i_{D1} is switched off, forward current, i_F flows through the built-in diode of Q_2 by the energy accumulated at the motor inductance. If Q_1 is switched on in this condition, Q_2 is into on-state under the influence of reverse recovery time, t_{rr} of built-in diode on Q_2, and high level of reverse current (recovery current), i_{Dr} flows.

Next, during i_{Dr} recoverying time (oblique lined part in Fig.) Voltage spike, which is determined by L_S di_{Dr}/dt, will be produced by the stray inductance presence in the circuit.

This voltage spike should be limited as low as possible.

The countermove, mentioned before, is as follows.

(1) Residual inductance should be limited to the lowest level, bewaring the circuit layout fully. (Twisted pair wire will be used as lead of power supply line in order to make current loop area small. It is to be desired that the layout of Q_1 source and Q_2 drain should be connected directly not to exist the inductance, and so is Q_3 source and Q_4 drain. The same kind of care is required at parallel connection.)
If it is hard to protect lead inductance from remaining at power supply line, one of the countermove is that a capacitor (C=0.1~1.0μF) is connected at the bottom of Q_3 drain and Q_4 source terminals like Q_1 drain and Q_2 source terminals.
Photo from A to E in Fig. 4-7 shows the waveform in various layout condition for reference.

(2) Voltage peak is limited, connecting CR snubber between drain and source.

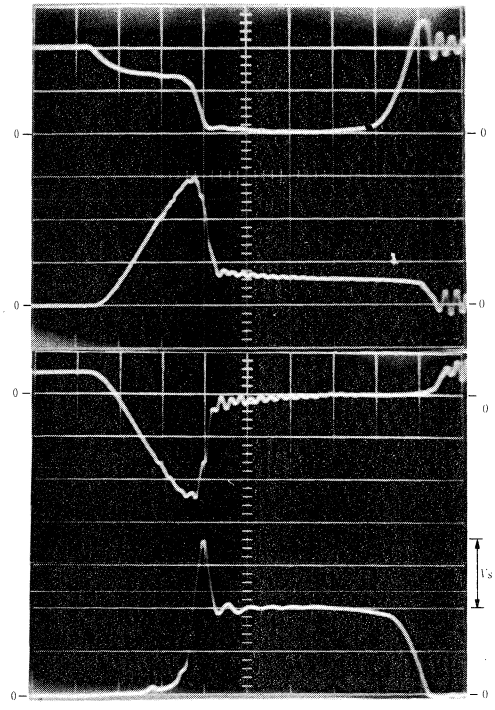
Test Conditions $\begin{bmatrix} V_{CC}=100\text{V},\ f=20\text{kHz} \\ V_{GS}=\begin{matrix}+15\text{V} \\ -10\text{V}\end{matrix},\ I_D=5\text{A},\ di/dt=80\text{A}/\mu\text{s} \end{bmatrix}$

Photo. Ⓐ

〔Layout Conditions〕

① V_{CC}~D_1·S_2 : Twisted Pair Wire (L_S≒170nH)

② Lead of S_1·D_2 Terminals : 10cm Lead Wire (L_S≒100nH)



V_{DS1} : 50V/DIV (Drain-source Voltage Waveform of Q_1)

i_{D1} : 10A/DIV (Drain Current Waveform of Q_1)

i_{D2} : 10A/DIV (Drain Current Waveform of Q_2)

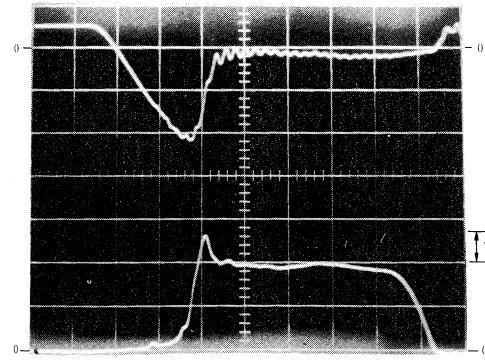
V_{DS2} : 50V/DIV (Drain-source Voltage Waveform of Q_2)

Photo Ⓑ

〔Layout Conditions〕

① V_{CC}~D_1·S_2 : Twisted Pair Wire (L_S≒170nH)

② Connection of S_1·D_2 Terminals : Copper Plate (L_S≒25nH)



i_{D2}

V_{DS2}

Fig. 4-7 (a) FET Q_1, Q_2 Voltage and Current Waveform, 2SK401 used

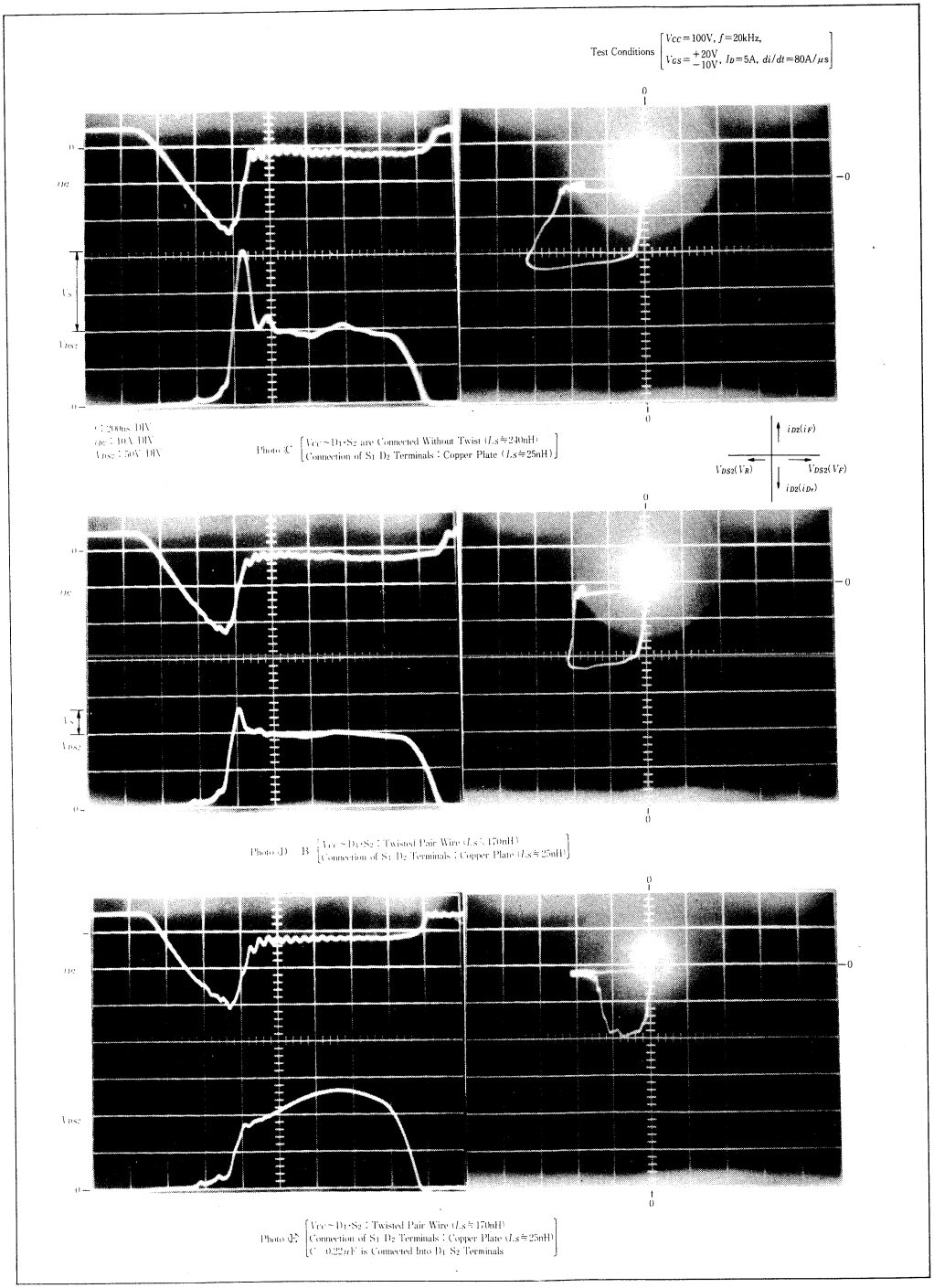


Fig. 4-7 (b) FET Q_2 Voltage and Current Waveform, 2SK401 used

4.7 Pay Attention to Circuit Layout

Stray inductance, in the circuit will cause over-voltage on high speed switching, slowing down of the switching speed (especially lead inductance at the gate), unexpected current unbalance among parallel connected devices, and also cause abnormal oscillations.

In order to solve these problems, circuit layout of power supply line and gate-source line must be minimized. This is done, by minimizing the area of current loops, by using twisted pairs of lead, and local decoupling capacitors abbrivi-ate the affects of any residual circuit inductance.

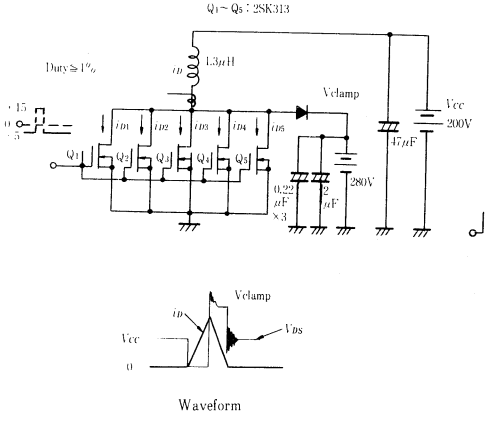
Circuit layout should be kept as symmetrical as possible in order to maintain the current balance in parallel connection.

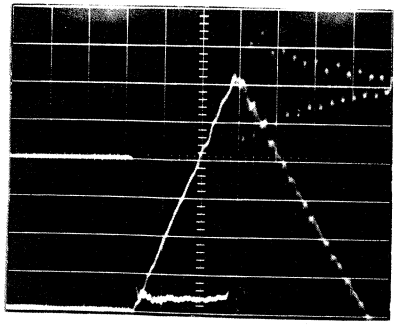
When devices is in parallel connection, small ferrite beads should be placed over the gate connections, or resistors in series (50 ~ 150Ω) should be placed into each gate, as to prevent abnormal oscillations.

4.8 Current dispersion at parallel connection in the high-speed switching operation (Note for the circuit arrangement and inter-connection at parallel connection)

When the power MOS FET is used as an arcing machine, multiple FETs are connected in parallel to obtain high current. In this case, because of high-speed operation (f = 200 to 500 kHz), floating inductance in the circuit may cause in transient voltage spike and current dispersion.

The former can be counteracted by shorten-ing and thickening the wires as much as pos-sible and as to the latter, some devices should





Waveform in the Experimental Circuit (I_D=30A)
V_{DS}=50V/DIV, I_D=5A/DIV, t=100ns/DIV

Fig. 4-8 Experimental Circuit Waveform

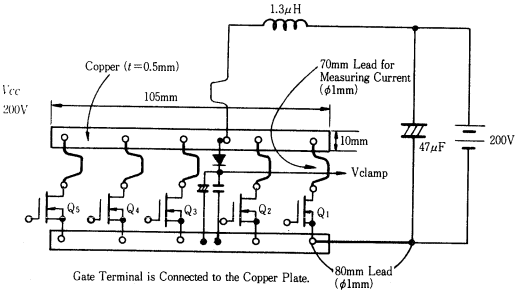


Fig. 4-9 Interconnection (I)

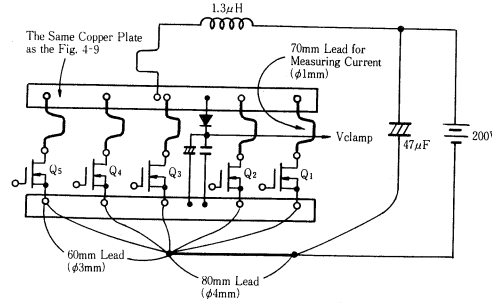


Fig. 4-10 Interconnection (II)

Table 4-2 Characteristics of sample 2SK313 and Current dispersion data in the circuit arrangement and interconnection

Item / No.	Electrical Characteristics					Current distribution (i_D=30A)	
	$V_{(BR)DSS}$ (V)	I_{DSS} (nA)	V_{th} (V)	g_m (S)	R_{on} (Ω)	Interconnection (I)	Interconnection (II)
	I_D=10mA V_{GS}=0	V_{DS}=360V V_{GS}=0	V_{DS}=10V I_D=1mA	V_{DS}=10V I_D=6A	V_{GS}=15V I_D=6A		
Q_1	502	9.0	2.98	3.31	0.66	i_{D1}≒8.0A	6.0A
Q_2	499	133	3.10	3.18	0.65	i_{D2}≒6.5	6.0
Q_3	502	27	3.11	3.19	0.65	i_{D3}≒5.7	5.8
Q_4	487	5.0	3.01	3.28	0.61	i_{D4}≒5.0	6.0
Q_5	476	17	3.02	3.29	0.58	i_{D5}≒4.8	6.2

be inquired in the circuit arrangement and interconnection. As to 2-type interconnections in Fig. 4-9 and Fig. 4-10, the current dispersion at parallel connection is measured in Fig. 4-8 Experimental circuit.

Table 4-2 shows main characteristics of used 5 FETs and current dispersion data in each interconnection.

As shown in Table 4-2, in Fig. 4-9 interconnection (I), as to Q_1 and Q_2, interconnection inductances of drain and source are small. As to current, Q_1 is the largest, about 8.0A, and Q_5 which has the largest interconnection inductance has the smallest current, about 4.8A. Current dispersion between devices is large. (See Fig. 4-11 Waveform photograph) Therefore, in Fig. 4-10 interconnection (II), source interconnection is equalized and interconnection inductance is balanced. In this method, as shown in Table 4-2 and Fig. 4-12 Waveform photograph, the current between devices is almost balanced. If the characteristics such as V_{th}, g_m, and R_{on} are met, the current between devices varies with circuit arrangement and interconnection. Therefore, to reduce the current dispersion of the power MOS FETs in parallel connection, circuit interconnection of each device should be placed symmetrically.

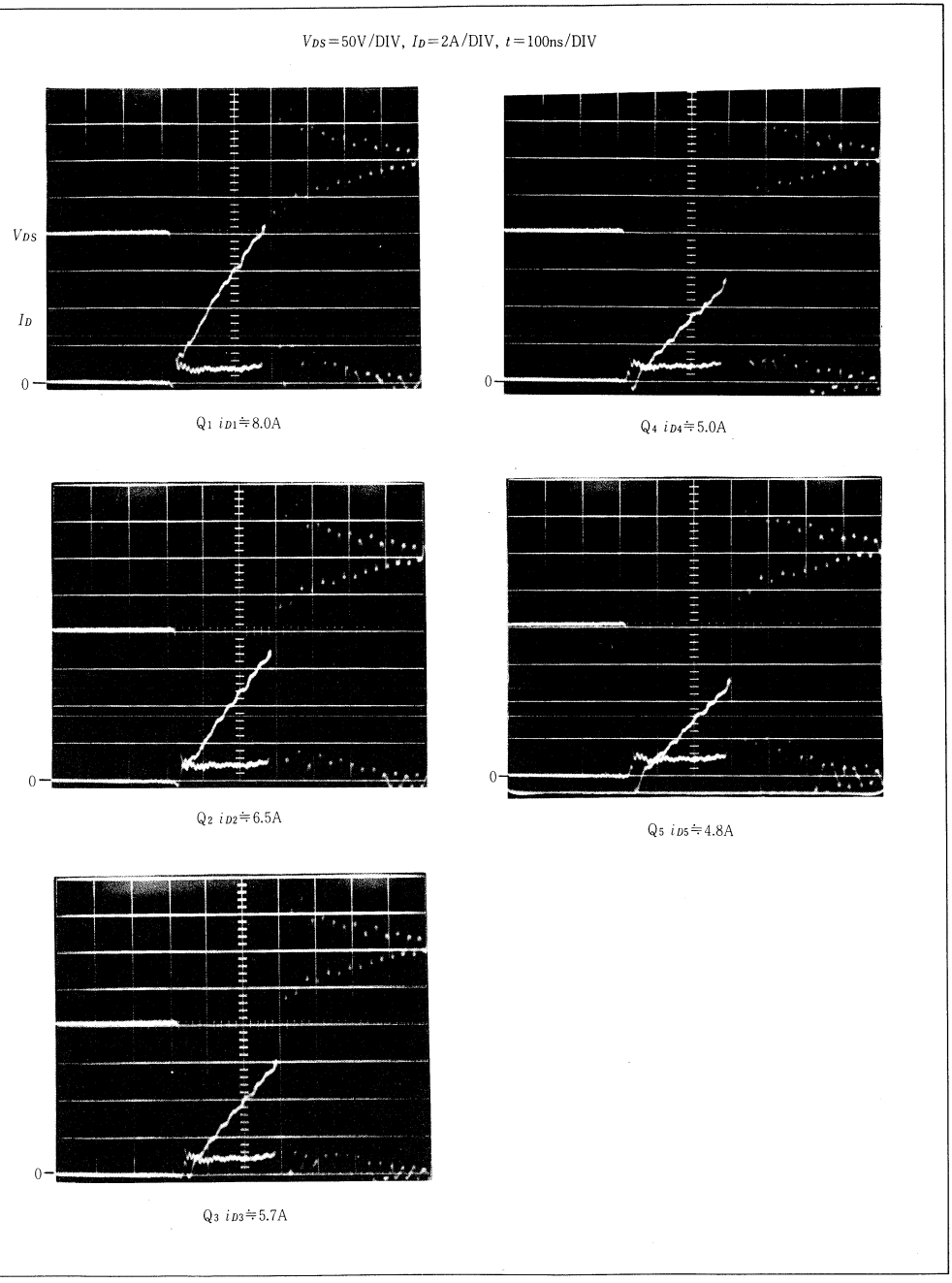


Fig. 4-11 Current distribution in the 2SK313 L load switching parallel operation (Interconnection I)

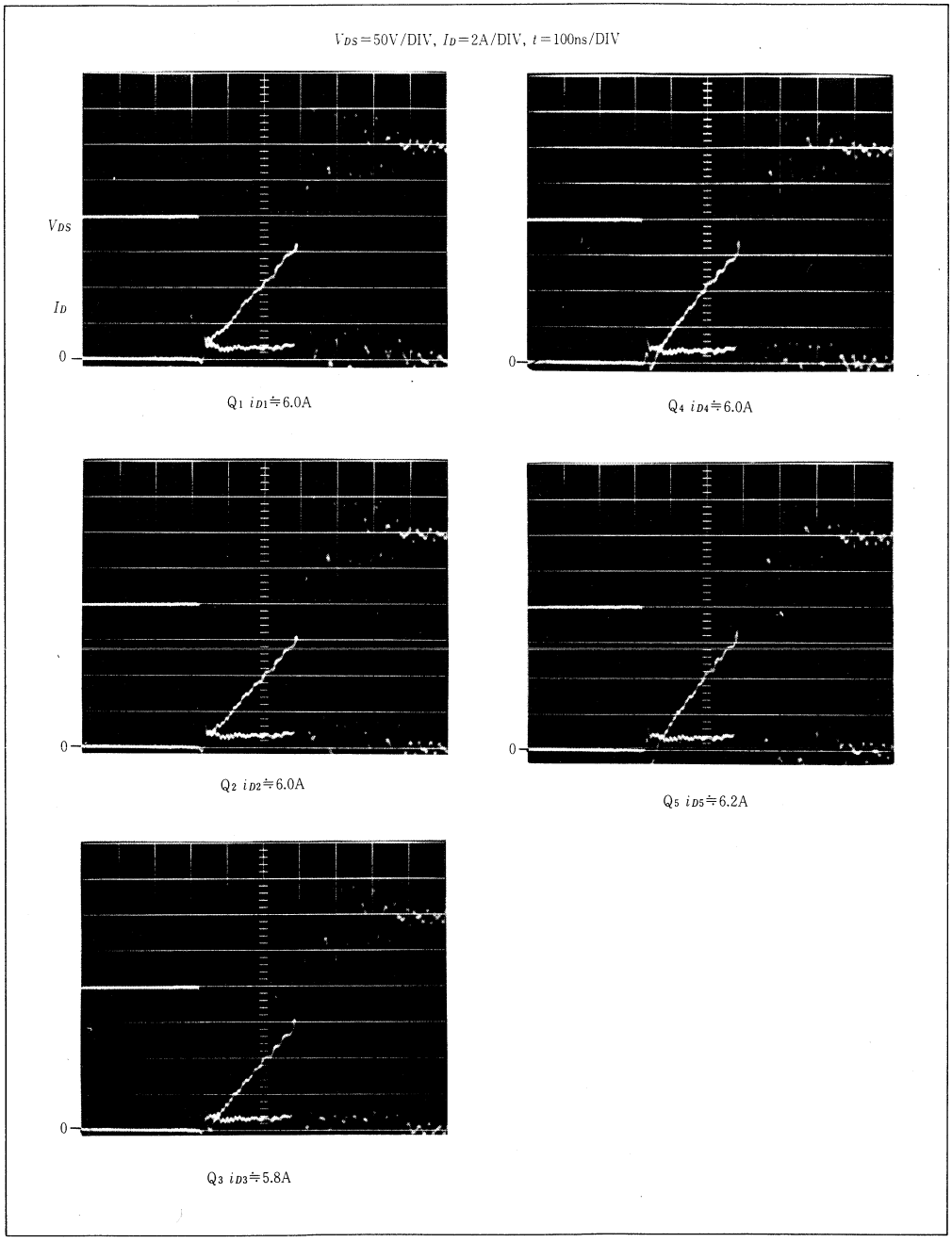


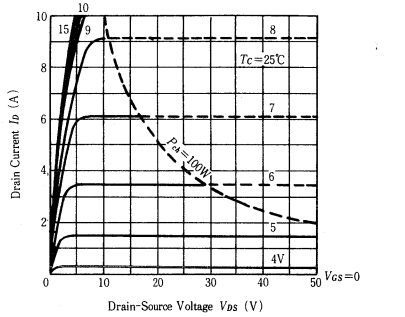
Fig. 4-12 Current distribution in the 2SK313 L load switching parallel operation (Interconnection II)

5. CHARACTERISTICS OF POWER MOS FETS

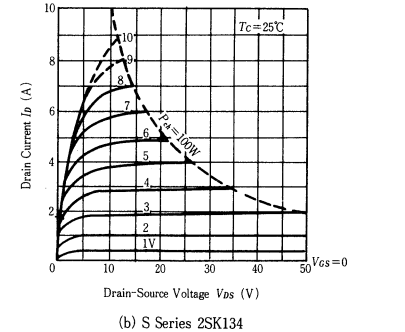
5.1 Output Characteristics

Fig. 5-1 shows the output characteristics of the D series 2SK413 and S series 2SK134, which have the same specification. Whereas in a small signal MOS FET the forward transconductance $|Y_{fs}|$ is 10 ~ 20 mS (milli-Siemens) at best, in a power MOS FET it is 1.0 ~ 15S. Also, as is obvious from Fig. 5-1, they have what is called pentode characteristics and excellent linearity of $|Y_{fs}|$ in relation to I_D.

P channel MOS FETs also have similar characteristics. P channel and N channel types have complementary characteristics.



(a) D Series 2SK413



(b) S Series 2SK134

Fig. 5-1 Typical Output Characteristics

5.2 Frequency Response Characteristics

One of the outstanding features of the power MOS FET is that it has excellent high speed and high frequency characteristics. Therefore, they can be applied in high-speed switching regulators, high-output broadcasting transmitters, etc.

The cut-off frequency of an intrinsic MOS FET is defined by the ratio of the mutual conductance and the input capacitance, and in a typical MOS FET, it will be in the order of GHz. In fact, however, the cut-off frequency is limited by the parasitic resistance and the input capacitance of the gate.

Fig. 5-2 shows the equivalent circuit of MOS FET in the saturation region.

In Fig. 5-2, the cut-off frequency (f_c), at which the voltage gain falls to −3dB of its low-frequency value, is given by the following equation.

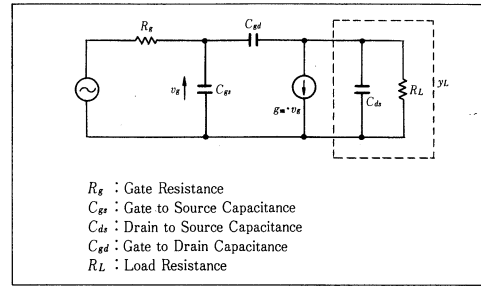


Fig. 5-2 Equivalent circuit of MOS FET

$$f_c \simeq \frac{1}{2\pi} \cdot \frac{1}{R_g\{C_{gs} + (1 - A_0)C_{gd}\}} \quad \cdots\cdots (1)$$

Here, A_0 is the low-frequency voltage gain, and R_g is the series resistance of the gate.

Fig. 5-3 shows the cut-off frequencies of the vertical and the lateral structure devices, found by substituting into equation (1) the parameters (calculated values) of a power MOS FET which has a silicon gate. In the lateral structure, C_{gd} is much smaller than C_{gs}, and can be neglected.

In the vertical structure, as explained in paragraph 2, C_{gs} is a function of the voltage gain (A_0) in the low frequency region, because C_{gd} is large.

We would like to summarize the above, as follows.

(1) In the case of low voltage gain, the cut-off frequencies of the vertical and the lateral structures show the same level. The input impedance ratio at f_C depends on R_g ratio, so the impedance of the vertical structure is 1.5 ~ 2 times lower than that of the lateral structure.

(2) In the case of high gain amplifier circuits, the frequency characteristics of the lateral structure and better than that of the vertical structure, because in the vertical structure the feedback capacitance (C_{gd}) has a great influence.

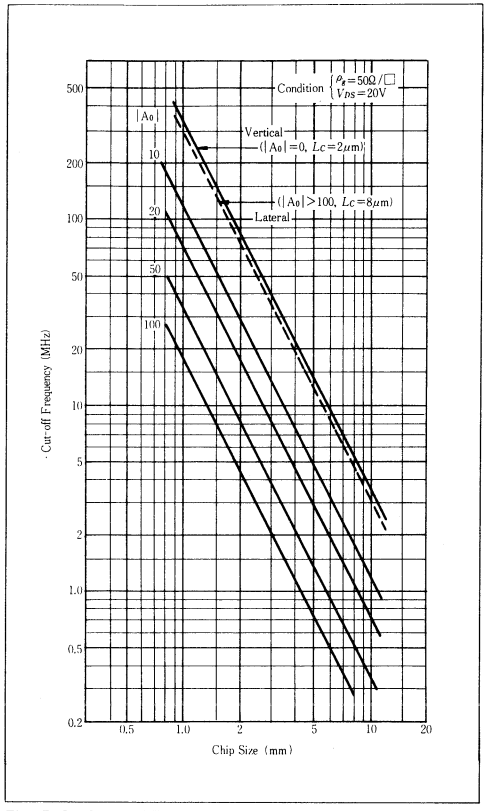


Fig. 5-3 Cut-off Frequency of Silicon Gate Power MOS FETs

To further improve the frequency characteristics, the use of low resistance material such as metal is required. This will improve the cut-off frequency by 10 ~ 100 times. Fig. 5-4 shows the frequency characteristics and the test circuits of typical kinds of MOS FETs. In 2SK317 and 2SK221Ⓗ, the gate material is metal-gate.

5.3 Switching Characteristics

When using power MOS FETs for power switching, such as in switching regulators, the load of the switching device is usually inductive. Here, however, we would like to assume a resistance load, because it can be treated easily.

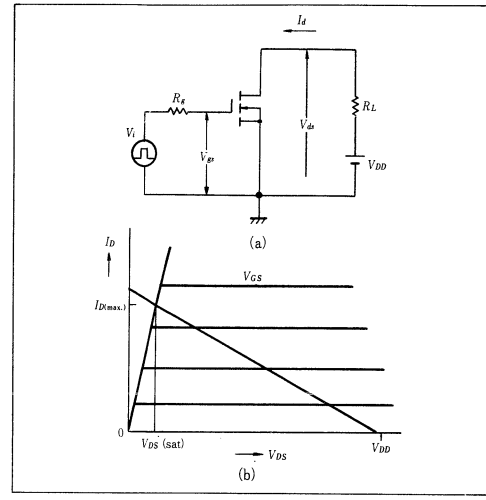


Fig. 5-5 Switching Circuit and Typical Output Characteristics & Load Curve

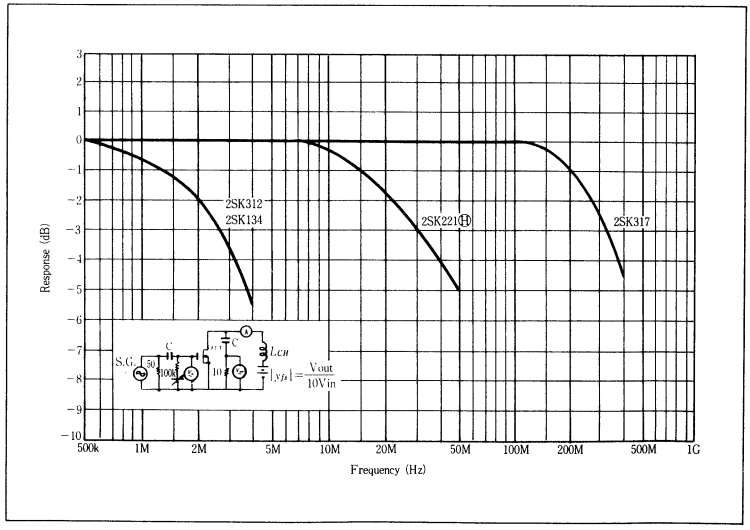


Fig. 5-4 Frequency Response Characteristics of y_{fs} (Source Common)

Fig. 5-5 shows the resistance load switching circuit (a), simplified current-voltage characteristics, and the load line (b). In this figure, we suppose that the rising curve of current vs. voltage is shown by a straight line, and g_m=0.

Therefore, in Fig. 5-5 (b), the point of the drain voltage=V_{DS}

(sat) is included in the non-saturation region, and the region of $V_{DS}>V_{DS}$ (sat) is the saturation region.

In the lateral structure, C_{gd} is much smaller than C_{gs} and C_{ds}, so it can be neglected. The time constants are given by the following equations.

$$\tau_i \simeq R_g \cdot C_{in}=R_g \cdot C_{gs} \quad \cdots\cdots\cdots\cdots\cdots (2)$$

$$\tau_o \simeq R_L \cdot C_{out}=R_g \cdot C_{ds} \quad \cdots\cdots\cdots\cdots\cdots (3)$$

τ_i : input time constant

τ_o : output time constant

Then, the switching waveform is shown in Fig. 5-6.

The quantity of charge, Q_{on}, which is stored in the gate and shows how easily the device can be driven, is given by the following equation.

$$Q_{on}=C_{gs} \cdot V_G \text{ max} \quad \cdots\cdots\cdots\cdots\cdots (4)$$

The transitional charge current (i_{rush}) is given as follows.

$$i_{rush}=\frac{C_{gs} \cdot V_G \text{ max}}{t_{on}} \quad \cdots\cdots\cdots\cdots\cdots (5)$$

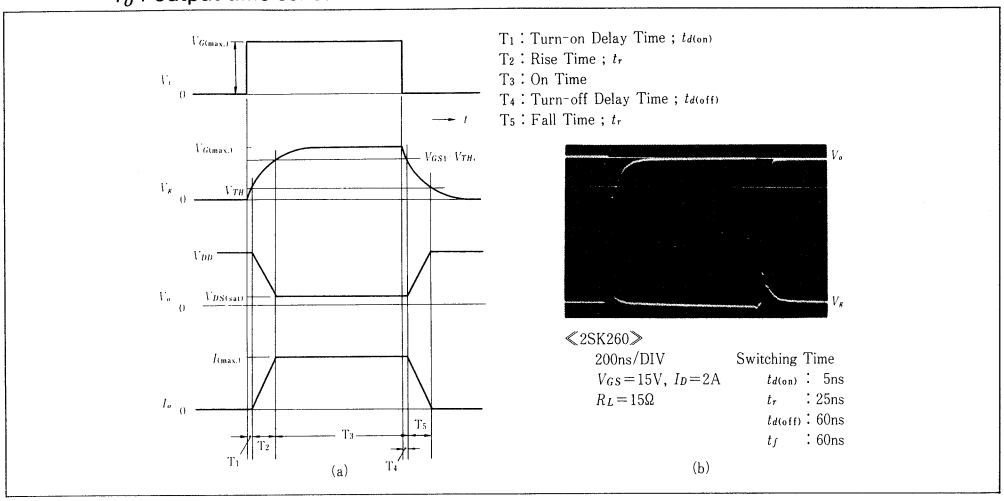


Fig. 5-6 Switching Waveform of Lateral Power MOS FETs

In the vertical structure, the feedback capacitance (C_{gd}) is large and depends largely on the drain voltage, so the operation analysis will be more complicated. Fig. 5-7 shows the C_{gd}-drain voltage dependency of the vertical and the lateral structures (2SK312, 2SK260) under the conditions of the same chip size and the same 400V breakdown voltage. With a depletion layer spreading in the drain just under the gate electrode, the value of C_{gd} will decrease sharply.

Considering the above, we would like to show the C_{gd}- and g_m-drain voltage dependencies in Fig. 5-8 at $V_{GS}>V_{DS}$, C_{gd} is equal to C_{gd0}, the oxide film capacitance just under the drain electrode. When $V_{GS}<V_{DS}$, the depletion layer expands to the drain region, and $C_{gd}<<C_{gs}$. The threshold voltage, at which the drain surface is P-inverted, is supposed to be 0. Under these conditions, we would like to look at the switching operations. When the drain voltage is in the region of $V_{DS}>V_{DS}$ (sat), the device is in the saturation region, and in the region of V_{DS} (sat) $<V_{DS}<V_{GS}$, C_{gd} is equal to C_{gd0}. The equivalent circuit is as shown in Fig. 5-8 (c). The time constant of the input capacitance at charging or discharging is given by the following equations.

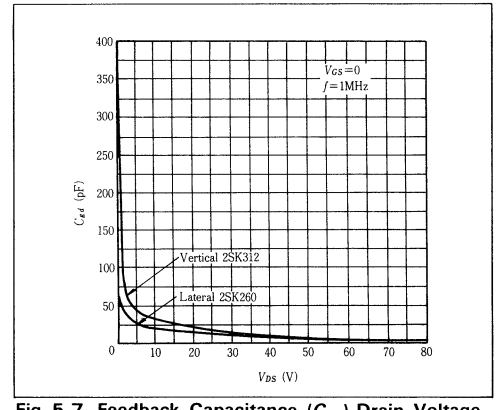


Fig. 5-7 Feedback Capacitance (C_{gd})-Drain Voltage Dependency

$$\tau_1 \simeq R_g \cdot C_{gs} \ (V_{DS}>V_{GS})$$

$$\tau_1' \simeq R_g \{C_{gs}+(1+g_m \cdot R_L)\}C_{gd}$$

$$(V_{DS} \text{ (sat)} <V_{DS}<V_{GS}) \quad \cdots\cdots\cdots (6)$$

When $V_{DS}=V_{DS}$ (sat), the device is in the non-saturation region. The equivalent circuit is

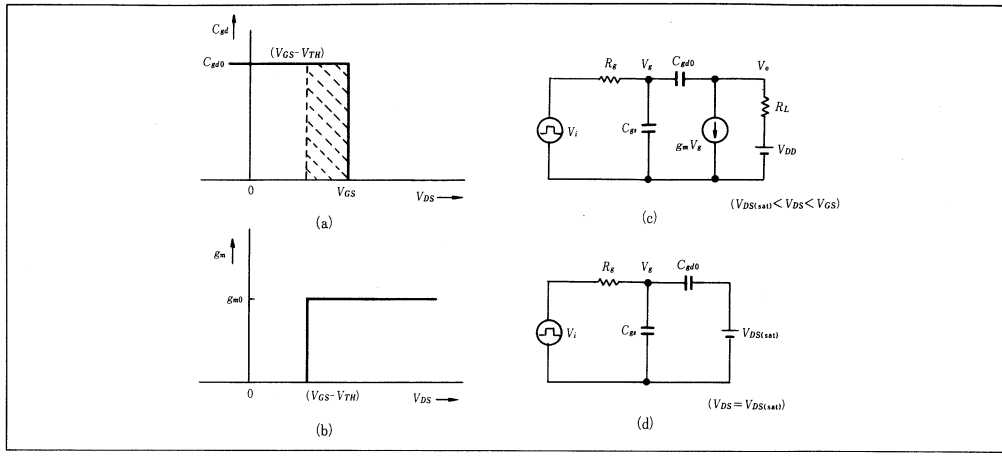


Fig. 5-8 Drain Voltage Dependencies of C_{gd} and g_m (a), (b), & Equivalent Circuit (c), (d)

as shown in Fig. 5-8 (d) and the time constant is given as follows.

$$\tau_2 \simeq R_g (C_{gs} + C_{gd0}) \quad \cdots\cdots\cdots\cdots\cdots (7)$$

Fig. 5-9 shows the switching waveform as a model, based on the above operations. T_1, T_2, T_4, and T_5 show the turn-on delay time $t_{d(on)}$, the rise time t_r, the turn-off delay time $t_{d(off)}$ and the fall time t_f ($t_{on} = t_{d(on)} + t_r$, $t_{off} = t_{d(off)} + t_f$) respectively.

$T_6 \sim T_9$ show the charging and discharging time of C_{gd}. T_6 and T_9 indicate the region in which the mirror integration is operated, and it is equal to the time to charge and discharge the changes, whose quantity is equivalent to the shaded part of Fig. 5-8 (a).

Fig. 5-9 (b) shows the gate driving waveform V_g and the output voltage waveform V_o of the vertical structure, as actually measured. The gate voltage waveform is similar to the basic waveform shown in (a), quantitatively. This

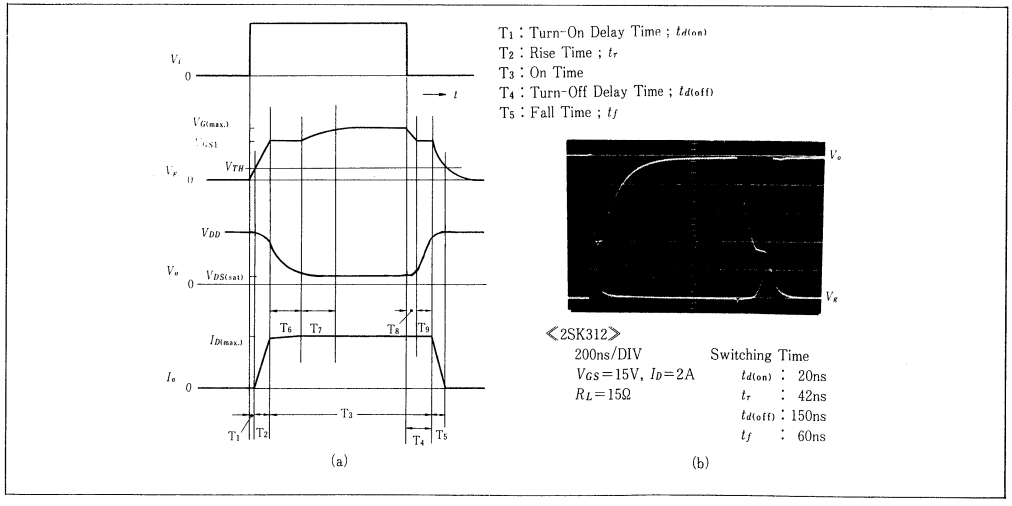


Fig. 5-9 Switching Waveform of Vertical Power MOS FET

means that we can explain the switching operation using the approximate values of the feed back capacitance and g_m shown in Fig. 5-8 (a), and (b).

The quantity of stored charges, which shows how easily the gate can be driven, is given by the following equation.

$$Q_{on} = (C_{gs} + C_{gd0}) V_{G\,max} \quad \cdots\cdots\cdots\cdots (8)$$

The transitional charge current (i_{rush}) is given as follows.

$$i_{rush} = \frac{(C_{gs} + C_{gd0})V_{G\,max}}{t_{on}} \quad \cdots\cdots\cdots (9)$$

The following summarizes a comparison of the switching operations of the vertical and the lateral structures.

(1) The gate driving power required is determined by the ratio of the quantity of stored charges in gate capacitance. The driving power for the vertical structure device is larger than that for the lateral structure device by $(C_{gs} + C_{gd0})D/(C_{gs})S$.

(2) When the device is driven by a high speed pulse, the rise time (t_r) and the fall time (t_f), for both structures, are given by the following equations.

$$t_r \simeq C_{gs} R_g \ln \left(\frac{V_{Gmax} - V_{th}}{V_{GSmax} - V_{GS1}}\right) \quad \cdots\cdots (10)$$

$$t_f \simeq C_{gs} R_g \ln \left(\frac{V_{GS1}}{V_{th}}\right) \quad \cdots\cdots\cdots\cdots (11)$$

Here V_{GS1} is the gate voltage for saturation.

We would like to show the gate resistance (R_g) and the gate — source capacitance (C_{gs}) in Table 5-1, for reference.

In the vertical structure, t_r and t_f are faster than those of the lateral one, because of the small value of the gate resistance. The turn-off delay time, however, is larger, so the value of t_{off} ($= t_{d(off)} + t_f$) will be larger.

In an actual circuit, the output resistance (R) of the drive circuit will be added to this gate resistance (R_g).

Therefore, in high speed operation, the vertical structure device should be designed so that the output resistance of the drive circuit will be as small as possible, by adding one or two emitter follower circuits to the driver.

Fig. 5-10 and Fig. 5-11 show the turn off time of the device with the drive circuit added and that of the standard measuring circuit. Moreover, as shown in circuit (c), the operation speed will be further improved by making the gate potential negative at cut off time.

In power MOS FETs, in contrast with bipolar transistors, the switching time is not influenced by temperature, and the circuit design will be easier. Fig. 5-12 shows the relation of the switching time vs. temperature characteristics, compared to that of bipolar transistors.

Table 5-1 Gate Resistance (Rg) and Gate-Source Capacitance of Each Device

Category	Package	Type Number		Gate Material	Rg (Ω)	Cin (pF)	f_c (MHz)
		N-ch	P-ch		V_{DS} = 10 V, V_{gs} = −5 V, f = 1 MHz		
D Series	DPAK	2SK375	—	Silicon Gate	35	400	15
	TO-126	2SK511	—	Silicon Gate	2	40	250
	TO-220 AB	2SK346	2SJ102	Silicon Gate	3/3	650/1400	7/7
		2SK294	—		3	900	5
		2SK296	—		35	400	10
		2SK310	2SJ117		3/4	1200/1200	10/10
		2SK319	—		3	2000	5
	TO-3P	2SK413	2SJ118	Silicon Gate	2/2	1800/2500	3/3
	TO-3	2SK308	—	Silicon Gate	5	2300	4
		2SK298	2SJ116		3/4	2100/4100	5/3
		2SK312	—		3	4100	3
		2SK351	—		3	6000	2
S Series	TO-220 AB	2SK213	2SJ76	Silicon Gate	20/30	90/120	40/30
	TO-3	2SK134	2SJ49	Silicon Gate	40/40	600/900	3/2
		2SK175	2SJ55		80/70	600/1200	2/1
		2SK221 Ⓗ	—	Metal Gate	2	600	50
		2SK258 Ⓗ	—	Silicon Gate	20	800	7
		2SK260 Ⓗ	—		20	800	7
	RFPAK	2SK317	—	Metal Gate	2	600	300

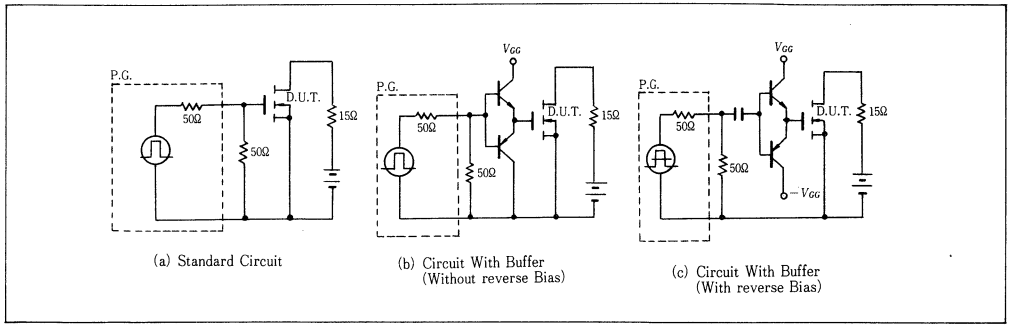


Fig. 5-10 Drive Circuit

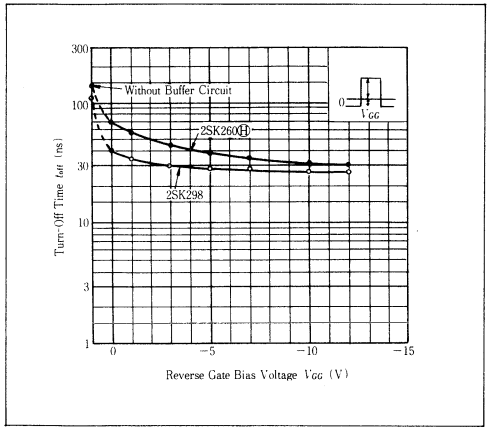


Fig. 5-11 Turn-Off Time vs. Reverse Gate Bias

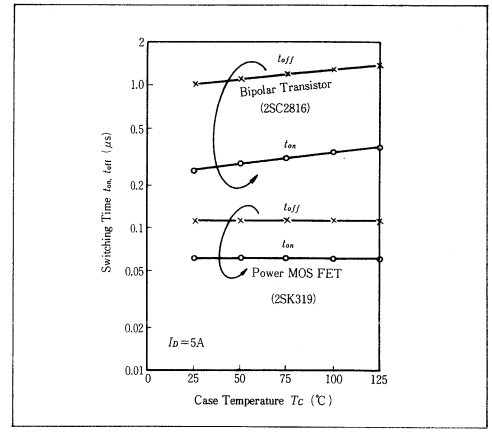


Fig. 5-12 Switching Time vs. Case Temperature

5.4 Input Dynamic Characteristics

Generally, when calculating the peak-rush current necessary for charging drive loss and gate input capacity in designing the power MOS FET drive circuit, evaluate from the following equations.

Drive loss $P_d = f \cdot C_{in} \cdot V_{GS}$ ..... (12)

Peak rush current $i_{(rush)} = \frac{C_{in} \cdot V_{GS}}{t}$ .. (13)

Where, input capacity C_{in} is generally the value when the bias is fixed in the data sheet. If using this value as it is, some problems occur. This is because in the C_{in}, gate drain capacity C_{gd}, which is a mirror capacity, exists, and is a function of the drain-source voltage V_{DS}. Also, since the gate-source capacity, C_{gs} is a function of V_{GS}, it contains complicated elements. These details are described in 5.3 Switching Characteristics. It is very complicated to design the drive circuit. As a function of V_{GS} and V_{DS}, gate charge load Q_g should be regulated.

(1) Gate charge factor

Fig. 5-13 shows the measurement circuit of the gate charge load, Q_g. This measuring theory is that when driving the gate with constant current, I_g, the time axis, t is multiplied by I_g and the time axis reads as the load, Q_g.

Fig. 5-14 shows $Q_g - V_{GS}$, V_{DS} characteristics at Turn-on and Turn-off measured in 2SK299. The vertical axis represents the drain-source voltage V_{DS}, and the gate-source voltage V_{GS}. The horizontal axis represents the gate charge load Q_g. In waveforms (a) and (b), the stage rised from zero shows the gate-source capacity C_{gs} charging time, and the next flat stage shows the gate-drain capacity C_{gd} charging time. To the contrary, waveforms (c) and (d) shows the discharging time. The loads necessary for charging C_{gs} and C_{gd} are

different from each other.
Fig. 5-15 shows Q_g — V_{GS} characteristics when V_{DD}·I_D of 2SK299 is a parameter. In Fig. 5-15-(b) waveform, the charge necessary for flowing V_{DD} = 100V and I_D = 1A is 16 nC. At this time, necessary V_{GS} is about 5.2V. (This value changes by V_{th}, g_m). However, in the actual switching operation, it is generally used in the following conditions that drain-source voltage is in "ON" (saturation) state, and a margin is added to reduce the ON resistance, and the overdrive when V_{GS} = 10 to 15V. Therefore, when designing the drive voltage as I_D = 1A, V_{GS} = 10V, the gate charge load is 28nC. Q_g is different between V_{DD} = 100V and V_{DD} = 200V because C_{gd} varies with V_{DS}.

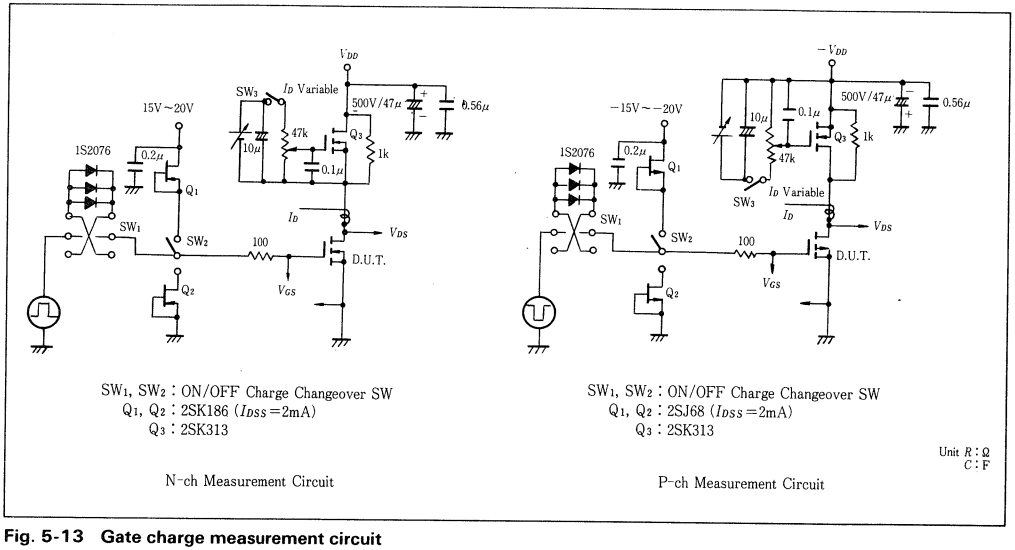
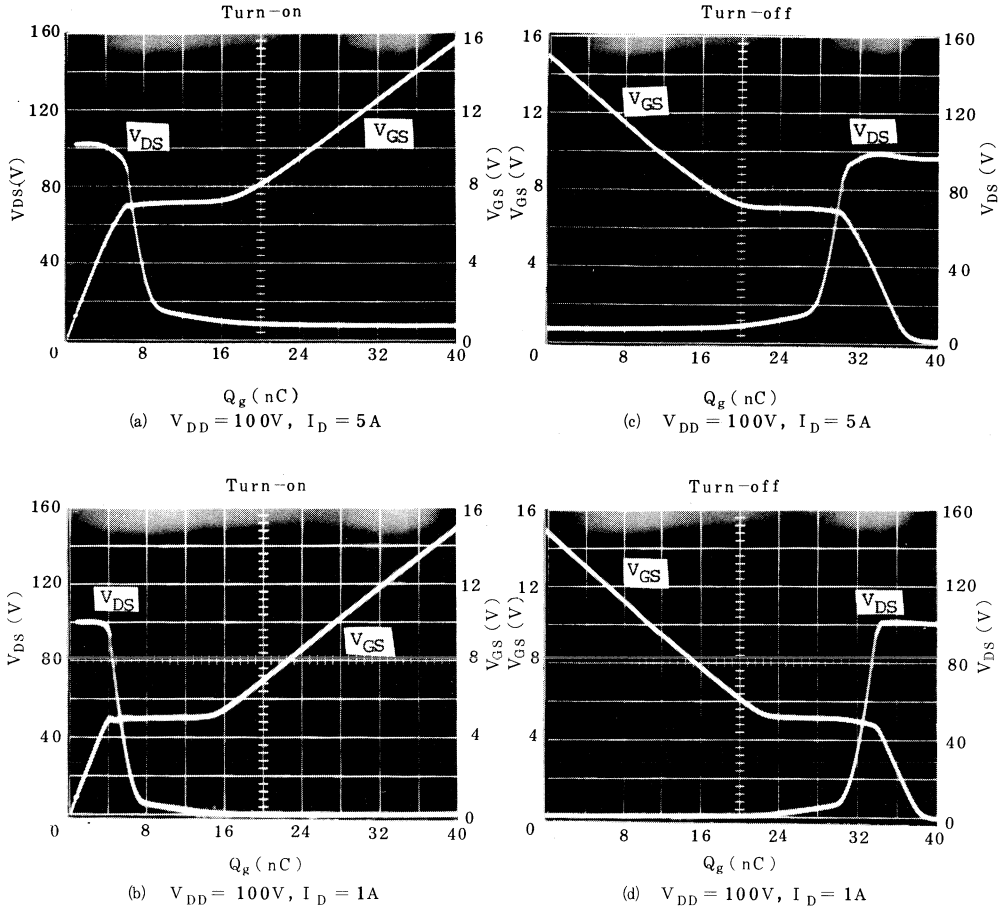


Fig. 5-13 Gate charge measurement circuit



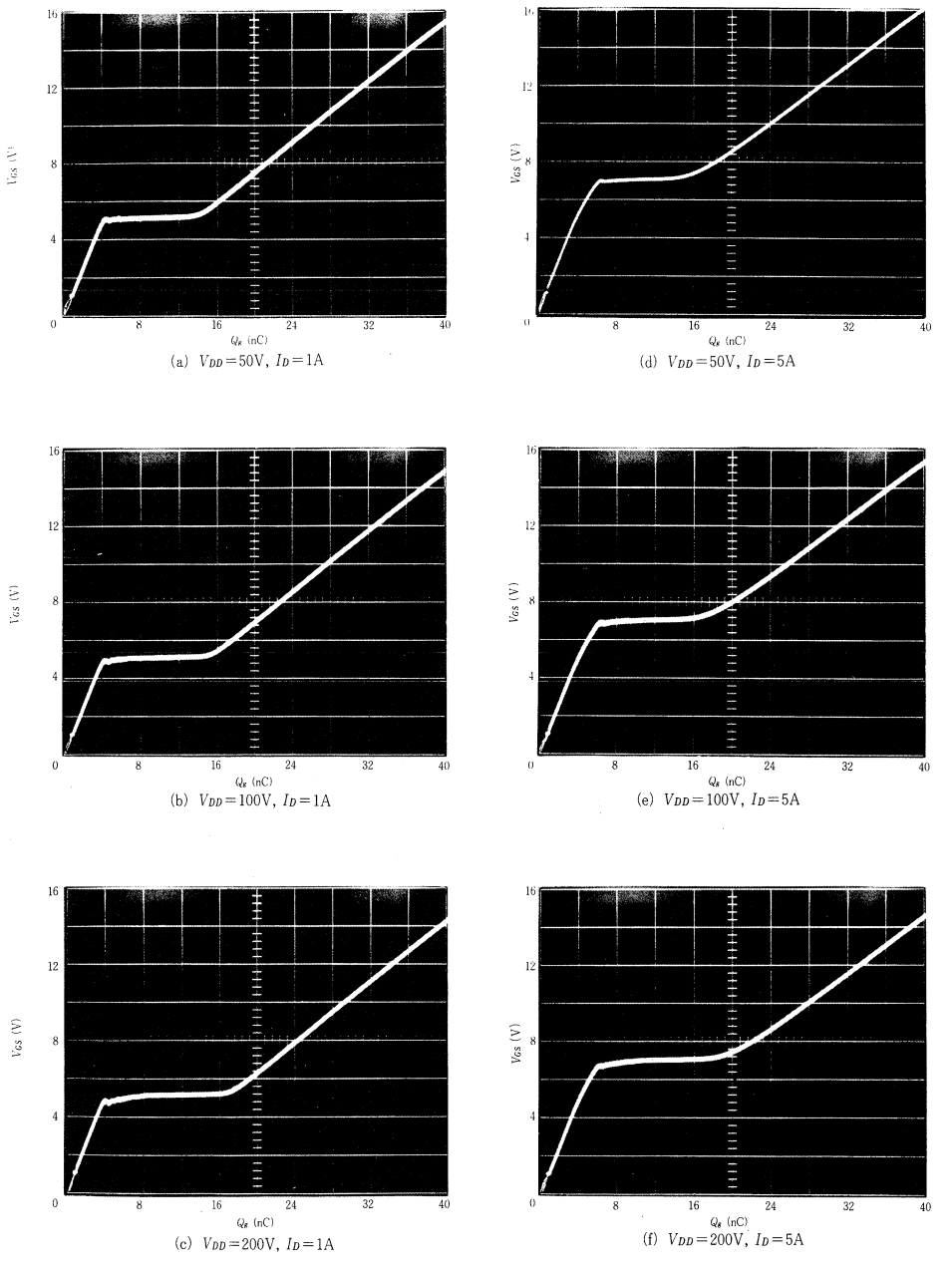
(a) $V_{DD} = 100V$, $I_D = 5A$

(c) $V_{DD} = 100V$, $I_D = 5A$

(b) $V_{DD} = 100V$, $I_D = 1A$

(d) $V_{DD} = 100V$, $I_D = 1A$

Fig. 5-14 2SK299 $Q_g - V_{GS} \cdot V_{DS}$ Characteristics



(a) V_{DD}=50V, I_D=1A

(b) V_{DD}=100V, I_D=1A

(c) V_{DD}=200V, I_D=1A

(d) V_{DD}=50V, I_D=5A

(e) V_{DD}=100V, I_D=5A

(f) V_{DD}=200V, I_D=5A

Fig. 5-15 2SK299 $Q_g - V_{GS}$ Characteristics

(2) Designing of drive circuit

The drive loss and necessary peak rush current of the drive circuit are evaluated by the following equations with the gate charge load Q_g.

Drive loss $P_d = f \cdot Q_g \cdot V_{GS}$ ..... (14)

Peak rush current $i_{(rush)} = \dfrac{Q_g}{t}$ ..... (15)

<Example>

Using the 2SK299, when $f = 100$kHz, $V_{DD} = 100$V, $V_{GS} = 15$V, switching time $t_{on} = 50$ ns, and $I_D = 5$A, what is the drive loss and necessary peak rush current?

<Solution>

Since Q_g in the above conditions is 39 nC in Fig. 5-15 (e),

$$P_d = f \cdot Q_g \cdot V_{GS}$$
$$= 100 \times 10^3 \times 39 \times 10^{-9} \times 15$$
$$= 58.5 \text{ mW}$$
$$i_{(rush)} = \frac{Q_g}{t} = \frac{39 \times 10^{-9}}{50 \times 10^{-9}} = 0.78\text{A}$$

As shown above, the answer can be obtained with ease.

Fig. 5-16 shows the comparison between the drive loss measured by the Fig. 5-17 Circuit and the drive loss calculated using the equation (14). The horizontal axis represents frequency. As shown in this figure, calculated value and measured value match well, which indicates that determining the gate charge Q_g facilitates designing the drive circuit accurately.

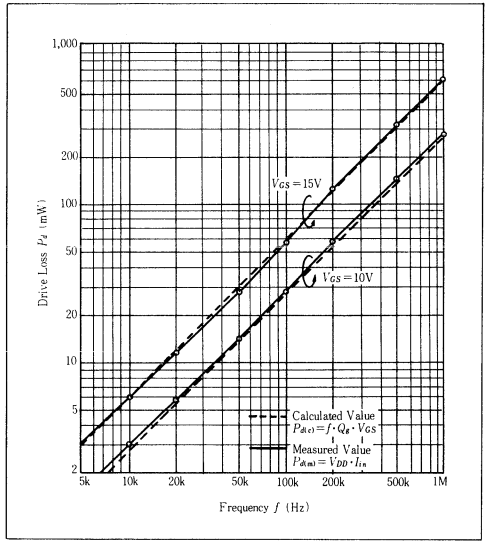


Fig. 5-16 Drive loss of Power MOS FET (2SK320)

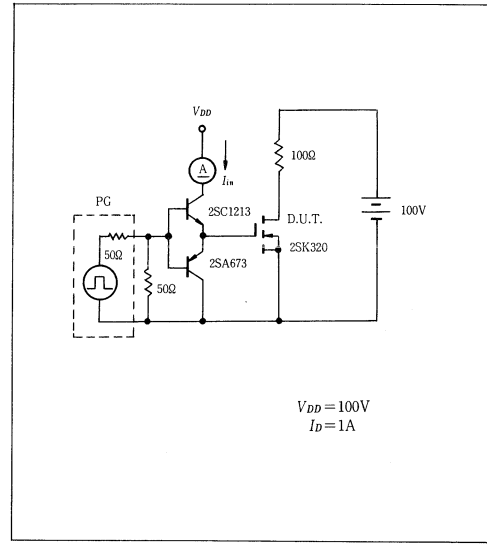


Fig. 5-17 Test circuit

(3) Gate Charge Characteristics

Fig. 5-18 shows typical gate charge characteristics and the waveforms of V_{GS}, V_{DS} and I_D. The characteristic curve can be divided into three areas. Area 1 indicates a period in which the gate source capacity (C_{gs}) is charged until the V_{GS} reaches the value required to supply specific drain current I_D. The FET is "off" between the threshold voltage V_{GS}(th) and t_1 during this period. When the V_{GS} value exceeds V_{GS}(th), the drain current I_D begins to flow and becomes stable at t_2. Area 2 is a transition area between the V_{DS} active and inactive areas. That is, the drain source pressure V_{DS} varies and the gate drain (mirror) capacity C_{gd} is charged. This mirror effect increases C_{in}, activates the FET, the V_{DS} transition lessens, and as a result, the effect is lost at t_3. In area 3, the V_{DS} is inactive and doesn't very much. That is, the $V_{DS(on)}$ of the FET is maintained as $I_D \times R_{DS(on)}$. C_{in} (3) in area 3 is larger than C_{in}(1), but smaller than C_{in}(2). C_{in}(1) and C_{in}(3) correspond to C_{iss} and are equivalent to the value of $C_{gs} + C_{gd}$. However, C_{iss} and $C_{gs} + C_{gd}$ are not equal because the value of V_{DS} differs between areas 1 and 3 (the C_{gd} value differs). That is, C_{in}(3) of area 3 is larger than C_{in}(1) because of the large C_{gd} caused by the thin depletion

layer immediately under the gate.

(4) Calculating Method of Switching Time Using the Gate Charge Characteristic Q_g

Fig. 5-19 (c) shows a standard circuit which measures switching time, and Fig. 5-19 (a) shows the transient response characteristic of gate input pressure. In the figure (a), when C_{in} is fixed, the V_{GS} characteristic is;

$$V_{GS(t)} = V_{GG}\{1 - \exp(-\frac{t}{C_{in} \cdot R_s})\} \ldots (16)$$

V_{g1} and V_{g2} are;

$$V_{g1} = V_{GG}\{1 - \exp(-\frac{t_1}{C_{in} \cdot R_s})\} \ldots .. (17)$$

$$V_{g2} = V_{GG}\{1 - \exp(-\frac{t_2}{C_{in} \cdot R_s})\} \ldots .. (18)$$

t_1 and $t_2 - t_1$ can be got from formulas (17) and (18). They are as follows because C_{in} differs between area 1 and area 2 as seen from Fig. 5-20.

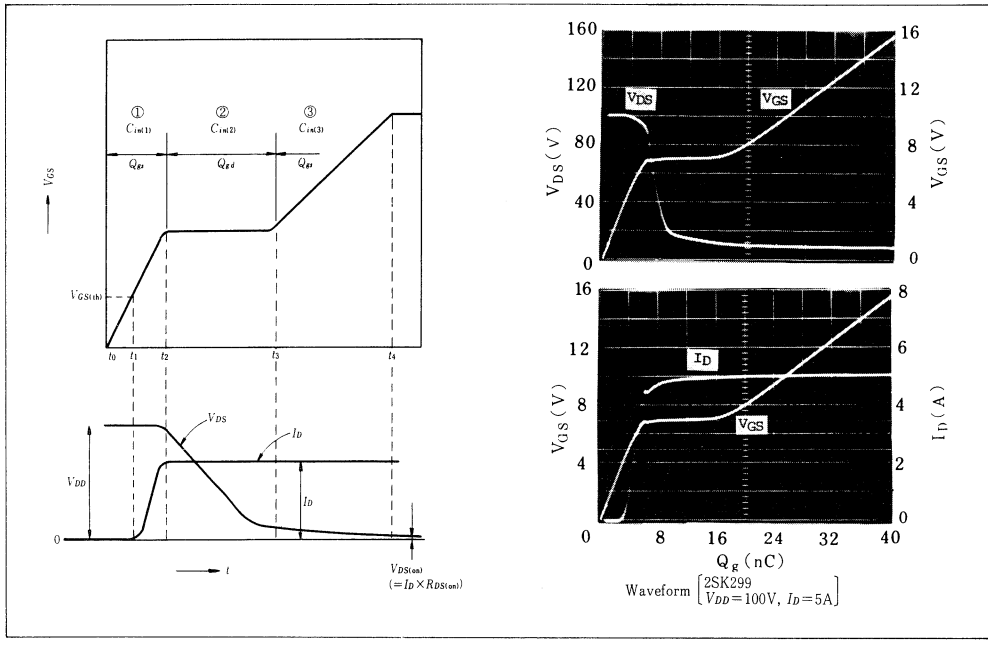


Fig. 5-18 Typical Gate Charge Waveform and V_{DS}, I_D Waveforms

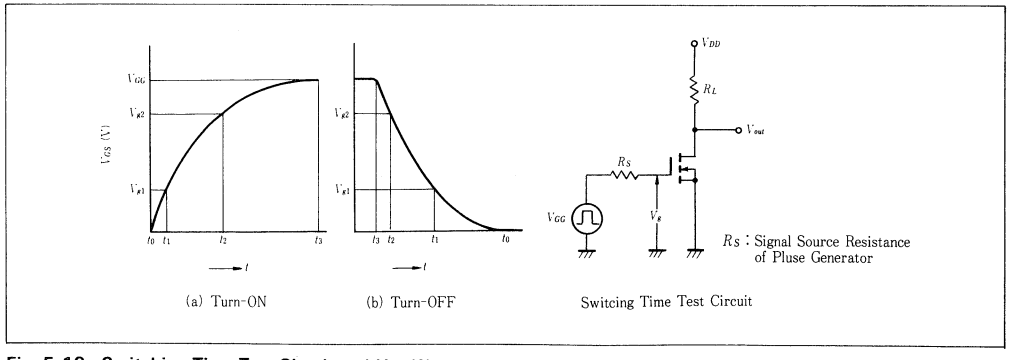


Fig. 5-19 Switching Time Test Circuit and V_{GS} Waveforms

$$t_1 = (C_{in}(1)\cdot R_s)\ \ln\left(\frac{V_{GG}}{V_{GG}-V_{g1}}\right) \quad \ldots (19)$$

$$t_2 - t_1 = (C_{in}(2)\cdot R_s)\ \ln\left(\frac{V_{GG}-V_{g1}}{V_{GG}-V_{g2}}\right) \quad \ldots (20)$$

$C_{in}(1)$ and $C_{in}(2)$ of area 1 and area 2 are obtained with following formulas.

$$C_{in}(1) = \frac{\Delta Q_g}{\Delta V_g} = \frac{Q_{g1}}{V_{g1}} \quad \ldots\ldots\ldots\ldots\ldots (21)$$

$$C_{in}(2) = \frac{\Delta Q_g}{\Delta V_g} = \frac{Q_{g2}-Q_{g1}}{V_{g2}-V_{g1}} \quad \ldots\ldots\ldots (22)$$

In the Fig. 5-20 waveforms, t_1 is the turn-on delay time $t_{d(on)}$, and $t_2 - t_1$ is the rise time t_r. If substituting formulas (21) and (22) for formulas (19) and (20), $t_{d(on)}$ and t_r are;

$$\therefore t_{d(on)} = \frac{Q_{g1}}{V_{g1}} \cdot R_s \ln\left(\frac{V_{GG}}{V_{GG}-V_{g1}}\right) \quad \ldots (23)$$

$$\therefore t_r = \left(\frac{Q_{g2}-Q_{g1}}{V_{g2}-V_{g1}}\right)\cdot R_s \ln\left(\frac{V_{GG}-V_{g1}}{V_{GG}-V_{g2}}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots (24)$$

The turn-off delay time $t_{d(off)}$ and fall time t_f can be also obtained using the above method. With Fig.5-19(b);

$$V_{GS(t)} = V_{GG}\cdot\exp\left(-\frac{t}{C_{in}\cdot R_s}\right) \quad \ldots\ldots\ldots (25)$$

t_2 and $t_1 - t_2$ are;

$$t_2 = (C_{in}(1)\cdot R_s)\ \ln\frac{V_{GG}}{V_{g2}} \quad \ldots\ldots\ldots\ldots (26)$$

$$t_1 - t_2 = (C_{in}(2)\cdot R_s)\ln\frac{V_{g2}}{V_{g1}} \quad \ldots\ldots\ldots (27)$$

With Fig. 5-21, $C_{in}(1)$ and $C_{in}(2)$ are;

$$C_{in}(1) = \frac{\Delta Q_g}{\Delta V_g} = \frac{Q_{g3}-Q_{g2}}{V_{GG}-V_{g2}} \quad \ldots\ldots\ldots (28)$$

$$C_{in}(2) = \frac{\Delta Q_g}{\Delta V_g} = \frac{Q_{g2}-Q_{g1}}{V_{g2}-V_{g1}} \quad \ldots\ldots\ldots (29)$$

In the Fig. 5-21 waveforms, t_2 is the turn-off delay time $t_{d(off)}$, and $t_1 - t_2$ is the fall time t_f.

$$\therefore t_{d(off)} = \left(\frac{Q_{g3}-Q_{g2}}{V_{GG}-V_{g2}}\right)\cdot R_s \ln\left(\frac{V_{GG}}{V_{g2}}\right) \quad \ldots (30)$$

$$\therefore t_f = \left(\frac{Q_{g2}-Q_{g1}}{V_{g2}-V_{g1}}\right)\cdot R_s \ln\left(\frac{V_{g2}}{V_{g1}}\right) \quad \ldots\ldots (31)$$

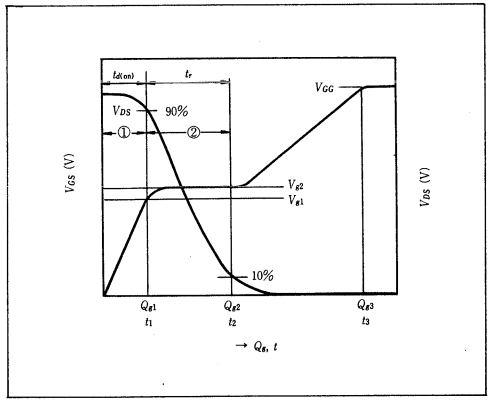


Fig. 5-20 Gate Charge Characteristic (Turn-on)

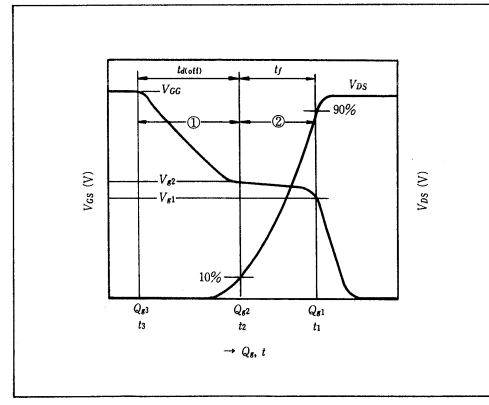


Fig. 5-21 Gate Charge Characteristic (Turn-off)

5.5 Area of Safe Operation (ASO)

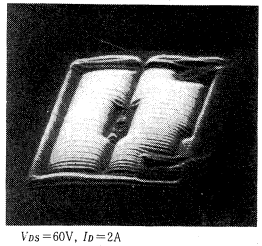
5.5.1 Forward Bias ASO

The most basic and important characteristic required for a power device is a high breakdown strength.

Since the current flowing in power MOS FETs does not concentrate locally, power MOS FETs are free from secondary breakdown in the high voltage region.

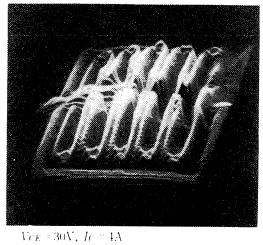
Fig. 5-22 shows thermal mapping of chip surfaces, under power on, for a power MOS FET and conventional bipolar transistor.

Whereas the thermal mapping in the power MOS FET is uniform, a hot spot is generated in the bipolar transistor, although the power applied is one-half that applied to the power MOS FET. Fig. 5-23 shows breakdown points of power MOS FETs in relation to those of bipolar transistors.ASO of bipolar transistors is limited by secondary breakdown in the high voltage region. On the other hand, in a power MOS FET, the guaranteed area of safe operation is equal to the range of thermal limitation. ASO design is very simple.



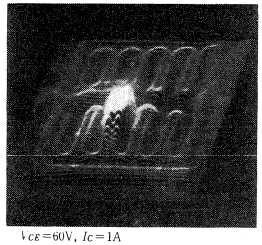
V_{DS}=60V, I_D=2A

(A) Power MOS FET (2SK135)



V_{CE}=30V, I_C=1A

(B) Bipolar Transistor (2SC1343)



V_{CE}=60V, I_C=1A

(C) Generation of Hot Spot
Bipolar Transistor (2SC1343)

Fig. 5-22 Chip Surface Temperature at Power ON

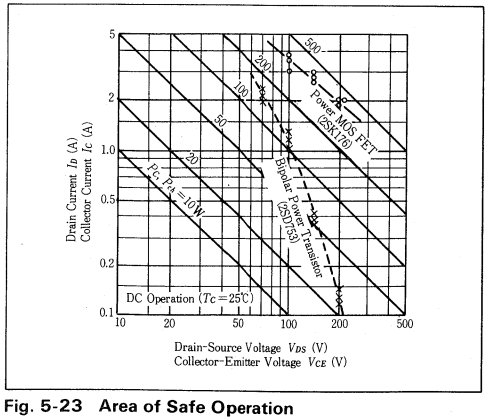


Fig. 5-23 Area of Safe Operation

We would like to show an example of ASO design as follows.

ASO design concepts of a power MOS FET are all thermal problems. (Surge may be considered as a thermal problem after all, but in this case, we will consider P_{ch} in a general sense of the term.

(1) Condition $T_j \leqq T_{jmax}$ should be satisfied.
(2) Both DC ASO curve and Pulse ASO curve are the lines on which P_{ch} is constant.
(3) Pulse ASO is given by calculation of transient thermal resistance.
(4) Temperature derating is "one" at T_C = 25 °C, and is "zero" at $T_C = T_{jmax}$.

<<example>>

In 2SK260Ⓗ (P_{ch}=125W, T_{jmax}=150 °C), is the following application example within the ASO:

T_C (the case temperature) =55 °C
V_{DS}=200V
I_D=1A
PW (pulse width)=2ms
T(Period)=10ms

Answer

(1) Find the value of transient thermal resistance at the point of PW=2ms, Duty=PW/T=0.2 in Fig. 5-24. γ(t)=0.44
(2) $\theta_{j\text{-}c}$ of 2SK260Ⓗ is found from the maximum rating; $\theta_{j\text{-}c}$=(150−25)/125=1.0 (°C/W), then the transient thermal resistance is; $\theta_{j\text{-}c(t)} = \theta_{j\text{-}c} \cdot \gamma(t)$=0.44(°C/W).
(3) The junction temperature (T_j) = $\theta_{j\text{-}c(t)} \cdot P_{ch} + T_C$=0.44×200+55=143(°C). This meets the condition of $T_j \leqq T_{jmax}$, and concludes that the above application example is within ASO.

Fig. 5-25 shows the ASO of 2SK260Ⓗ, based on the graph in Fig. 5-24.

The actual breakdown points are shown by (x, and they are outside the transient ASO. This means that actually the device will be destroyed at approximately 300 °C, not at the point of $T_j = T_{jmax}$.

5.5.2 Reverse Bias ASO

For power switching applications, such as switching regulators, the load of the switching device is usually inductive. Therefore, not only the forward bias ASO, as described in the preceding section, but also the reverse bias ASO should be considered. Generally, in a switching power supply, the emitter-base junction is reverse biased to reduce t_{stg} and t_f. In this case, the larger the current becomes, the smaller t_{stg} and t_f will be. And, according to it, the reverse bias ASO will be narrower, which

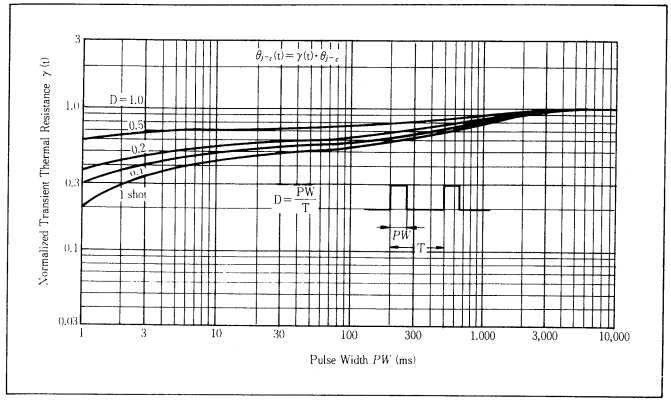


Fig. 5-24 Transient Thermal Resistance (TO-3 Package)

means the operation area is more limited, as shown in Fig. 5-26. On the other hand, in a power MOS FET, it is possible to make t_{off} smaller by reverse bias of the gate, without narrowering the operation area. This gives flexibility in circuit design.

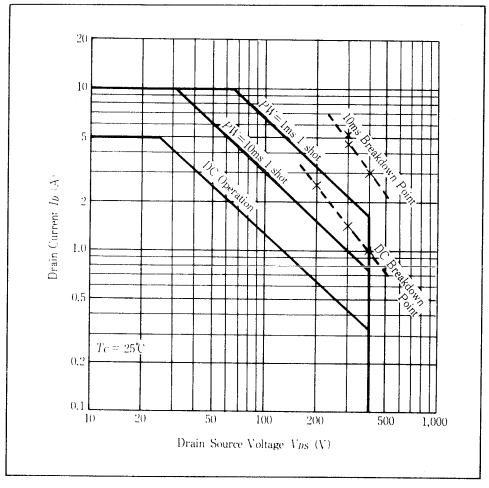


Fig. 5-25 2SK260Ⓗ ASO

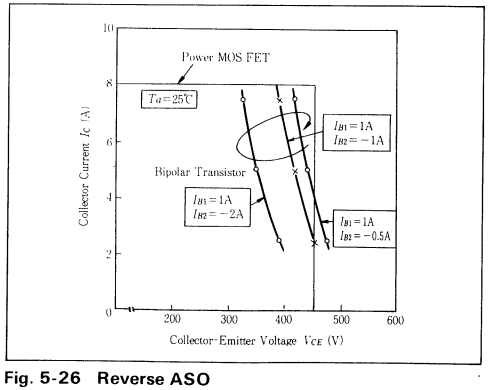


Fig. 5-26 Reverse ASO

5.6 Temperature Characteristics

Fig. 5-27 shows the transfer characteristics of power MOS FETs. In the high current area, the temperature coefficient is negative and current concentration does not occur. A wide area of safe operation is provided and destruc-

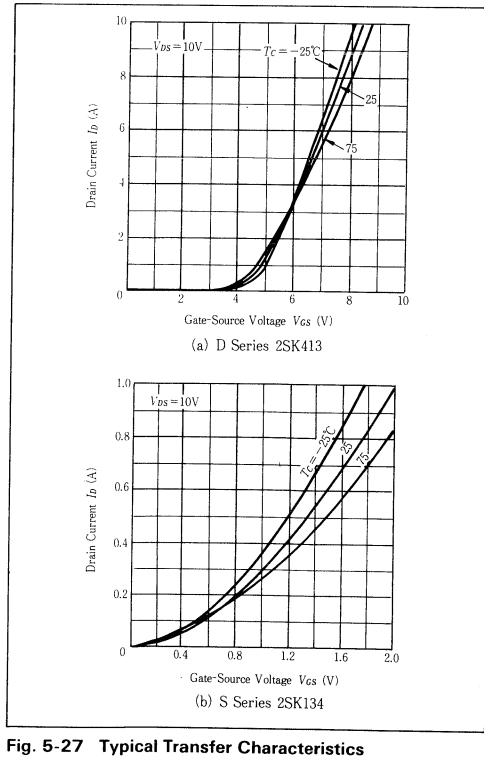


Fig. 5-27 Typical Transfer Characteristics

tion by thermal runaway is largely prevented.

Since the transfer characteristics of power MOS FETs are of the enhancement type, as in the case of bipolar transistors, power MOS FETs don't require a complex biasing circuit like depletion type FETs do.

The cross point at which the temperature coefficient becomes zero, is quite different between the D series device and the S series device, owing to their structures and processes. The cross point is 2 ~ 6A in D series device, and about 100mA, in S series device, although it depends on device type.

Therefore, by setting the idling current about 100mA, the S series MOS FET, when applied to a class-B push-pull audio power amplifier, can dispense with a current temperature compensation circuit, which is required in bipolar transistor circuits.

5.7 Source-Drain Diode Characteristics

In both D series and S series Power MOS FETs, as shown in Fig. 5-28 and Fig. 5-29, a diode exists parasitically, between source and drain.

The forward current and the breakdown voltage ratings of this diode have the same characteristics as those of the power MOS FET.

Fig. 5-30 shows the V_F-I_F characteristics of this diode, and Fig. 5-31, the waveform of the backward recovery time (t_{rr}). Also we would like to show the t_{rr}'s on a line scale, comparing the Fast Recovery Diode with some MOS FET's.

As is obvious from it, this diode has excellent characteristics, much the same as a typical diode. Moreover, when this diode is used in a bridge circuit, PWM amplifier output stage, etc, it can dispense with the external commutating diode, resulting in a reduction of the number of components.

If a channel is produced by making V_{GS} positive, the current flows equally in both directions. When the current is low, V_F is given by $I_F \times R_{on}$. The V_F of this diode is smaller than that of a typical diode. Therefore, in some cases, this diode is better than a typical one.

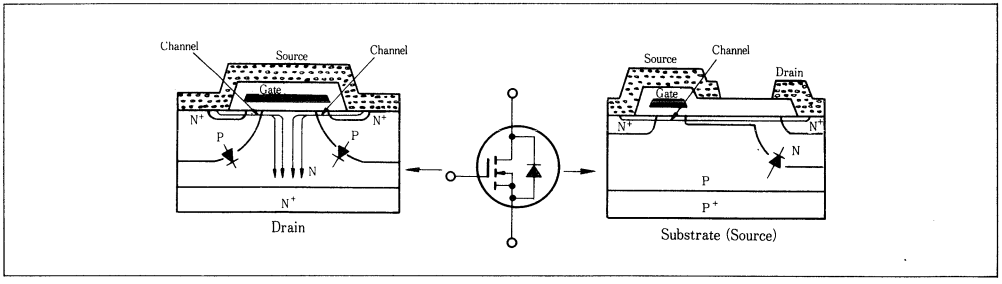


Fig. 5-28 Structure of D Series (Vertical type) (N channel)

Fig. 5-29 Structure of S Series (Lateral type) (N channel)

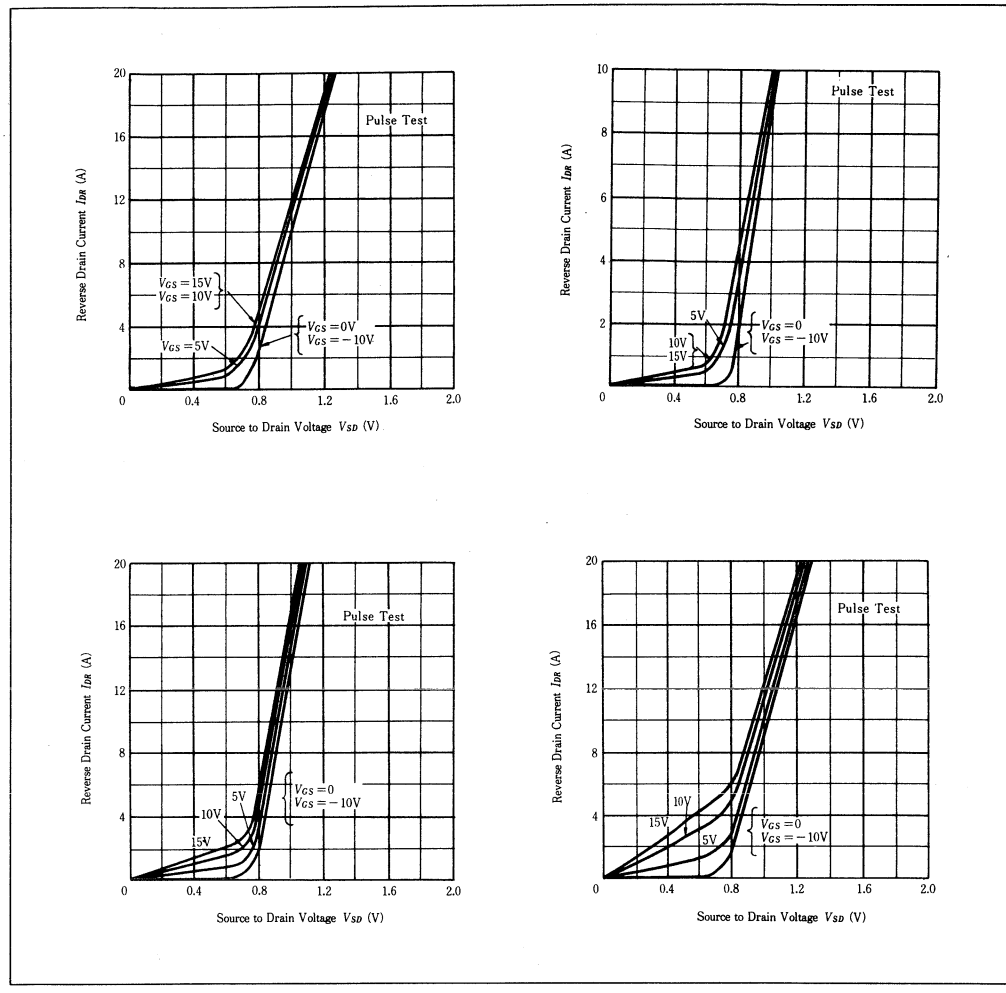
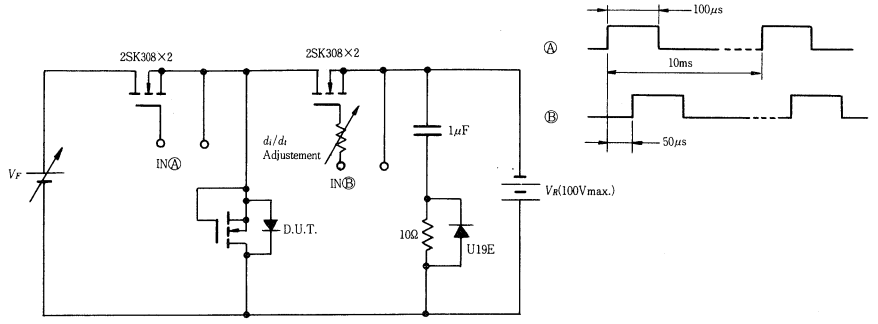
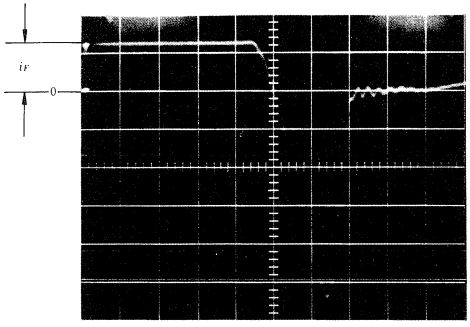


Fig. 5-30 V_F-I_F Characteristics

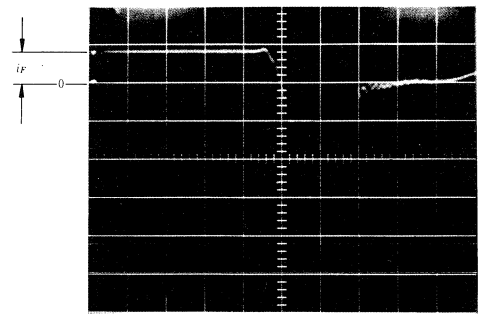


Measuring Circuit

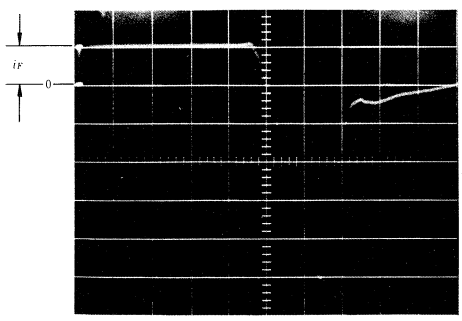
Scale I : 5A/DIV
t : 0.2μs/DIV



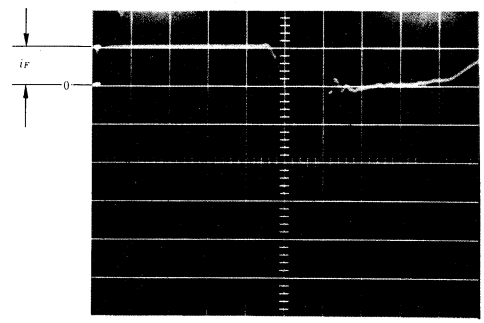
2SK313, 2SK350
(i_F=6A, di/dt=100A/μs)



2SK299, 2SK320
(i_F=4A, di/dt=100A/μs)



2SK401, 2SK412
(i_F=5A, di/dt=100A/μs)



2SK308, 2SK383
(i_F=5A, di/dt=100A/μs)

Fig. 5-31 t_{rr} Waveform of the Built-in Diode

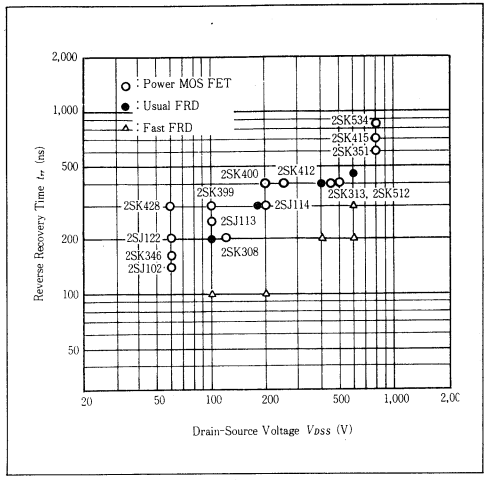


Fig. 5-32 Comparison to the built-in diode and the FRD t_{rr}

5.7.1 Precautions in Handling the Built-in Diode

An built-in diode of the power MOS FET is used as a commutating diode in a motor control circuit. In this case, if the reverse voltage is charged immediately after a high current is supplied to the diode, it may be destroyed depending on the circuit and the operating conditions.

Fig. 5-33 and 5-34 show a basic motor control circuit and the waveform of the motor control operation. These waveforms are at Q_2 and Q_3 off and Q_1 and Q_4 on. Q_4 is continuously on when Q_1 is chopping.

Gate drive signal is put into G_1, then Q_1 is switched on and i_{D1} flows. When Q_1 current i_{D1} is switched off, forward current, i_F flows through the built-in diode of Q_2 by the energy accumulated at the motor inductance. If Q_1 is switched on in this condition, Q_2 is into on-state under the influence of reverse recovery time, t_{rr} of built-in diode on Q_2, and high level of reverse current (recovery current), i_{Dr} flows.

This excess recovery current may destroy the diode at a point in the shaded area in the figure, which indicates the period in which the built-in diode voltage recovers. Therefore, restricting the recovery current i_{Dr} is an effective method to prevent diode destruction. Table 5-2 shows the detailed circuit countermeasures.

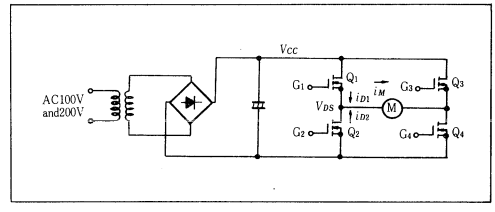


Fig. 5-33 Typical Motor Control Circuit

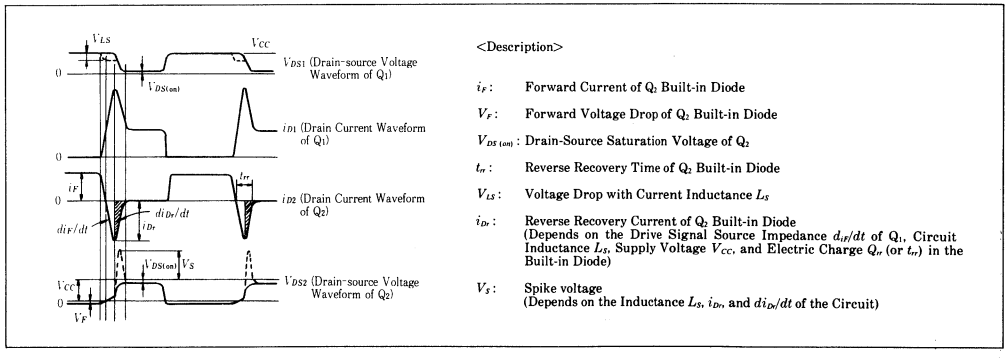
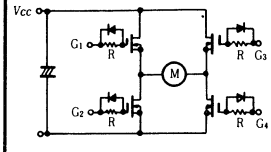
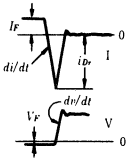
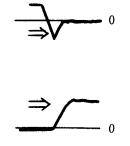
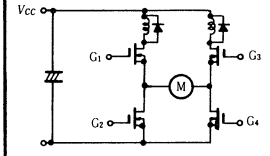
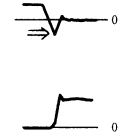
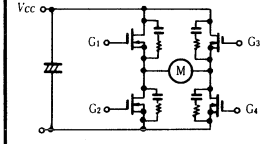
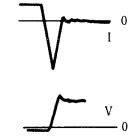
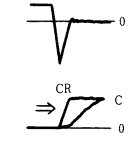
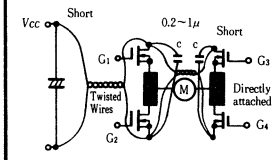
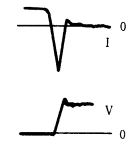
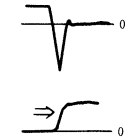
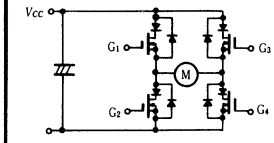
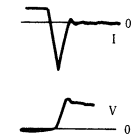
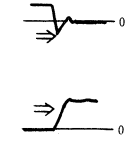


Fig. 5-34 Waveform of the Motor Control Operation

Table 5-2 Circuit Countermeasures against Built-in diode Destruction

Classification	Countermeasures	Circuit	Waveforms of the built-in diode		Circuit constants, etc.
			Before improvement	After improvement	
①	Delay the turn-on time, by inserting a resistor and diode which are connected in parallel into the gate of the Power MOS FET. This controls di/dt and dv/dt of the built-in diode to restrict the recovery current (in this case, the turn-off time does not have to be delayed).				R=330Ω~820Ω (di/dt=20~50A/μs)
②	Insert an L and diode connected in parallel into the drain of the Power MOS FET. This controls di/dt to restrict the recovery current i_{Dr}.				L=2μH~20μH
③	Insert a C or CR snubber between the drain and source of the Power MOS FET to restrict dv/dt and voltage spike of the built-in diode.				R=10~47Ω C=0.01μF~0.1μF Wiring of the snubber be as short as possible.
④	Wires between +, − terminals of the power supply line and the drain/source of each arm (in the case of N/N) should be twisted. C are also connected. By directly attaching wires to the upper and lower arms and minimizing stray inductance, the voltage spike and dv/dt are restricted.				Should be done together with countermeasures ① to ③.
⑤	Connect the fast diode to the external of the Power MOS FET not to flow the current in the built-in diode.				

5.8 Design of High Breakdown Voltage Application (Series Operation)

(1) Totem pole connection

Fig. 5-35 shows a basic "totem pole" circuit, in which power MOS FETs are connected in series. This circuit has been used extensively as a saturated logic circuit, the basic circuitry for TTL IC. Operation of this circuit will be explained.

When no bias is applied to Q_1, Q_1 is cut off because power MOS FETs have enhancement type transfer characteristics, thus the following relationships hold;

$$V_{G1} = 0,\ I_D = 0$$

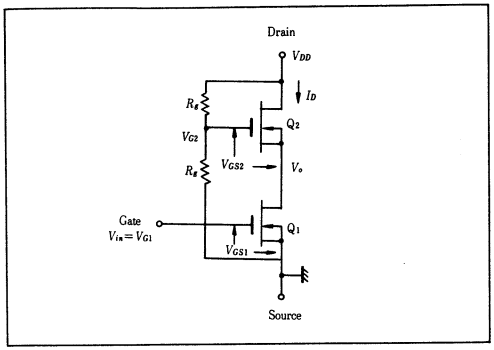


Fig. 5-35 Basic Totem Pole Circuit

$$V_{G2} = \tfrac{1}{2}V_{DD}\left(\because V_{G2} = V_{DD}\cdot\frac{R_g}{R_g+R_g}\right)$$

$$V_O = V_{G2} - V_{GS2}$$
$$= \tfrac{1}{2}V_{DD} - V_{th2}$$

where V_{th2} is the threshold voltage of Q_2. Generally, $V_{th2} << V_{DD}$. Therefore $V_O \simeq \frac{1}{2} V_{DD}$. And the voltage applied to Q_1 and Q_2 will be about $\frac{1}{2} V_{DD}$.

Next, let us consider a transient state. When the gate bias of Q_1 is increased gradually from zero, Q_1 will become conductive and so will Q_2 at the same time. If load resistance Z_L is inserted between V_{DD} and drain of Q_2, drain voltage will be $V_D = V_{DD} - Z_L \cdot I_D$ and V_O ($=\frac{1}{2}V_D - V_{GS2}$) will gradually decrease.

If V_{DD} has a much larger value than V_{GS2} and Q_2 is driven up to the saturation region, then the characteristics of an equivalent MOS FET would be dependent on Q_1.

Generally, when devices are operated in series, voltage unbalance due to switching time difference presents a problem. This problem is overcome in power MOS FETs because switching time can be made as short as several tens of nanoseconds.

Fig. 5-36 and 5-37 show breakdown and output characteristics where a single device is used. When this device is used in the circuit shown in Fig. 5-35, the breakdown and output characteristics would be as shown in Figs. 5-38 and 5-39. Breakdown voltage in Fig. 5-38 is twice as high as in Fig. 5-36. The disadvantage is that on-resistance is also doubled, as is obvious from Figs. 5-39 and 5-37. A method of improving on-resistance is described in the following section.

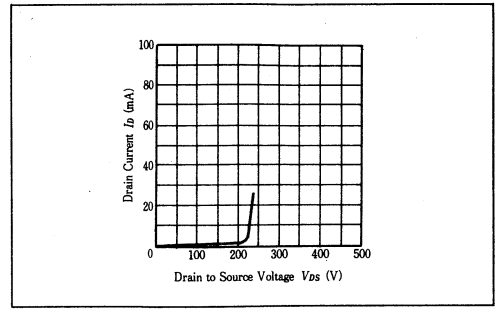


Fig. 5-36 Breakdown Characteristics (Single Device)

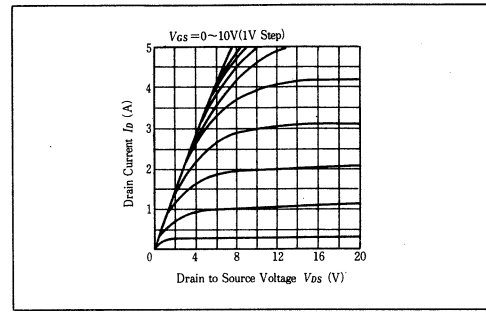


Fig. 5-37 Output Characteristics (Single Device)

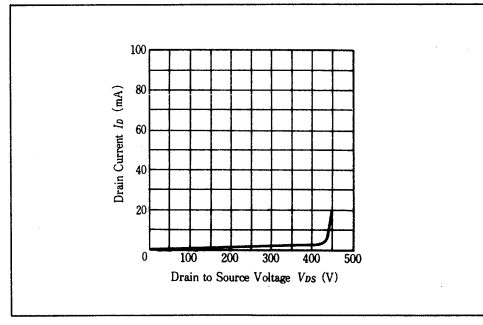


Fig. 5-38 Breakdown Characteristics

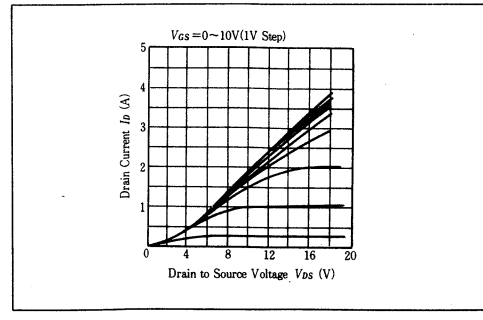
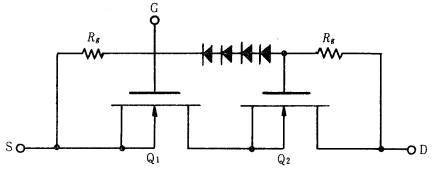


Fig. 5-39 Output Characteristics

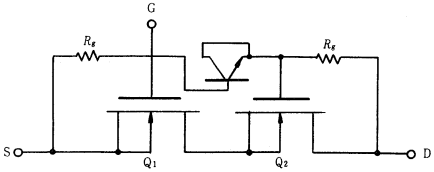
(2) How to reduce on-resistance in basic circuit

On-resistance (or saturation voltage) can be reduced by performing level shift of the Q_2 gate potential in the positive direction. This can be accomplished, for instance, by the methods shown in Fig. 5-40. Fig. 5-41 shows the output characteristics for a case where the gate is level-shifted to the positive side. (14V is the maximum allowable gate-to-source voltage.)

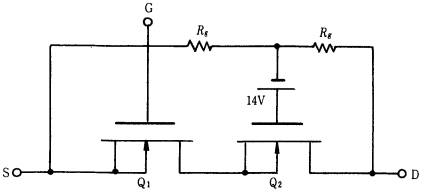
In the circuit shown in Fig. 5-40, as in the basic circuit, the equivalent drain to source breakdown voltage is twice as high as when a single device is used.



(A) Level Shift by Using of Diode



(B) Level Shift by Using of Breakdown Voltage in External Transistor



(C) Level Shift by Using of External Power Supply

Fig. 5-40 How to Reduce ON-Resistance

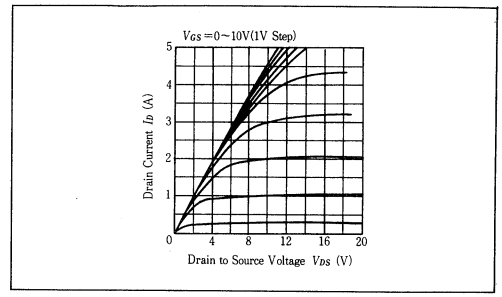


Fig. 5-41 Output Characteristics ((C) Circuit)

(3) Improvement of high frequency characteristics in totem pole connection

When the circuit shown in Fig. 5-35 is modified for a source follower, becasue of the different operation of Q_1 and Q_2, a phase differential occurs under the influence of the power MOS FET input capacitance (about 500 pF for 2SK134, 600 pF for 2SJ49, f=1MHz). As a

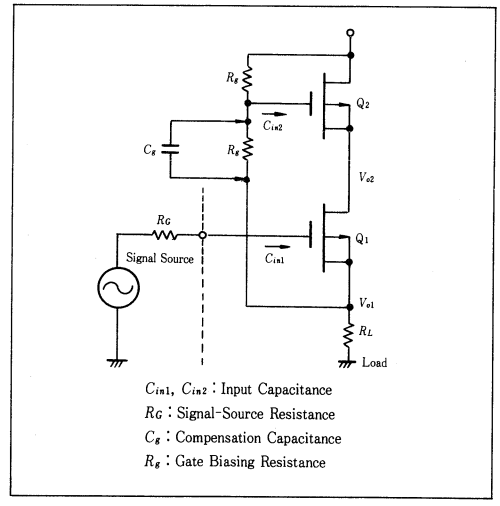


Fig. 5-42 Improved Totem Pole Circuit

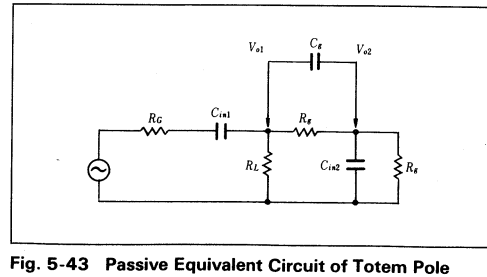


Fig. 5-43 Passive Equivalent Circuit of Totem Pole

result, characteristics worsen, as high frequency gain drops and phase shift increases.

This is expressed in Fig. 5-42. The equivalent circuit with passive devices alone is represented in Fig. 5-43.

It has been verified experimentally that the phase differential of V_{O1} and V_{O2} can be eliminated and driving in the same phase can be achieved by equalizing C_g with C_{in2} and that phase shift as 100 kHz can be limited within −90 degrees.

5.9 Analysis of Oscillation in Source Follower Circuits

<Reference>

There have been many works on analysis of oscillation in source follower circuits. The most general analysis for source follower circuits is about the case in which the real part of the input impedance is negative and the imaginary part is ZERO. An example is described as followers. The sumplified equivalent circuit of source follower is shown in Fig. 5-44.

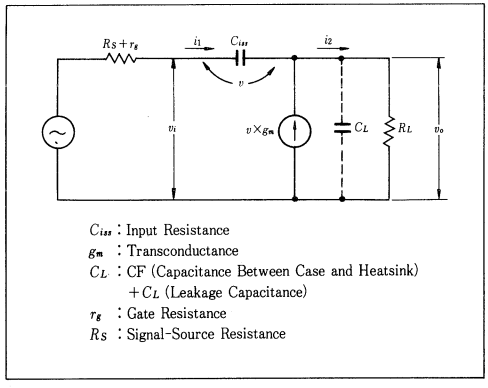


Fig. 5-44 Equivalent Circuit of Source Follower Circuit

The input impedance Z_{in} can be obtained as follows;

$$Z_{in}=\frac{v_i}{i_1}=\frac{1}{j\omega C_{iss}}+R_L\left(1+\frac{g_m}{j\omega C_{iss}}\right) \quad \ldots\ (1)$$

In the case of load consisting of paralleled resistor and capacitor Substitute $\frac{R_L}{1+j\omega C_L R_L}$ instead of R_L in equation (1).

$$Z_{in}=\frac{1}{j\omega C_{iss}}-\frac{j\omega C_L R_L{}^2}{1+\omega^2 C_L{}^2 R_L{}^2}-\frac{j\omega g_m R_L}{(1+\omega^2 C_L{}^2 R_L{}^2)\omega^2 C_{iss}}+\frac{R_L}{1+\omega^2 C_L{}^2 R_L{}^2}-\frac{\omega^2 C_L R_L{}^2 g_m}{(1+\omega^2 C_L{}^2 R_L{}^2)\omega^2 C_{iss}} \quad \ldots\ (2)$$

The condition for negative resistance is;

$$R_s+r_g+\frac{R_L}{1+\omega^2 C_L{}^2 R_L{}^2}-\frac{C_L R_L{}^2 g_m}{(1+\omega^2 C_L{}^2 R_L{}^2)C_{iss}}<0 \quad \ldots\ (3)$$

moreover, approximately,

$$R_s+r_g+R_L-\frac{C_L R_L{}^2 g_m}{C_{iss}}<0 \quad \ldots\ (4)$$

Therefore, to prevent oscillation, external gate resistor R_G should be inserted. Then the following equation can be obtained.

$$R_G+R_s+r_g+R_L-\frac{C_L R_L{}^2 g_m}{C_{iss}}\geqq 0$$

However, the insertion of external R_G makes Power MOS FETs frequency response worse. Therefore, when selecting R_G, a compromise between stability against oscillation and amplifier's frequency response should be considered. Voltage gain vs. frequency vs. R_G is shown in Fig. 5-45.

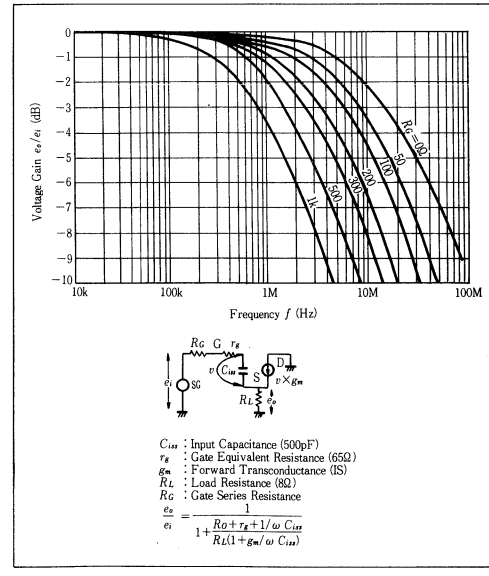


Fig. 5-45 Frequency Characteristics of Source Follower (Calculated Value)

6. DISCONTINUED POWER-MOS FET AND REPLACEMENT

6.1 MAINTENANCE PART

Type	Replacement
2SK196Ⓗ	2SK214

6.2 DISCONTINUATION PLAN

Type	Replacement
2SK535Ⓛ	2SK579Ⓛ
2SK535Ⓢ	2SK579Ⓢ
PM4550C	PM45502C

6.3 DISCONTINUED PRODUCTS

Type	Replacement	Type	Replacement
2SJ47	2SJ48	2SK226	2SK1057
2SJ50Ⓗ	2SJ50	2SK227	2SK1058
2SJ77Ⓚ	2SJ77	2SK261	2SK213
2SJ79Ⓚ	2SJ79	2SK262	2SK213
2SJ81	2SJ160	2SK263	2SK213
2SJ82	2SJ161	2SK264	2SK214
2SJ83	2SJ162	2SK286	—
2SJ85	2SJ76	2SK343	2SK413
2SJ86	2SJ76	2SK344	2SK414
2SJ87	2SJ76	2SK345	2SK346
2SJ88	2SJ77	2SK347Ⓛ	2SK579Ⓛ
2SJ96	—	2SK347Ⓢ	2SK579Ⓢ
2SJ99	2SJ118	2SK398	2SK399
2SJ100	2SJ119	2SK402	2SK641
2SJ101	2SJ102	2SK403	2SK641
2SJ112	2SJ113	2SK411	—
2SK132	2SK133	2SK441	2SK384
2SK135Ⓗ	2SK135	2SK561	2SK622
2SK214Ⓚ	2SK214	PM1201B	—
2SK216Ⓚ	2SK216	PM1220B	—
2SK225	2SK1056	PF0002	PF0007

6.4 COMPARISON LIST T03, T03P, HPAK S-Series

T03P 'S' SERIES
The HPAK has been continued 1986.

The T03P packeged S Series offer a more convenient, single sided mounting alternative to the established metal can T03. They also can be used in place of the now obsolete H PAK.

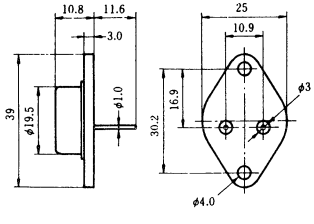
The T03P S Series use the same die that are used in T03 versions (and previously in the HPAK), so the electrical characteristics are unchanged. T03P will also fit directly into a PCB laid out for HPAK.

Table 8 T03P S Series Equivalents

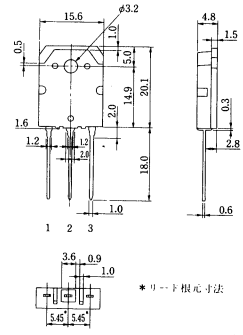
T03	T03P	VDSS (V)	ID/A	HPAK (obsolete)
2SK133	2SK1056	120	7	2SK225
2SK134	2SK1057	140	7	2SK226
2SK135	2SK1058	160	7	2SK227
2SJ48	2SJ160	120	−7	2SJ81
2SJ49	2SJ161	140	−7	2SJ82
2SJ50	2SJ162	160	−7	2SJ83

7. Standard Outline Dimensions

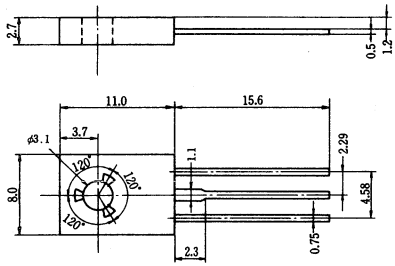
Various types of Hitachi transistor package is available to fulfill specific applications and performance. For guaranteed dimensions on individual package, refer the outline drawings for each device data sheet. Standard outline dimensions of Hitachi transistor packags are listed below to assist you in designing semiconductor-circuit. However, note that all dimensions listed below are for your, reference-not guaranteed.



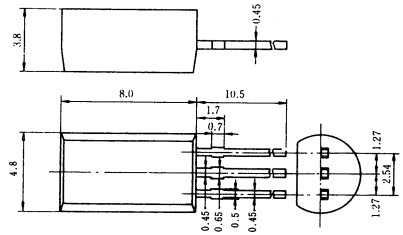
(JEDEC TO-3)



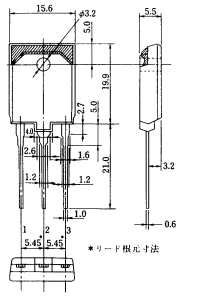
(TO-3P)



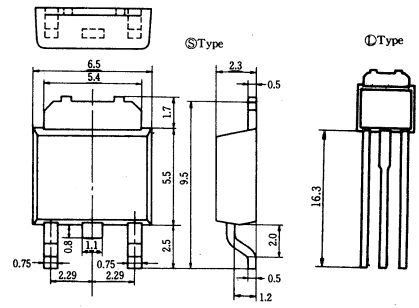
(JEDEC TO-126 MOD.)



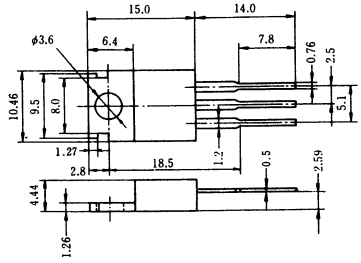
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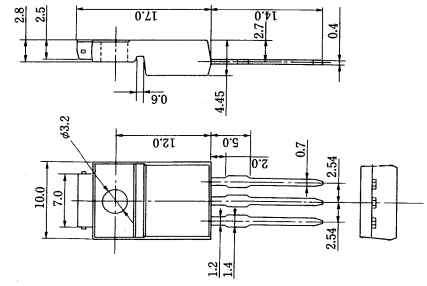
(TO-3P · FM)



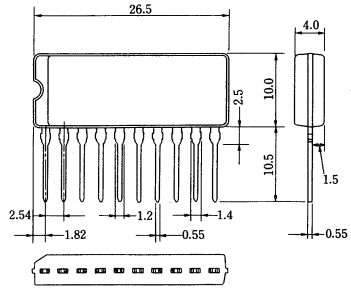
(DPAK)



(JEDEC TO-220AB)



(JEDEC TO-220FM)



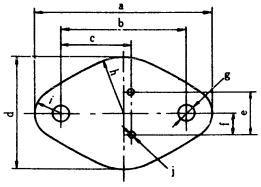
(SP-10)

8. INSULATING SPACERS AND WASHERS FOR POWER TRANSISTORS

The spacers and washers listed below are recommendable for insulating each power transistor package. Upon your request, the spacers and washers are available.

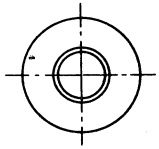
Outline	Accessories		Note
	Spacer	Washer	
TO-3	SK41C	YC10D	
		YC60S	
	SK40A	YC30C	High Voltage Use ($V_{CES} \geq 1{,}500V$)
TO-3P	SK022A	—	
	SK023A	—	High Voltage Use ($V_{CES} \geq 1{,}500V$)
TO-126 MOD.	SK18A	YZ28S	
TO202AA MOD.	SK18A	YC11C	
TO-220AB	SK16B	YC20A	
		YC40B	
		YC40D	
		YZ033S	We recommed to use with YC40D.

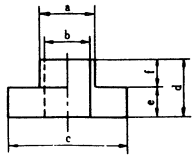
Spacer



	a	b	c	d	e	f	g	h	i	j	thickness
SK40A	43.0±0.2	30.2±0.1	16.9±0.1	29.0±0.2	10.9±0.1	5.5±0.1	φ3.1±0.1	14.5R	6.0R	$\phi 1.5^{+0.3}_{-0}$	0.075 ±0.025
SK41C	42.0±0.2	30.2±0.1	16.7±0.1	29.0±0.2	10.9±0.1	5.5±0.1	φ4.2±0.1	14.5R	6.0R	$\phi 1.5^{+0.3}_{-0}$	

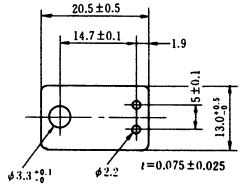
Washer



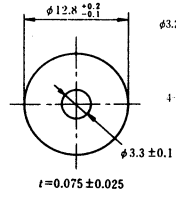


	a	b	c	d	e	f
YC10D	φ3.7±0.1	φ3.1±0.1	φ8.0±0.2	5.0±0.2	2.0±0.1	3.0±0.1
YC11C	φ3.7±0.1	φ3.1±0.1	φ8.0±0.2	4.0±0.2	2.0±0.1	2.0±0.1
YC20A	φ4.3±0.1	φ3.3±0.1	φ8.0±0.2	2.8±0.2	2.0±0.1	0.8±0.1
YC30C	φ6.0±0.1	φ3.1±0.1	φ16.0±0.2	3.7±0.2	2.0±0.1	1.7±0.1
YC40B	$\phi 3.45^{+0.05}_{-0.06}$	$\phi 3.03^{+0.08}_{-0.05}$	φ5.3±0.20	2.0±0.2	1.0±0.1	1.0±0.1
YC40D	φ3.45±0.08	$\phi 3.03^{+0.08}_{-0.05}$	φ5.3±0.2	3.2±0.2	1.0±0.1	2.2±0.1

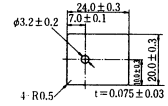
SK16B



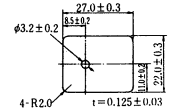
SK18A



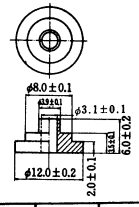
SK022A



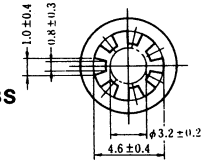
SK023A



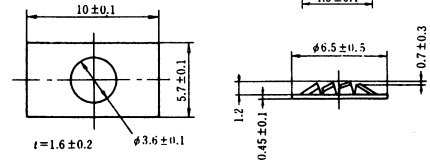
YC60S



YZ28S



YZ033S



(Dimensions in mm)

9. NOMENCLATURE OF HITACHI SEMICONDUCTOR DEVICES

1. Nomenclature of the Semiconductor Devices

The "Japanese Industrial Standards"(JIS-C-7012) prescribes nomenclature of transistors as follows:

2	S	A	537	A	Ⓗ	B
First item (digit)	Second item (letter)	Third item (letter)	Fourth item (digits)	Fifth item (letter)	Sixth item (letter)	Seventh item (letter)

The first item (digit) indicates the type of semiconductor devices.

(a) For the other semiconductor devices, the digit for the first item is indicated by n-1, n being the effective numbers of the electrodes of the semiconductors.

(b) As to the composite devices, their nomenclature is given according to the biggest effective number of the electrodes which are contained in them.

(Note): "Effective number of the electrodes" means the number of the electrodes indispensable for operation of the particular device, not the number of the electrodes which are actually drawn outside from it.

But the shield and getter terminals of the devices are excluded from the effective numbers.

The foregoing may be summarized as follows:

Type of semiconductor products	Effective number of the electrodes	Digit in the first item
Ordinary transistors; FET wite single gate	3	2
FET with the duai gates, etc.	4	3

The second item (letter "S") indicates that the product is of semiconductor device.

The third item (letter) indicates polarity and application of the semiconductor device. It is prescribed in the following manner.

the third item is prescribed as follows.

- A: High-frequency devices on which output electrodes negative voltage is impressed. } PNP-transistors
- B: Low-frequency devices on which output electrodes negative voltage is impressed. } PNP-transistors
- C: High-frequency devices on which output electrodes positive voltage is impressed. } NPN-transistors
- D: Low-frequency devices on which output electrodes positive voltage is impressd. } NPN-transistors
- J: P-channel field-effect transistors (FET)
- K: N-channel field-effect transistors (FET)

The fourth item (number) has the digits of 11 or more, which are given according to the sequence of the registration with the "JIS."

The fifth item (letter) indicates a revision of the product originally named. To each revision, A, B, C, etc., is added.

The original product can be functionally replaced by its revised types, but not necessarily vice versa.

The above is a brief summary of the nomenclature laid down in JIS-C-7012.

Hitachi, Ltd., uses further affixes of its own which are the sixth and seventh item, (letter in bracket).

The sixth item (letter)

Ⓗ means "specially manufactured for communications industry."

Ⓚ means "specially manufactured for communications industry" (plastic molded types)

The seventh item (letter)

In case the item named needs further classification according to its own electrical characteristics, an appendix such as A, B, C etc. is put at the end of its name.

The nomenclature of the devices given in the following examples has the meanings as they are shown.

2SA537AⒽB : A PNP-transistor for high-frequency use, a revision of 2SA537Ⓗ; specially manufactured for communication industry.

(Ⓗ stands for high reliability.): sub-classified by h_{FE} into its B group, whose h_{FE} value ranges from 60 to 120.

For the convenience of the users of this data book, the technical symbols such as for maximum ratings, electrical characteristics are shown below.

10. TECHNICAL SYMBOLS AND ITS DEFINITIONS

For the convenience of the users of this Data Book, the technical symbols such as for maximum ratings, electrical characteristics are shown below.

1. General Principles for the Symbols

In order to show DC characteristics, capital letter is used; and small letter is used to show AC characteristics and small-signal characteristics. But attention should be given to some exceptions. There are some symbols of capital letter which indicate other than DC characteristics; examples are such as: power output(P_{out}), power gain(PG), noise figure(NF), and storage quality factor (Q_s).

The use of suffixes is as described in the following examples. There are some exceptions and conventional usages which depart from the principles.

Examples:

Symbol	First item	Second item	Third item	
T	$_{opr}$			The first item gives a supplementary explanation of the contents of the symbol.
P	$_{out}$			
I	$_{F}$			The first item indicates the direction of transmission, and an example of a four-terminal parameter.
h	$_{i}$	$_{e}$		
I	$_{C}$	$_{B}$	$_{X}$	The third item indicates the state of the third electrode.
V	$_{C}$	$_{E}$	$_{O}$	
V	$_{C}$	$_{E}$	$_{(sat)}$	The third item indicates the state of the device.
V	$_{G1}$	$_{S}$	$_{(off)}$	

The first item is divided up into the following three main categories.

(a) To provide a supplementary explanation of the contents indicated by the symbol. (In this case, the first item sometimes has three letters or more.)

(b) To indicate the electrode in question when the symbol refers to current or voltage.

(c) To indicate the direction of transmission, and in case four-terminal parameters are referred to.

I , i: Input parameter.

R, r: Reverse transmission parameter.

F, f: Forward transmission parameter.

O , o: Output parameter.

The second item indicates the grounding electrode (the reference electrode of the voltage).

The third item indicates the electrical state of the electrode (the third electrode) other than the first and the second item of the device itself.

The third item has the following meanings:

S: the third electrode is short-circuited to the grounding electrode.

R: the prescribed resistance is to be connected between third electrode and the grounding electrode.

O: the third electrode is left open.

X: the third electrode is in a state than other that of S, R, or O as given above. In this Handbook, this is always indicated with reverse bias,

($_{sat}$): indicates that the device is in the state of saturation as to the electrical characteristics.

($_{off}$): indicates that the device is in the cut-off state as to the electrical characteristics.

2. Symbols for the Maximum Ratings

In semiconductor products, the maximum ratings are usually defined in terms of the "absolute maximum ratings." The strictest care must be taken to assure that the values given in the maximum-rating tables for each type are never surpassed, even for an instant. Even momentary excess of these maximum ratings set leads to immediate deterioration or destruction of the device concerned. Even if the device should be able to operate the excess, it must be assumed that its life has been shortened extremely. In designing electronic circuits with semiconductor devices, the first step to circuit-design is to make sure that their maximum ratings should never be exceeded, no matter what electrical fluctuations due to the external conditions may occur.

In many cases these maximum ratings are closely interrelated, and careful attention must be paid to the fact that they are not compatible at the same time. For example, let us take it that current and voltage applied to a transistor are both within the range of their maximum ratings. In this case, the power consumption of the transistor will be given by the product of them. It must be within the range of the permissible collector dissipation of the given type. Furthermore, this permissible collector dissipation will decrease if the service temperature is higher; the service range will be reduced relatively.

The following table gives brief definitions of the various items of the maximum ratings prescribed for the different devices given in this Data Book.

Table 1. Maximum ratings of transistors

Item	Definitions of the maximum ratings
V_{CBO}	Maximum value (base grounding) of voltage which can be applied between the collector and base when the emitter is open.
V_{CBX}	Maximum value (base grounding) of voltage which can be applied between the collector and the base when the given bias has been applied between the emitter and the base (reverse bias to be used in this Handbook).
V_{CEX}	Maximum value (emitter grounding) of voltage which can be applied between the collector and emitter when the prescribed bias has been applied between the base and the emitter (this is always reverse bias in this Handbook).
V_{CES}	Maximum value (emitter grounding) of voltage which can be applied between the collector and emitter when the base and emitter have been D.C. short-circuited.
V_{CER}	Maximum value (emitter grounding) of voltage which can be applied between the collector and emitter when the prescribed D.C. resistance has been connected between the base and emitter.
V_{CEO}	Maximum value (emitter grounding) of voltage which can be applied between the collector and emitter when the base is open.
V_{EBO}	Maximum value (base grounding) of voltage which can be applied between the emitter and base when the collector is open.
$i_{C(peak)}$	Peak value of the A.C. collector current which can be applied within range wherein the mean current will not exceed the following I_C.
$I_{C(surge)}$	Maximum value of the surge current which can applied at the prescribed pulse width or the test circuit.
I_C	Maximum value of D.C. current which can be continuously applied to the collector within the permissible range of the collector dissipation of the mean value of the A.C. current.
I_E	Same definition as that of I_C with respect to the emitter current.
I_B	Same definition as that of I_C with respect to the base current.
P_C	Maximum value of the collector dissipation which can be consumed continuously by the transistor under the prescribed heat radiation conditions.
T_j	Upper limit value of the junction temperature which must not be surpassed by $(T_a + \theta_{ja} \cdot P_{diss})$, the sum of the ambient temperature during operation (T_a) and the temperature rise ($\theta_{ja} \cdot P_{diss}$) due to the inner loss within the transistor itself (P_{diss}).
T_{stg}	Upper and lower limit values of the ambient temperature which must not be surpassed when the transistor out of operation is kept in storage.

Table 2. Maximum ratings of field-effect transistors (FET)

Item	Definitions of the maximum ratings
V_{DSX}	Maximum value of the voltage which can be applied between the drain and the source when the given bias is applied between the first gate and the source.
V_{DSS}	Maximum value of voltage which can be applied between the drain and the source when the gate and the source have been D.C. Short-circuited.
V_{GSS}	Maximum value of voltage which can be applied between the gate and the source when the drain and the source have been D.C. Short-circuited.
V_{GSX}	Maximum value of the voltage which can be applied between the gate and source when the given bias is applied between the drain and the source.
$i_{D(peak)}$	Peak value of the AC drain current which can be applied within range wherein the mean current will not exceed the following I_D.
I_D	Maximum value of the D.C. current which can be applied continuously to the drain with the permissible range of the channel dissipation.
I_{DR}	Maximum value of the reverse D.C. current which can be applied continuously to the immanent diode in source to drain with the permissible range of the channel dissipation.
$i_{DR(peak)}$	Peak value of the reverse AC drain current which can be applied with in range wherein the mean current will not exceed the following I_{DR}
I_G	Maximum value of the D.C. current which can be applied continuously to the gate within the permissible range of the channel dissipation.
P_{ch}	Same as P_C for transistors.
T_{ch}	Same as T_j for transistors.
T_{stg}	Same as transistors.

3. Symbols for the Electrical Characteristics

As for the electrical characteristics of the various devices described in this Data Book, the limit values as well as the standard values are given whenever possible for all items which will be necessary in circuit design. These characteristics may be divided up into the following five categories.

(a) Withstand voltage characteristics

These are items laid down for the purpose of guaranteeing the maximum-rated voltage of the given product. The withstand voltage indicates the voltage between the two specified electrodes when the given current has been applied to the prescribed electrode (in transistors and FET, the given bias conditions are to be imposed upon the other electrode).

In most cases, testing is performed by means of

a curve tracer, and adjustments are made so that the peak value of the A.C. (50 or 60 Hz) half-wave shall come to the value of the prescribed current. Care must be taken never to test these items by applying D.C. current; there shall be danger of thermal destruction of the device.

(b) Cut-off current characteristics

This refers to the D.C. current flowing into the prescribed electrode when the given voltage has been applied between the two prescribed electrodes (in transistors and FET, the given bias conditions are imposed upon the other electrode).

Of all the characteristics of semiconductor products, this value is the most sensitive to temperature, and has a temperature coefficient of approximately 10 (%/℃).

Therefore, when the device is to be operated at a higher ambient temperature, its operating range must be narrower and care must be taken of possible thermal runaway.

(c) D.C. characteristics

These characteristics give the bias point(h_{FE}, V_{CE}), the gain at the enlarged-amplitude operation(h_{FE}), the driving conditions ($V_{BE(sat)}$), as well as the width of the operating-region ($V_{CE(sat)}$) of the device in question. They also have an important significance when the device is applied for switching use.

(d) Small signal characteristics (Low-frequency, High-frequency)

These characteristics give the input-output and transmission characteristics of the devices to be used in small signal (low-frequency or high-frequency) operations in the recommended applications. For the device to be used in low frequency, the characteristics are indicated at 270 (Hz). For the devices to be used in high-frequency, their characteristics are indicated with the frequency in which they are generally expected to operate.

(e) Operating characteristics

These characteristics are given under the standard operating conditions in which the devices are applied. The approximate performance characteristics in the operating conditions may be estimated from the characteristics in the preceding four sections. But the operating characteristics indicate the actual operating characteristics at the recommended operating point.

The measuring conditions and the definitions of these items are given in Table 3 and the following table.

Table 3 Electrical characteristics of FET

Category	Symbol	Prescribed measuring conditions, contents of definitions
(a)	$V_{(BR)DSS}$	Determines I_D. It is assumed that $V_{GS}=0$
	$V_{(BR)DSX}$	Determines I_D and V_{GS}.
	$V_{(BR)GSS}$	Determines I_G. It is assumed that $V_{DS}=0$
(b)	I_{GSS}	Determines V_{GS}. It is assumed that $V_{DS}=0$
(c)	I_{DSS}	Determines V_{DS}. It is assumed that $V_{GS}=0$
	I_{DSX}	Determines V_{DS}, V_{GS}.
	$R_{DS(on)}$	Determines I_D, V_{GS}.
	$V_{DS(on)}$	Determines I_D, V_{GS}.
	V_{DF}	Determines I_F. It is assumed that $V_{GS}=0$
	$V_{GS(off)}$	Determines V_{DS} and I_D.
	R_{OFF}	Determines V_{DS} and V_{GS}.
(d)	V_n	Determines V_{DS}, I_D, R_g and f. (Noise voltage reffered to input.)
	NF	Determines V_{DS}, I_D, R_g and f.
	$\lvert y_{fs} \rvert$	Determines V_{DS} and f. It is assumed $I_D=I_{DSS}$.
	C_{iss}	Determines V_{DS} and f.
	C_{rss}	Determines V_{DS} and f.
	C_{oss}	Determines V_{DS}, V_{GS} and f.
(e)	$t_{d(on)}$	Determines V_{DD}, R_L, V_{GS} and I_D. Designate the measuring circuit.
	t_r	
	$t_{d(off)}$	
	t_f	
	t_{on}	$=t_{d(on)}+t_r$
	t_{off}	$=t_{d(off)}+t_f$

4. Indications of Units and Power

The units and power used in this Data Book with which to show the maximum ratings and the various characteristics are as follows.

(a) Indications of units (Note 1)

[Quantities]	[Symbols]	[Abbreviation]
Current	I, i	A
Voltage	V, v	V
Power	P	W
Charge	Q	C
Resistance	R, r	Ω
Capacitance	C	F
Inductance	L	H
Admittance	y	S
Conductance	g	S
Susceptance	b	S
Gain, attenuation	—	dB
Time	t	s
Frequency	f	Hz
Angle	(ϕ)	°
Temperature	T	℃
Length	(l)	mm
Efficiency	η	%

(b) Indications of power (Note 2)

[Power]	[Abbreviation]
10^{9}	G
10^{6}	M
10^{3}	k
10^{0}	—
10^{-3}	m
10^{-6}	μ
10^{-9}	n
10^{-12}	p
10^{-15}	f

Note 1: All of the units shown here are to be applied to the power product of 10^0. When indicating the power product in connection with time t (s) or frequency f (Hz), the following indications are to be used: t (μs), f (kHz), etc.

Note 2: Nowadays the power products of 10^9 to 10^{-15} is used for semiconductor products. But it does not follow that all of them are used for all other different quantities; 10^{-3} (m) and 10^{-9} (n) are not customarily used for capacitance.

DATA SHEETS

- S-SERIES
- D-SERIES
- D II-SERIES
- D III-SERIES
- POWER-MOS FET MODULES

NEW PRODUCTS

- D II-SERIES
- D III-SERIES
- POWER-MOS FET ARRAYS
- POWER-MOS FET MODULE

2SJ48,2SJ49,2SJ50

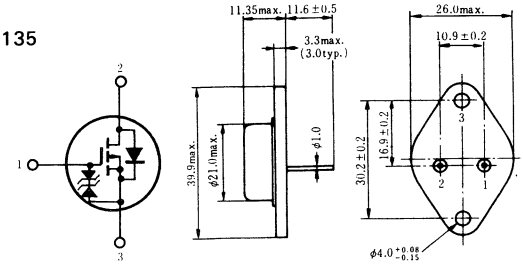
SILICON P-CHANNEL MOS FET

LOW FREQUENCY POWER AMPLIFIER

Complementary Pair with 2SK133, 2SK134, 2SK135

■ FEATURES

- High Power Gain.
- Excellent Frequency Response.
- High Speed Switching.
- Wide Area of Safe Operation.
- Enhancement-Mode.
- Good Complementary Characteristics.
- Equipped with Gate Protection Diodes.



1. Gate
2. Drain
3. Source (Case)

(JEDEC TO-3

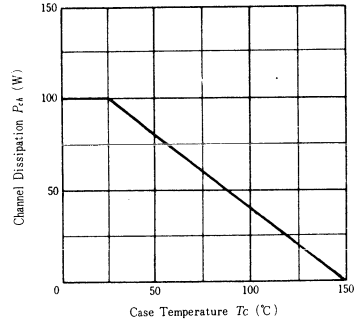
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating			Unit
		2SJ48	2SJ49	2SJ50	
Drain-Source Voltage	V_{DSX}	−120	−140	−160	V
Gate-Source Voltage	V_{GSS}	±14			V
Drain Current	I_D	−7			A
Body-Drain Diode Reverse Drain Current	I_{DR}	−7			A
Channel Dissipation	P_{ch}*	100			W
Channel Temperature	T_{ch}	150			°C
Storage Temperature	T_{stg}	−55 ~ +150			°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

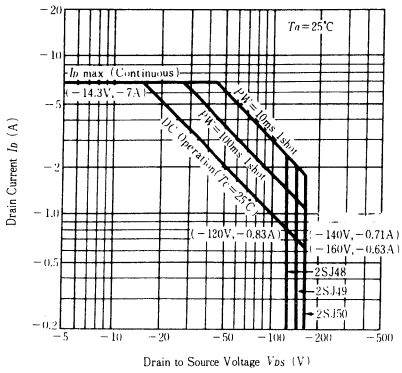


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

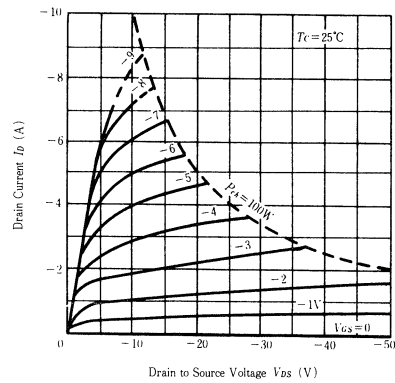
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SJ48	$V_{(BR)DSX}$	I_D=−10mA, V_{GS}=10V	−120	—	—	V
	2SJ49			−140	—	—	V
	2SJ50			−160	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±14	—	—	V
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=−100mA, V_{DS}=−10V	−0.15	—	−1.45	V
Drain-Source Saturation Voltage		$V_{DS(sat)}$	I_D=−7A, V_{GD}=0*	—	—	−12	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=−3A, V_{DS}=−10V*	0.7	1.0	1.4	S
Input Capacitance		C_{iss}	V_{GS}=5V, V_{DS}=−10V, f=1MHz	—	900	—	pF
Output Capacitance		C_{oss}		—	400	—	pF
Reverse Transfer Admittance		C_{rss}		—	40	—	pF
Turn-on Time		t_{on}	V_{DD}=−20V, I_D=−4A	—	230	—	ns
Turn-off Time		t_{off}		—	110	—	ns

*Pulse Test

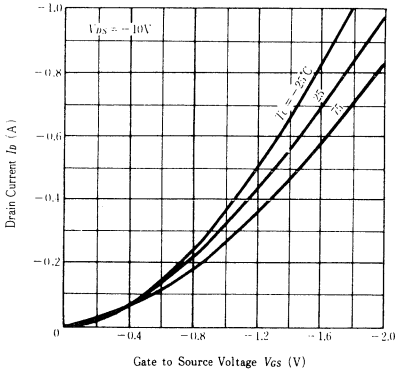
MAXIMUM SAFE OPERATION AREA



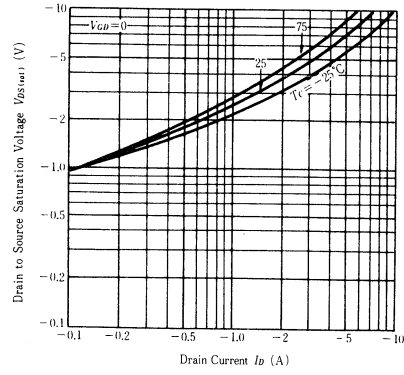
TYPICAL OUTPUT CHARACTERISTICS



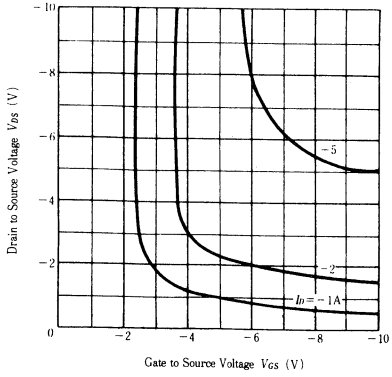
TYPICAL TRANSFER CHARACTERISTICS



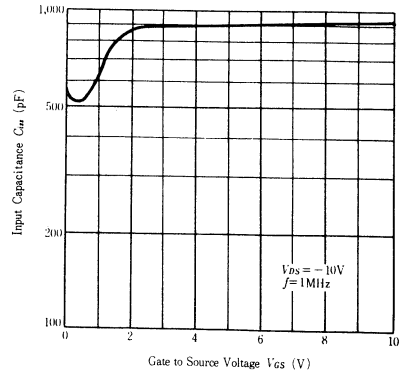
DRAIN TO SOURCE SATURATION VOLTAGE VS. DRAIN CURRENT



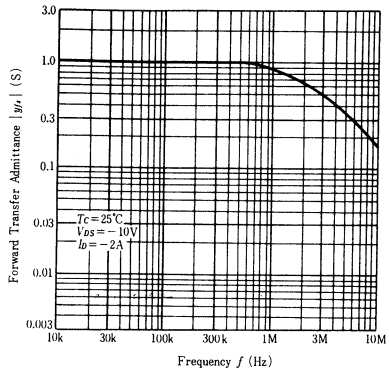
DRAIN TO SOURCE VOLTAGE VS. GATE TO SOURCE VOLTAGE



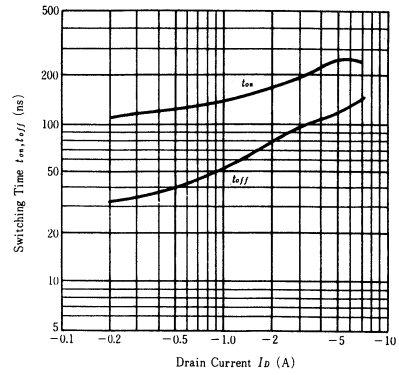
INPUT CAPACITANCE VS. GATE TO SOURCE VOLTAGE



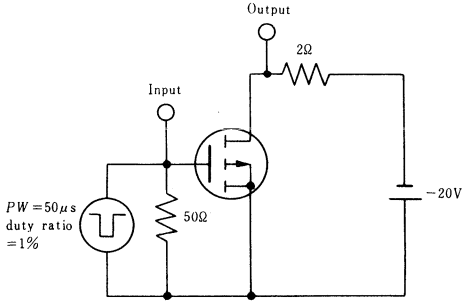
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



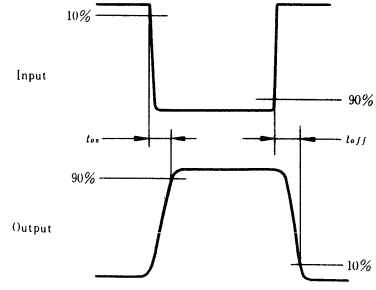
SWITCHING TIME VS. DRAIN CURRENT



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



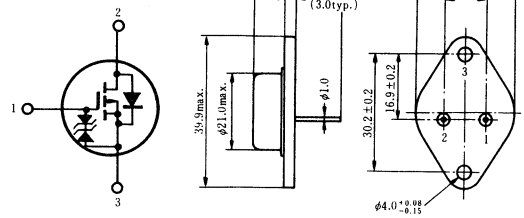
2SJ55, 2SJ56

SILICON P-CHANNEL MOS FET

LOW FREQUENCY POWER AMPLIFIER
Complementary Pair with 2SK175, 2SK176

■ FEATURES

- High Power Gain.
- Excellent Frequency Response.
- High Speed Switching.
- Wide Area of Safe Operation.
- Enhancement-Mode.
- Good Complementary Characteristics.
- Equipped with Gate Protection Diodes.



(JEDEC TO-3)

1. Gate
2. Drain
3. Source (Case)

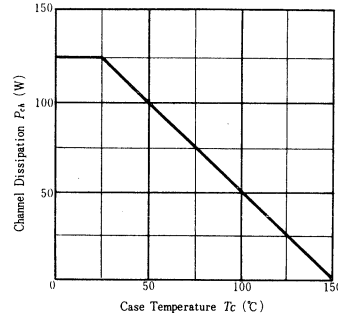
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SJ55	2SJ56	
Drain-Source Voltage	V_{DSX}	−180	−200	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	−8		A
Body-Drain Diode Reverse Drain Current	I_{DR}	−8		A
Channel Dissipation	P_{ch}*	125		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

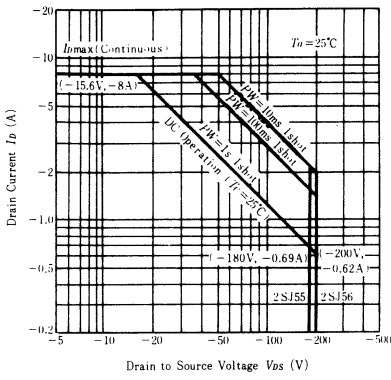


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

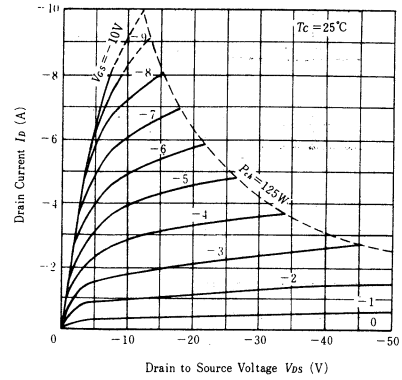
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SJ55	$V_{(BR)DSX}$	I_D=−10mA, V_{GS}=10V	−180	—	—	V
	2SJ56			−200	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=−100mA, V_{DS}=−10V	−0.15	—	−1.45	V
Drain-Source Saturation Voltage		$V_{DS(sat)}$	I_D=−8A, V_{GD}=0*	—	—	−12	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=−3A, V_{DS}=−10V*	0.7	1.0	1.4	S
Input Capacitance		C_{iss}	V_{GS}=5V, V_{DS}=−10V, f=1MHz	—	1200	—	pF
Output Capacitance		C_{oss}		—	700	—	pF
Reverse Transfer Capacitance		C_{rss}		—	60	—	pF
Turn-on Time		t_{on}	V_{DD}=−30V, I_D=−4A	—	320	—	ns
Turn-off Time		t_{off}		—	120	—	ns

*Pulse Test

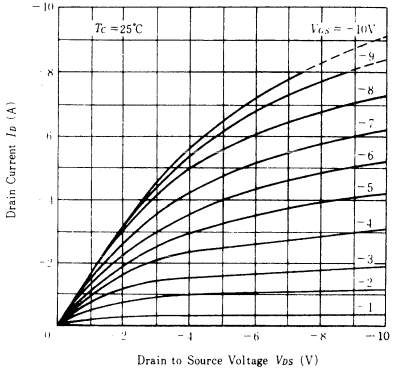
MAXIMUM SAFE OPERATION AREA



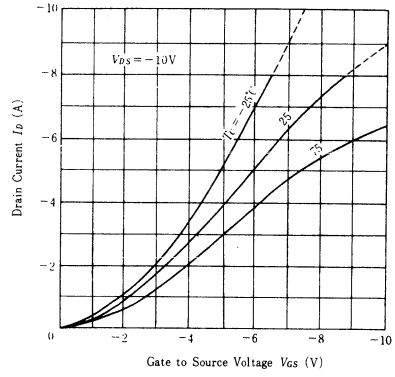
TYPICAL OUTPUT CHARACTERISTICS



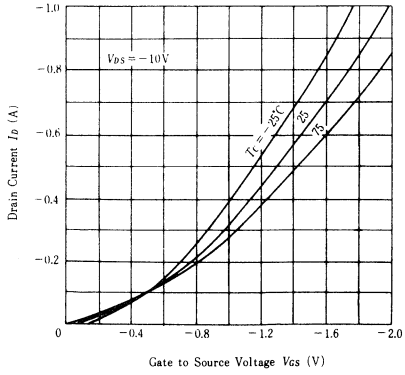
TYPICAL OUTPUT CHARACTERISTICS



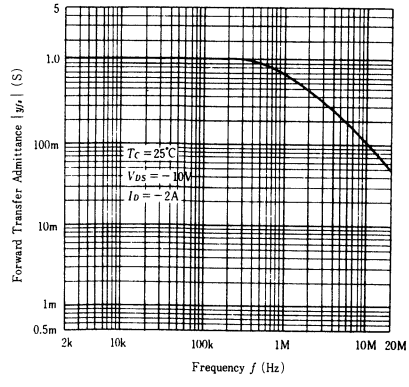
TYPICAL TRANSFER CHARACTERISTICS



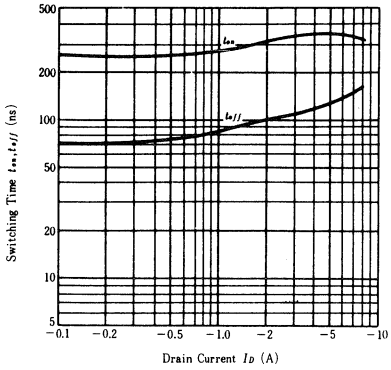
TYPICAL TRANSFER CHARACTERISTICS



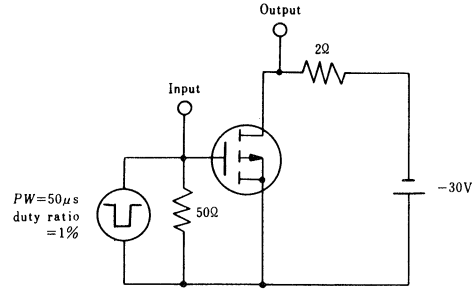
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



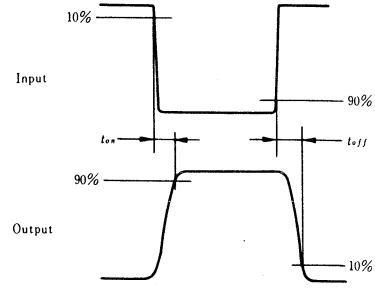
SWITCHING TIME VS. DRAIN CURRENT



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



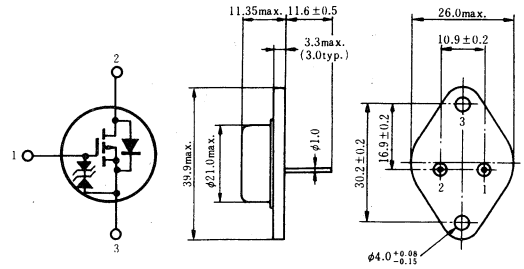
2SJ56H

SILICON P-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- High Speed Switching.
- High Cutoff Frequency. (f_c=1MHz)
- Enhancement-Mode.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2. Drain
3. Source (Case)

(JEDEC TO-3)

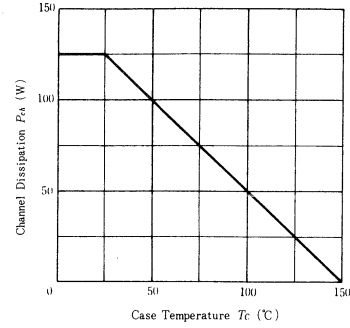
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	−200	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	−8	A
Body-Drain Diode Reverse Drain Current	I_{DR}	−8	A
Channel Dissipation	P_{ch}*	125	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

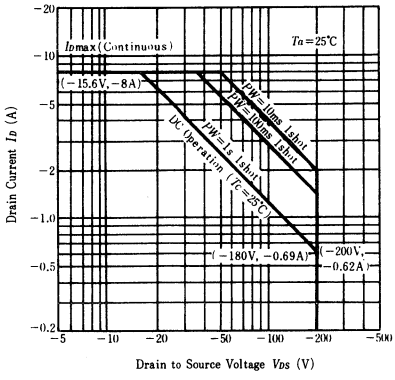


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

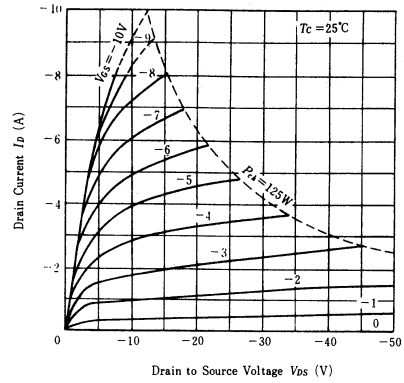
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−10mA, V_{GS}=0	−200	—	—	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=−160V, V_{GS}=0	—	—	−3.0	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=−100mA, V_{DS}=−10V	−0.55	—	−3.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=−4A, V_{GS}=−15V*	—	1.0	1.5	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=−4A, V_{GS}=−15V*	—	−4.0	−6.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=−3A, V_{DS}=−10V*	0.7	1.0	1.4	S
Input Capacitance	C_{iss}	V_{GS}=5V, V_{DS}=−10V, f=1MHz	—	1200	—	pF
Output Capacitance	C_{oss}		—	700	—	pF
Reverse Transfer Capacitance	C_{rss}	V_{GD}=5V, f=1MHz	—	60	—	pF
Turn-on Time	t_{on}	I_D=−2A, V_{GS}=−15V, R_L=15Ω	—	60	—	ns
Turn-off Time	t_{off}		—	200	—	ns

*Pulse Test

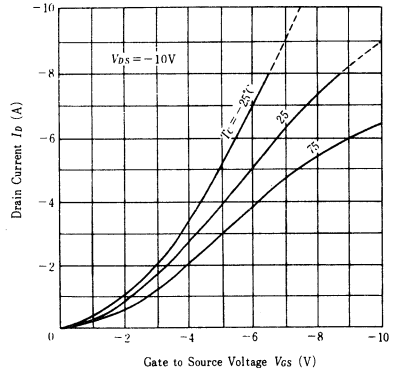
MAXIMUM SAFE OPERATION AREA



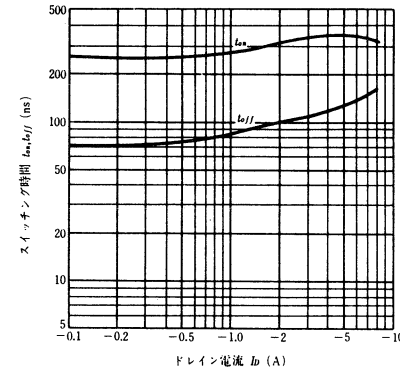
TYPICAL OUTPUT CHARACTERISTICS



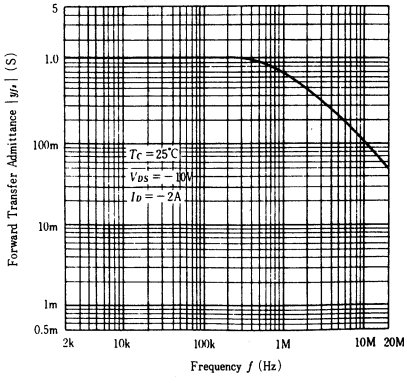
TYPICAL TRANSFER CHARACTERISTICS



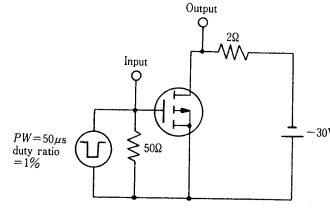
SWITCHING TIME VS. DRAIN CURRENT



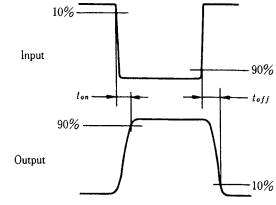
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



2SJ76,2SJ77, 2SJ78,2SJ79

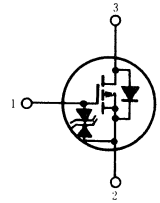
SILICON P-CHANNEL MOS FET

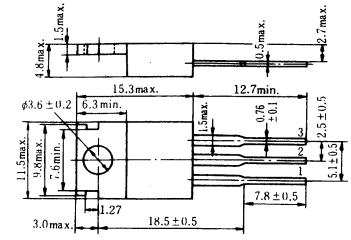
HIGH FREQUENCY AND LOW FREQUENCY POWER AMPLIFIER, HIGH SPEED SWITCHING

Complementary Pair with 2SK213, 2SK214, 2SK215, 2SK216

■ FEATURES

- Suitable for Direct Mounting.
- High Forward Transfer Admittance.
- Excellent Frequency Response.
- Enhancement-Mode.





1. Gate
2. Source (Flange)
3. Drain

(Dimensions in mm)

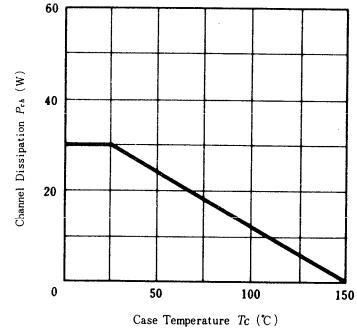
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Ratings				Unit
		2SJ76	2SJ77	2SJ78	2SJ79	
Drain-Source Voltage	V_{DSX}	−140	−160	−180	−200	V
Gate-Source Voltage	V_{GSS}	±15				V
Drain Current	I_D	−500				mA
Body-Drain Diode Reverse Drain Current	I_{DR}	−500				mA
Channel Dissipation	P_{ch}	1.75				W
	P_{ch}*	30				W
Channel Temperature	T_{ch}	150				°C
Storage Temperature	T_{stg}	−45 ~ +150				°C

*Value at T_c=25 °C

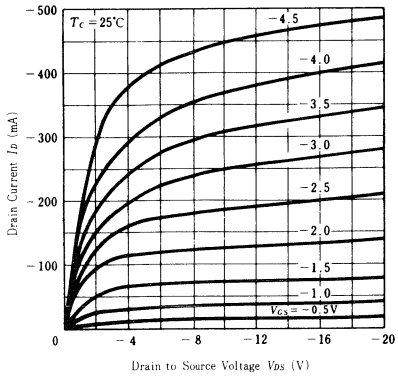
POWER VS. TEMPERATURE DERATING



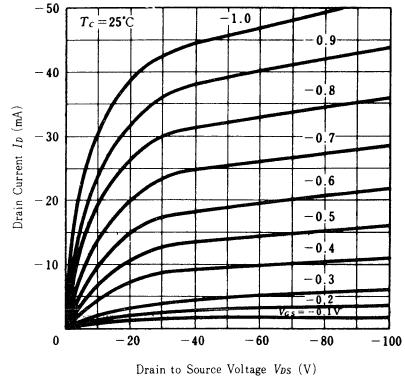
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SJ76	$V_{(BR)DSX}$	V_{GS}=2V, I_D=−1mA	−140	—	—	V
	2SJ77			−160	—	—	V
	2SJ78			−180	—	—	V
	2SJ79			−200	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±10μA, V_{DS}=0	±15	—	—	V
Gate-Source Voltage		$V_{GS(on)}$	I_D=−10mA, V_{DS}=−10V*	−0.2	—	−1.5	V
Drain-Source Saturation Voltage		$V_{DS(sat)}$	I_D=−10mA, V_{GD}=0*	—	—	−2.0	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=−10mA, V_{DS}=−20V*	20	35	—	mS
Input Capacitance		C_{iss}	V_{DS}=−10V, I_D=−10mA, f=1MHz	—	120	—	pF
Reverse Transfer Capacitance		C_{rss}		—	4.8	—	pF

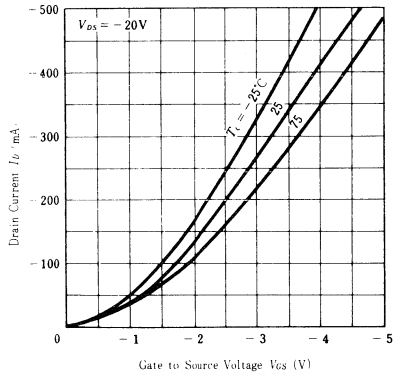
TYPICAL OUTPUT CHARACTERISTICS



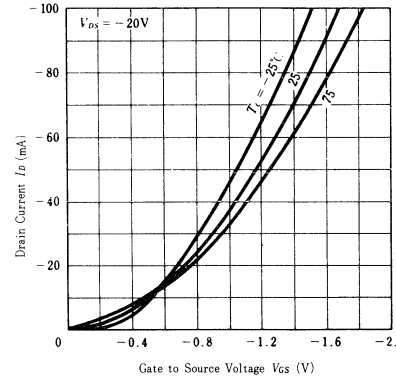
TYPICAL OUTPUT CHARACTERISTICS



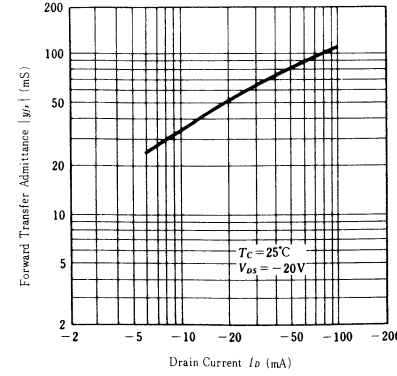
TYPICAL TRANSFER CHARACTERISTICS



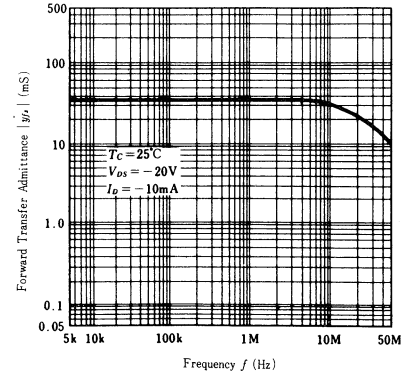
TYPICAL TRANSFER CHARACTERISTICS



FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



2SJ101, 2SJ102

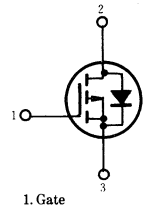
SILICON P-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

Complementary pair with 2SK345, 2SK346

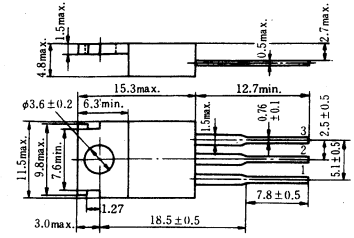
■ Features

- Low On-Resistance.
- High Speed Switching.
- No Secondary Breakdown.
- Good Complementary Characteristics.
- Suitable for PWM Amplifier, Switching Regulator, and DC-DC Converter.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

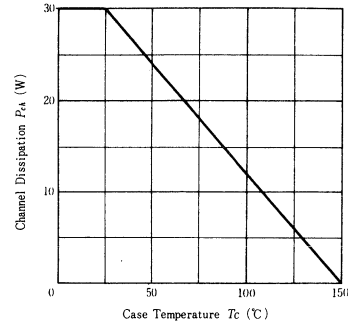


■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SJ101	2SJ102	
Drain-Source Voltage	V_{DSS}	−40	−60	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	−5		A
Drain Peak Current	$I_{D(peak)}$	−10		A
Body-Drain Diode Reverse Drain Current	I_{DR}	−5		A
Channel Dissipation	P_{ch}*	30		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

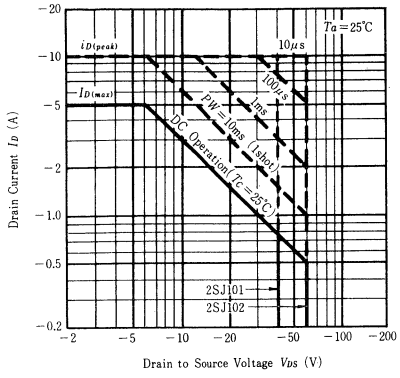


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

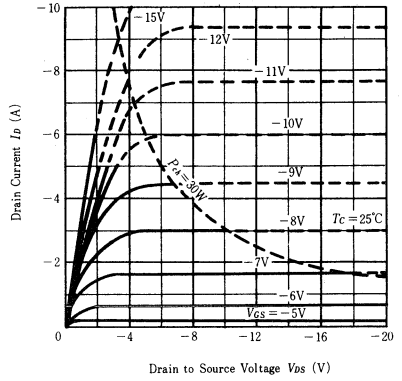
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SJ101	$V_{(BR)DSS}$	I_D=−10mA, V_{GS}=0	−40	—	—	V
	2SJ102			−60	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	2SJ101	I_{DSS}	V_{DS}=−30V, V_{GS}=0	—	—	−1	mA
	2SJ102		V_{DS}=−50V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=−1mA, V_{DS}=−10V	−2.0	—	−5.0	V
Static Drain-Source on State Resistance		$R_{DS(on)}$	I_D=−3A, V_{GS}=−15V*	—	0.3	0.4	Ω
Drain-Source Saturation Voltage		$V_{DS(on)}$	I_D=−3A, V_{GS}=−15V*	—	−0.9	−1.2	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=−3A, V_{DS}=−10V*	0.5	1.0	—	S
Input Capacitance		C_{iss}	V_{DS}=−10V, V_{GS}=0, f=1MHz	—	660	—	pF
Output Capacitance		C_{oss}		—	550	—	pF
Reverse Transfer Capacitance		C_{rss}		—	140	—	pF
Turn-on Time		$t_{d(on)}$	I_D=−2A, V_{GS}=−15V, R_L=15Ω	—	15	—	ns
Rise Time		t_r		—	45	—	ns
Turn-off Time		$t_{d(off)}$		—	45	—	ns
Fall Time		t_f		—	55	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=−3A, V_{GS}=0	—	−0.9	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=−3A, V_{GS}=0, di_F/dt=50A/μs	—	140	—	ns

*Pulse Test

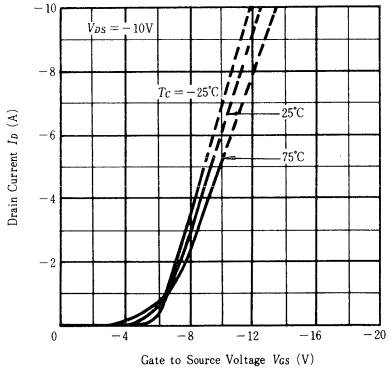
MAXIMUM SAFE OPERATION AREA



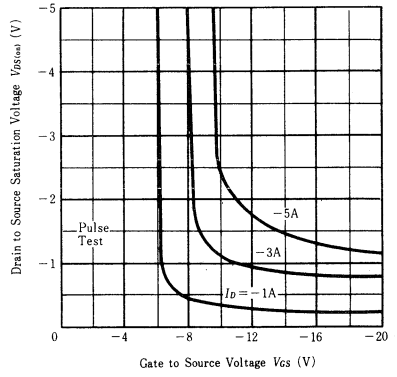
TYPICAL OUTPUT CHARACTERISTICS



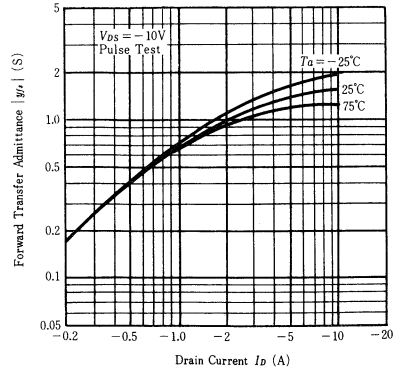
TYPICAL TRANSFER CHARACTERISTICS



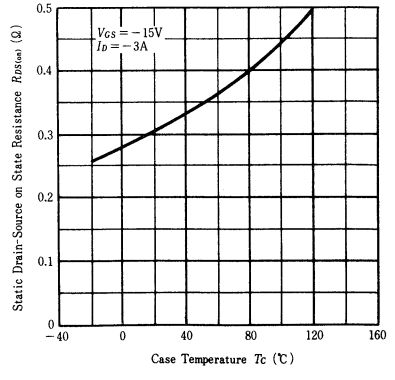
DRAIN—SOURCE SATURATION VOLTAGE VS. GATE—SOURCE VOLTAGE



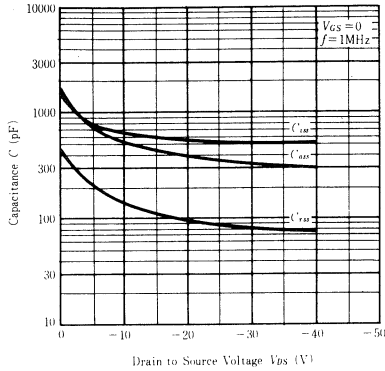
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



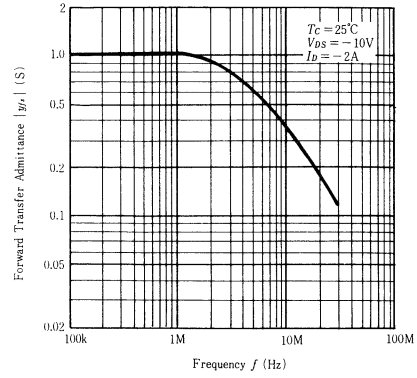
STATIC DRAIN—SOURCE ON STATE RESISTANCE VS. TEMPERATURE



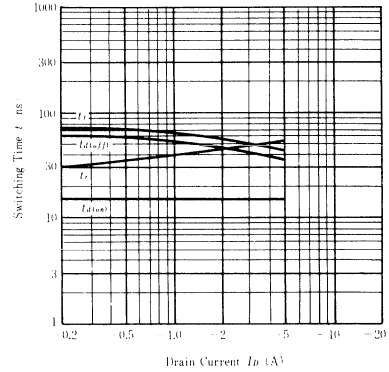
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



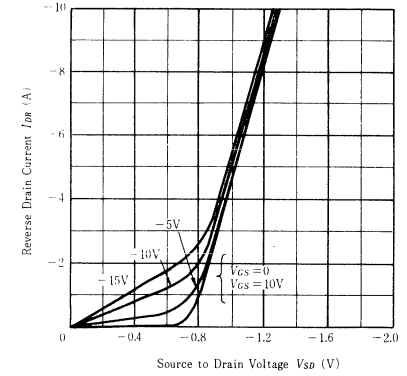
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



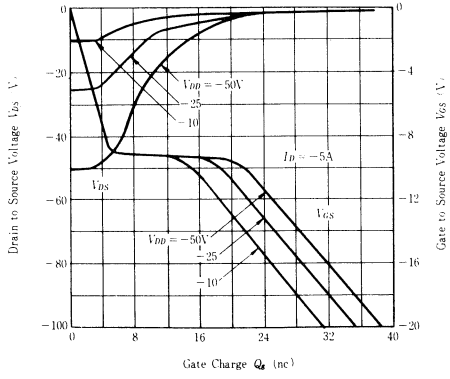
SWITCHING CHARACTERISTICS



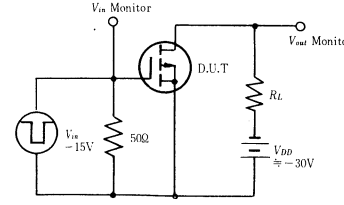
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



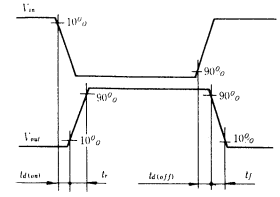
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS

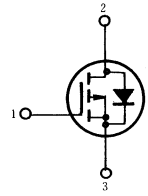


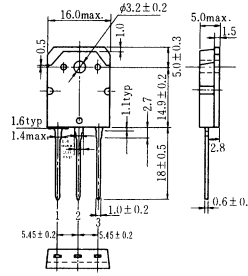
2SJ113

SILICON P-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

Complementary pair with 2SK399





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

(TO-3P)

■ FEATURES

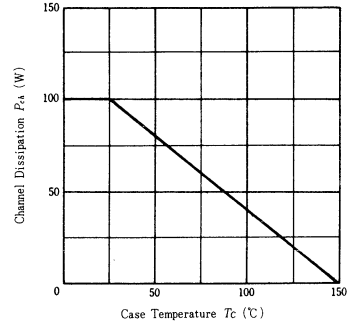
- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Control, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	−100	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	−10	A
Drain Peak Current	$I_{D(peak)}$	−15	A
Body-Drain Diode Reverse Drain Current	I_{DR}	−10	A
Channel Dissipation	P_{ch}*	100	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING



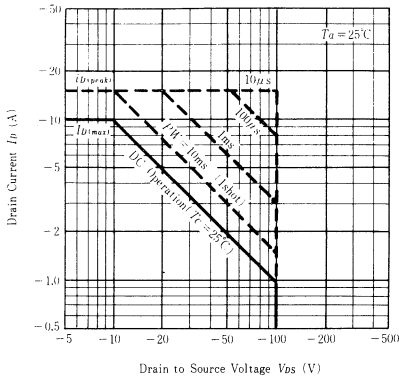
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−10mA, V_{GS}=0	−100	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=−80V, V_{GS}=0	—	—	−1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=−1mA, V_{DS}=−10V	−2.0	—	−5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=−5A, V_{GS}=−15V*	—	0.25	0.35	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=−5A, V_{GS}=−15V*	—	−1.25	−1.75	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=−5A, V_{DS}==−10V*	1.5	2.0	—	S
Input Capacitance	C_{iss}	V_{DS}=−10V, V_{GS}=0, f=1MHz	—	1100	—	pF
Output Capacitance	C_{oss}		—	650	—	pF
Reverse Transfer Capacitance	C_{rss}		—	90	—	pF
Turn-on Time	$t_{d(on)}$	I_D=−2A, V_{GS}=−15V, R_L=15Ω	—	20	—	ns
Rise Time	t_r		—	50	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	90	—	ns
Fall Time	t_f		—	70	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=−5A, V_{GS}=0	—	−0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=−5A, V_{GS}=0, di_F/dt=50A/μs	—	250	—	ns

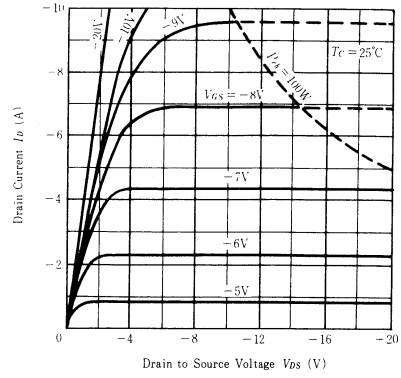
*Pulse Test

HITACHI

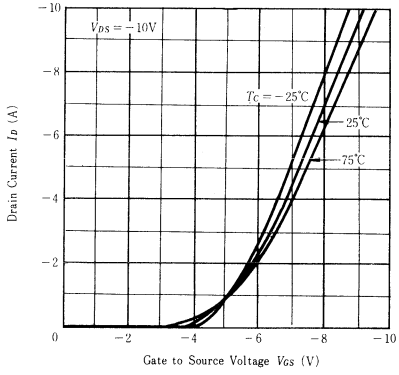
MAXIMUM SAFE OPERATION AREA



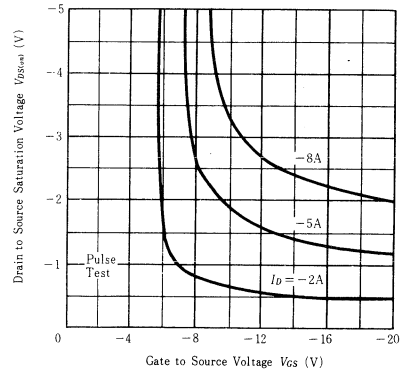
TYPICAL OUTPUT CHARACTERISTICS



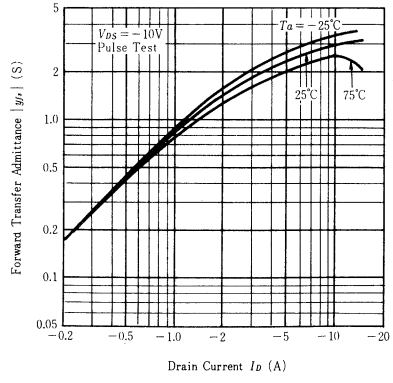
TYPICAL TRANSFER CHARACTERISTICS



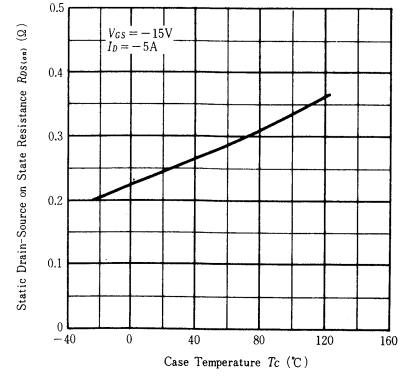
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE—SOURCE VOLTAGE



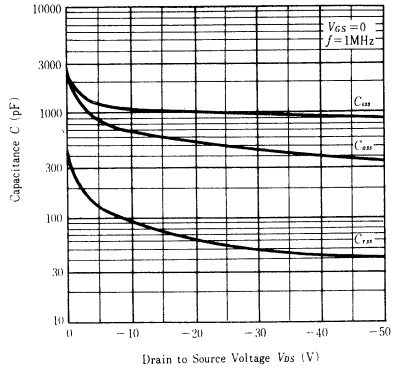
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



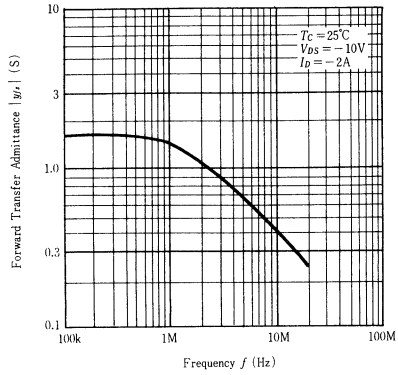
STATIC DRAIN—SOURCE ON STATE RESISTANCE VS. TEMPERATURE



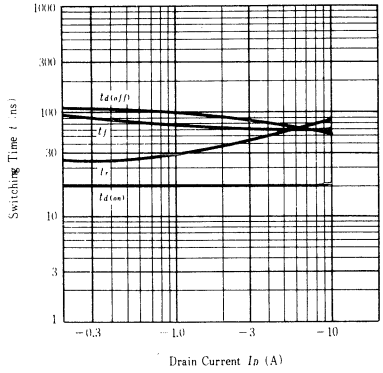
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



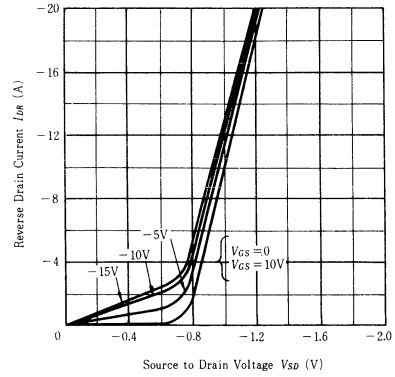
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



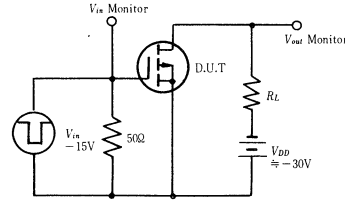
SWITCHING CHARACTERISTICS



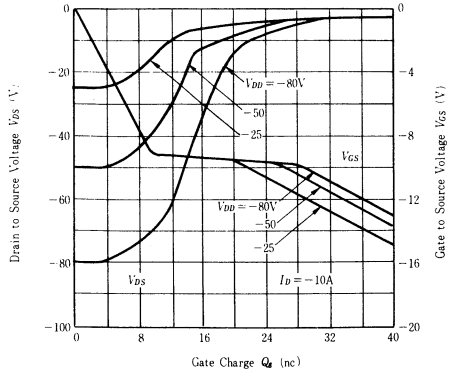
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



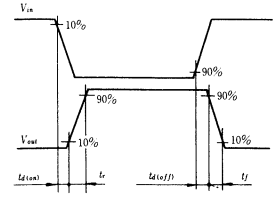
SWITCHING TIME TEST CIRCUIT



DYNAMIC INPUT CHARACTERISTICS



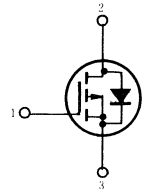
WAVEFORMS

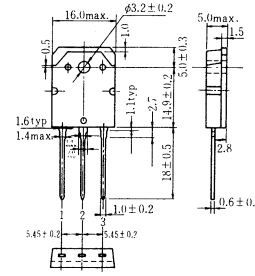


2SJ114

SILICON P-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

(TO-3P)

■ FEATURES

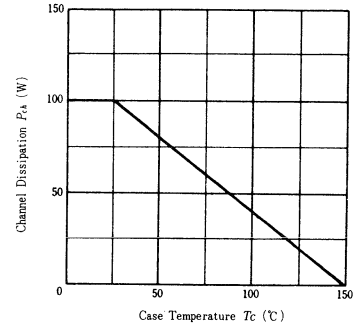
- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Control, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	−200	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	−8	A
Drain Peak Current	$I_{D(peak)}$	−12	A
Body-Drain Diode Reverse Drain Current	I_{DR}	−8	A
Channel Dissipation	P_{ch}*	100	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

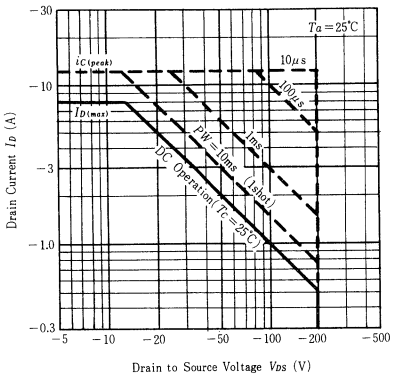


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

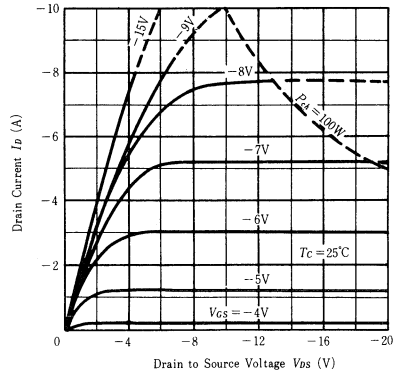
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−10mA, V_{GS}=10V	−200	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=−160V, V_{GS}=0	—	—	−1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=−1mA, V_{DS}=−10V	−2.0	—	−5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=−4A, V_{GS}=−15V*	—	0.6	0.8	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=−4A, V_{GS}=−15V*	—	−2.4	−3.2	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=−4A, V_{DS}=−10V*	1.0	1.8	—	S
Input Capacitance	C_{iss}	V_{DS}=−10V, V_{GS}=0, f=1MHz	—	1000	—	pF
Output Capacitance	C_{oss}		—	400	—	pF
Reverse Transfer Capacitance	C_{rss}		—	70	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=−2A, V_{GS}=−15V, R_L=15Ω	—	15	—	ns
Rise Time	t_r		—	35	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	100	—	ns
Fall Time	t_f		—	60	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=−4A, V_{GS}=0	—	−0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=−4A, V_{GS}=0, di_F/dt=50A/μs	—	300	—	ns

*Pulse Test

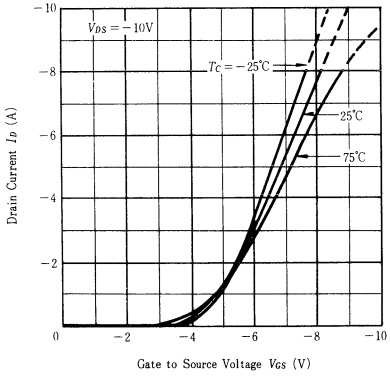
MAXIMUM SAFE OPERATION AREA



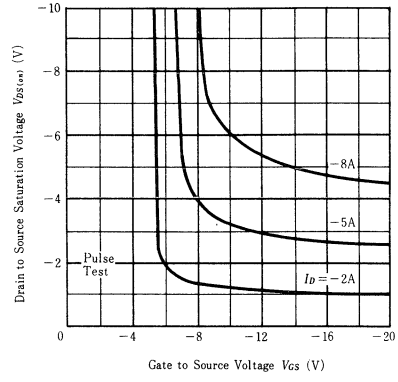
TYPICAL OUTPUT CHARACTERISTICS



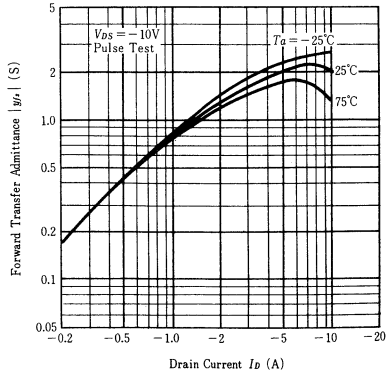
TYPICAL TRANSFER CHARACTERISTICS



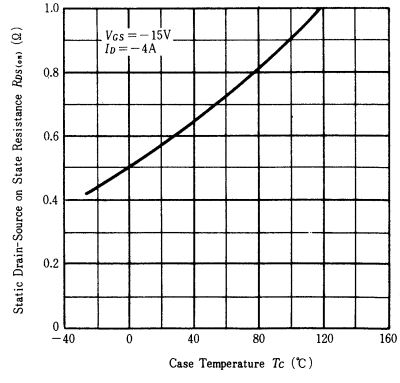
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



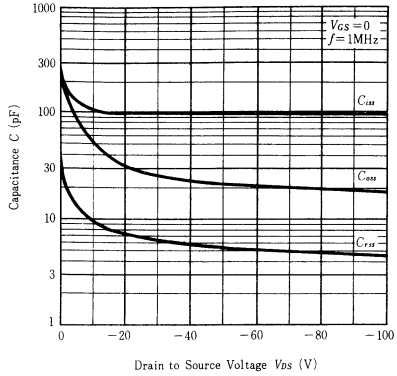
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



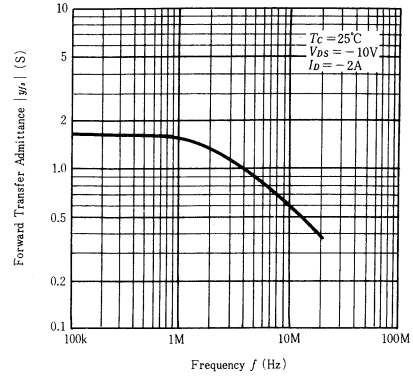
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



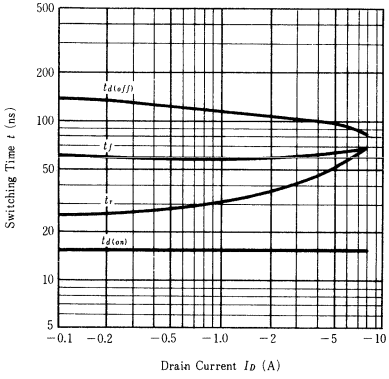
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



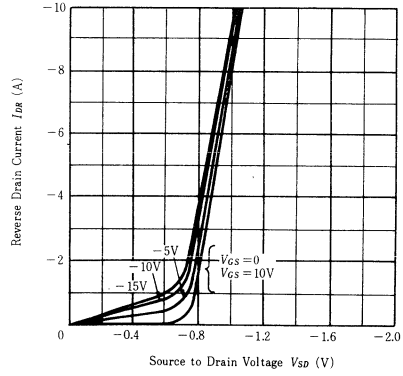
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



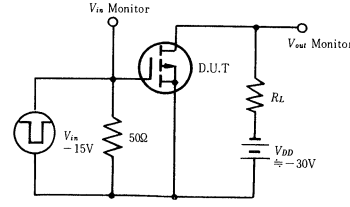
SWITCHING CHARACTERISTICS



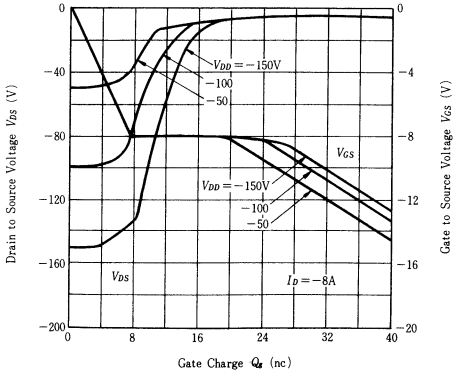
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



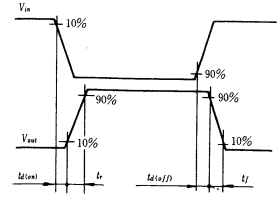
SWITCHING TIME TEST CIRCUIT



DYNAMIC INPUT CHARACTERISTICS



WAVEFORMS

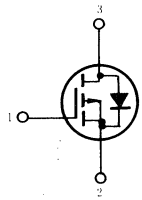


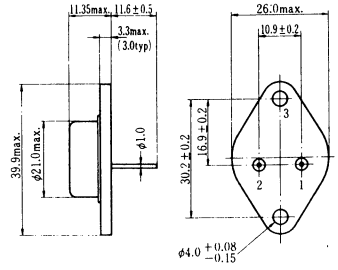
2SJ116

SILICON P-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

Complementary Pair with 2SK298, 2SK312





1. Gate
2. Source
3. Drain (Case)

(Dimensions in mm)

(JEDEC TO-3)

■ FEATURES

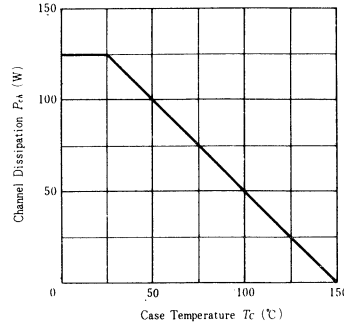
- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	−400	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	−8	A
Drain Peak Current	$I_{D(peak)}$	−15	A
Body-Drain Diode Reverse Drain Current	I_{DR}	−8	A
Channel Dissipation	P_ch*	125	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c 25 °C

POWER VS. TEMPERATURE DERATING



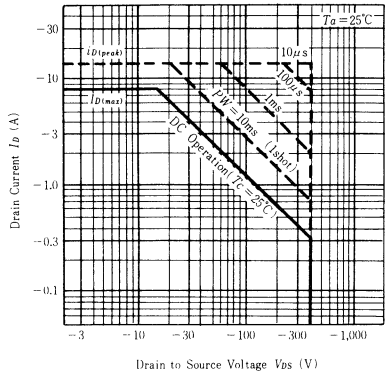
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−10mA, V_{GS}=0	−400	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=−320V, V_{GS}=0	—	—	−1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=−1mA, V_{DS}=−10V	−0.2	—	−5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=−4A, V_{GS}=−15V*	—	1.75	2.25	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=−4A, V_{GS}=−15V*	—	−7.0	−9.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=−4A, V_{DS}=−20V*	1.0	1.6	—	S
Input Capacitance	C_{iss}	V_{DS}=−10V, V_{GS}=0, f=1MHz	—	1400	—	pF
Output Capacitance	C_{oss}		—	330	—	pF
Reverse Transfer Capacitance	C_{rss}		—	25	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=−2A, V_{GS}=−15V, R_l=15Ω	—	15	—	ns
Rise Time	t_r		—	45	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	160	—	ns
Fall Time	t_f		—	60	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=−4A, V_{GS}=0	—	−0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=−4A, V_{GS}=0, di_F/dt=100A/μs	—	400	—	ns

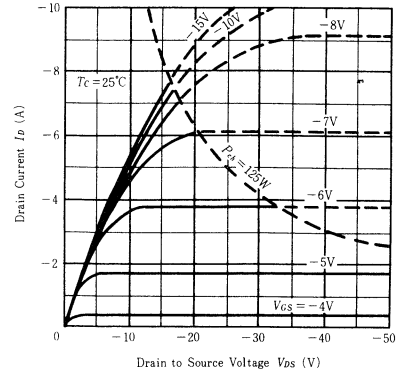
*Pulse Test

HITACHI

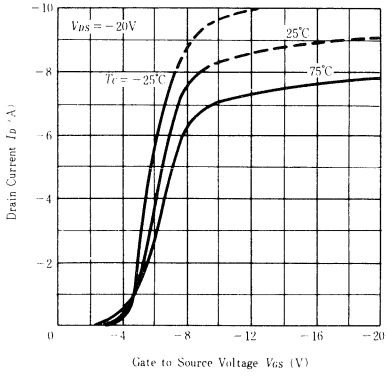
MAXIMUM SAFE OPERATION AREA



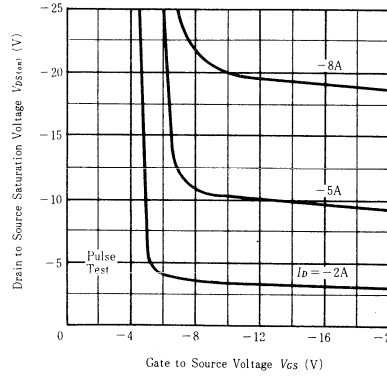
TYPICAL OUTPUT CHARACTERISTICS



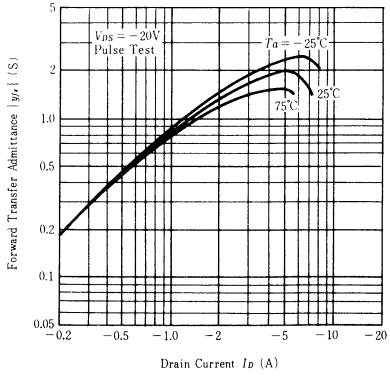
TYPICAL TRANSFER CHARACTERISTICS



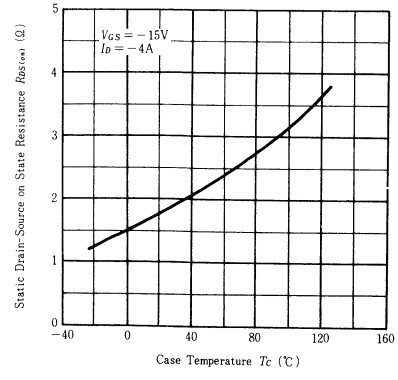
DRAIN - SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



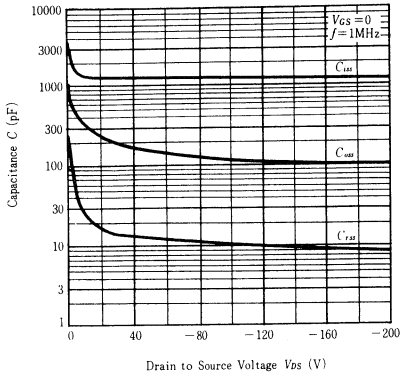
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



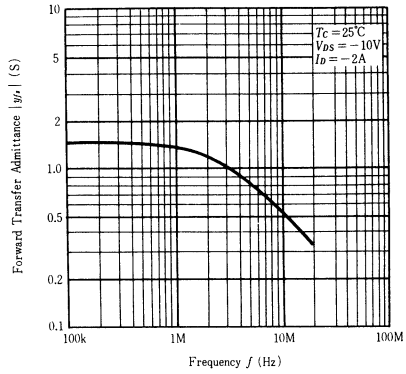
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



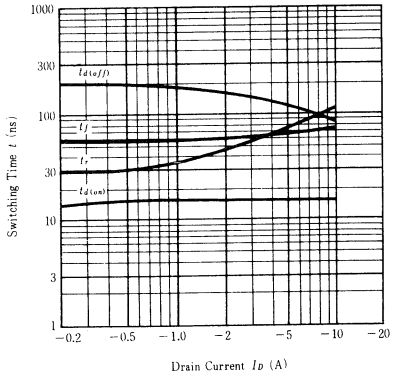
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



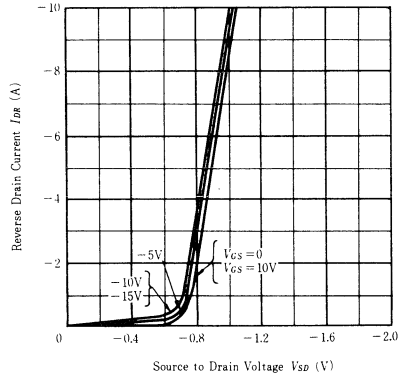
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



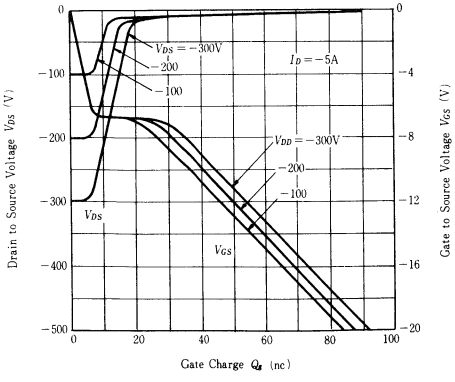
SWITCHING CHARACTERISTICS



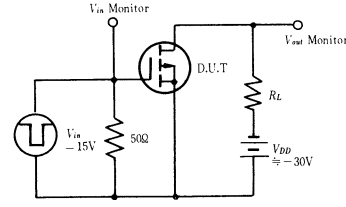
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



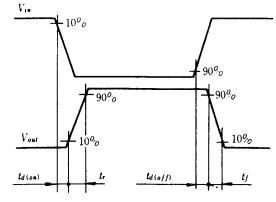
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS

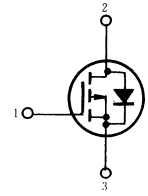


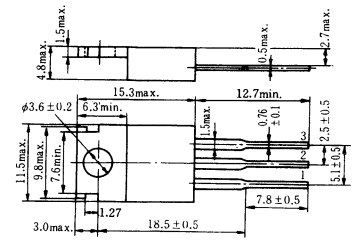
2SJ117

SILICON P-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

Complementary pair with 2SK310





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

(JEDEC TO-220AB)

■ FEATURES

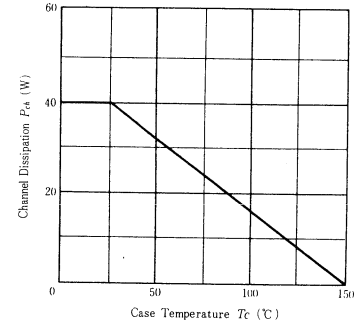
- High Breakdown Voltage.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	−400	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	−2	A
Drain Peak Current	$I_{D(peak)}$	−4	A
Body-Drain Diode Reverse Drain Current	I_{DR}	−2	A
Channel Dissipation	P_{ch}*	40	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

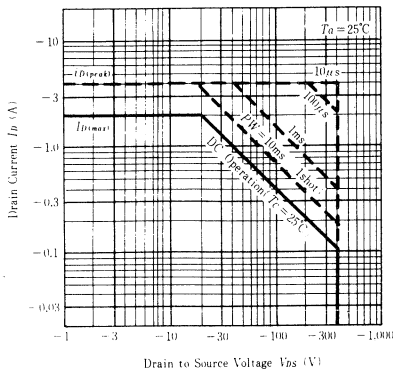


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

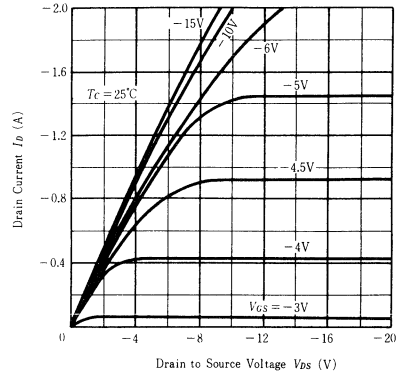
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−10mA, V_{GS}=0	−400	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=−320V, V_{GS}=0	—	—	−1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=−1mA, V_{DS}=−10V	−2.0	—	−5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=−1A, V_{GS}=−15V*	—	5	7	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=−1A, V_{GS}=−15V*	—	−5.0	−7.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=−1A, V_{DS}=−20V*	0.4	0.7	—	S
Input Capacitance	C_{iss}	V_{DS}=−10V, V_{GS}=0, f=1MHz	—	520	—	pF
Output Capacitance	C_{oss}		—	110	—	pF
Reverse Transfer Capacitance	C_{rss}		—	15	—	pF
Turn-on Time	$t_{d(on)}$	I_D=−2A, V_{GS}=−15V, R_L=15Ω	—	10	—	ns
Rise Time	t_r		—	25	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	45	—	ns
Fall Time	t_f		—	35	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=−1A, V_{GS}=0	—	−0.8	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=−1A, V_{GS}=0, di_F/dt=100A/μs	—	300	—	ns

*Pulse Test

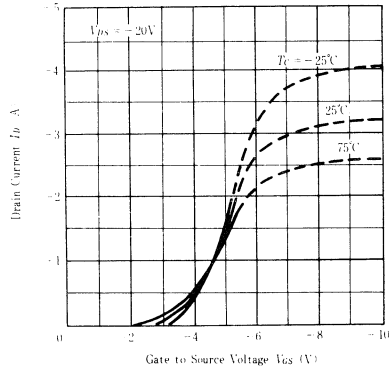
MAXIMUM SAFE OPERATION AREA



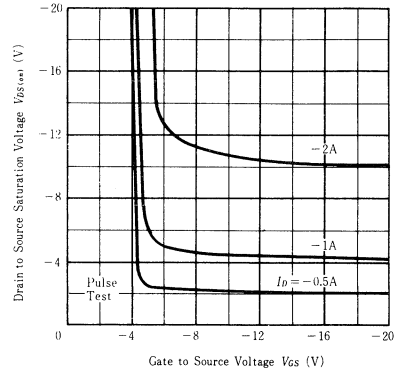
TYPICAL OUTPUT CHARACTERISTICS



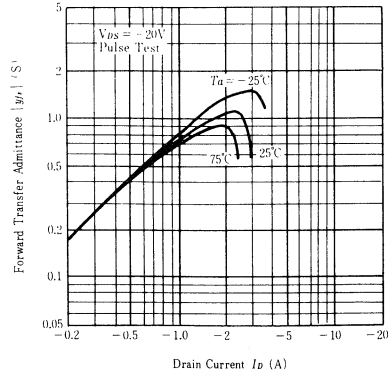
TYPICAL TRANSFER CHARACTERISTICS



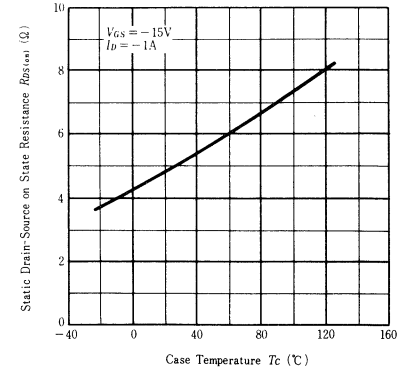
DRAIN - SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



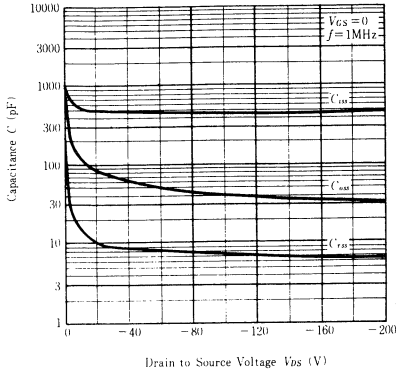
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



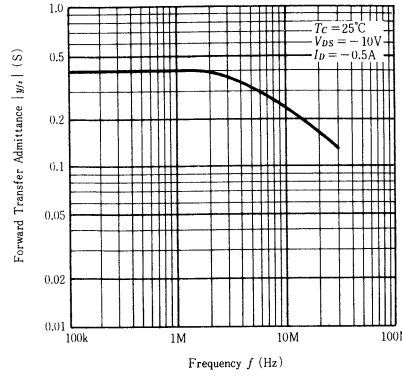
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



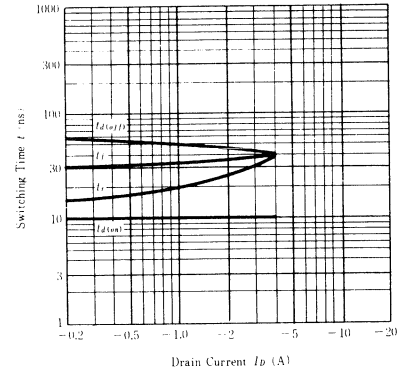
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



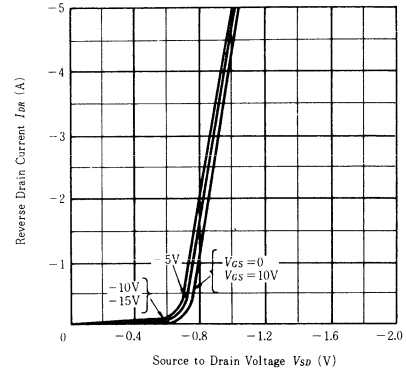
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



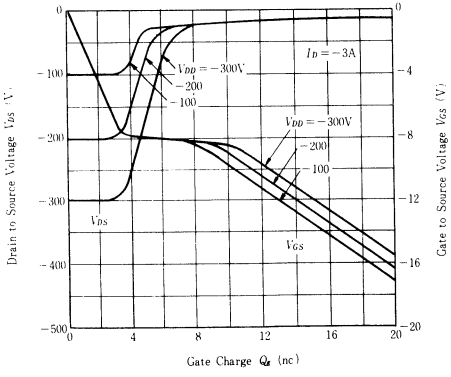
SWITCHING CHARACTERISTICS



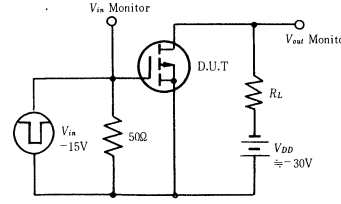
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



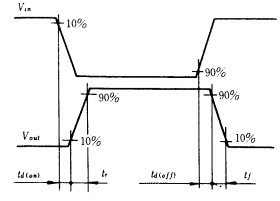
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS

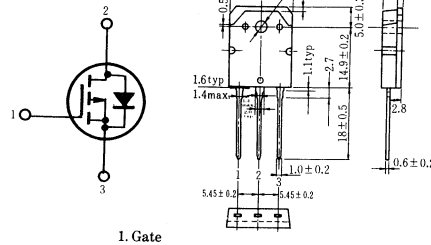


2SJ118,2SJ119

SILICON P-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

Complementary pair with 2SK413, 2SK414



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

(TO-3P)

■ FEATURES

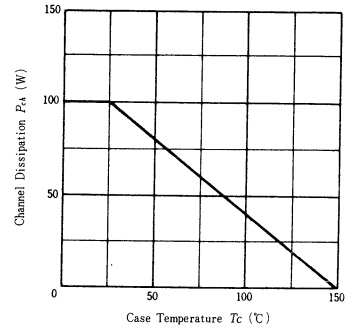
- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, PWM Amplifiers, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	2SJ118	2SJ119	Unit
Drain-Source Voltage	V_{DSS}	−140	−160	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	−8		A
Drain Peak Current	$I_{D(peak)}$	−12		A
Body-Drain Diode Reverse Drain Current	I_{DR}	−8		A
Channel Dissipation	P_{ch}*	100		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

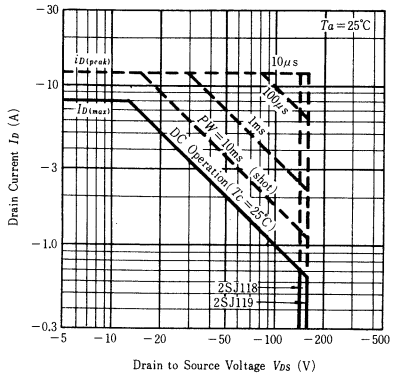


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

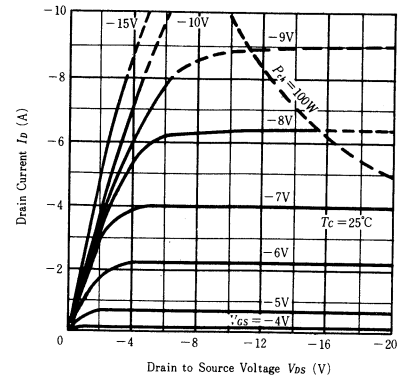
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SJ118	$V_{(BR)DSS}$	I_D=−10mA, V_{GS}=0	−140	—	—	V
	2SJ119			−160	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	2SJ118	I_{DSS}	V_{DS}=−120V, V_{GS}=0	—	—	−1	mA
	2SJ119		V_{DS}=−140V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=−1mA, V_{DS}=−10V	−2.0	—	−5.0	V
Static Drain-Source On State Resistance		$R_{DS(on)}$	I_D=−4A, V_{GS}=−15V*	—	0.4	0.5	Ω
Drain-Source Saturation Voltage		$V_{DS(on)}$	I_D=−4A, V_{GS}=−15V*	—	−1.6	−2.0	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=−4A, V_{DS}=−10V*	1.0	1.8	—	S
Input Capacitance		C_{iss}	V_{DS}=−10V, V_{GS}=0, f=1MHz	—	1050	—	pF
Output Capacitance		C_{oss}		—	450	—	pF
Reverse Transfer Capacitance		C_{rss}		—	80	—	pF
Turn-on Time		$t_{d(on)}$	I_D=−2A, V_{GS}=−15V R_L=2Ω	—	20	—	ns
Rise Time		t_r		—	50	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	90	—	ns
Fall Time		t_f		—	70	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=−4A, V_{GS}=0	—	−0.9	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=−4A, V_{GS}=0 di_F/dt=50A/μs	—	300	—	ns

*Pulse Test

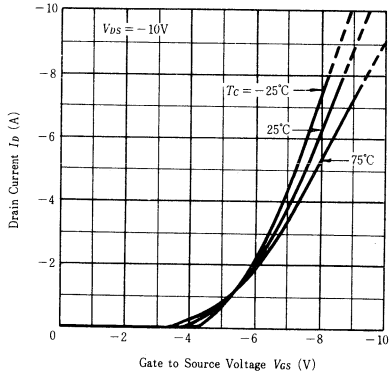
MAXIMUM SAFE OPERATION AREA



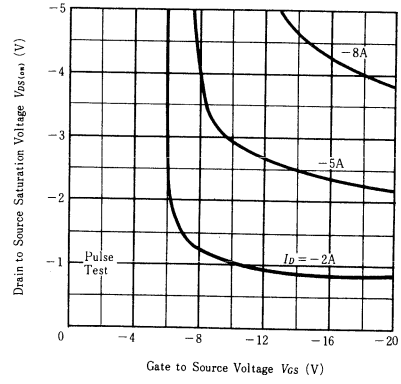
TYPICAL OUTPUT CHARACTERISTICS



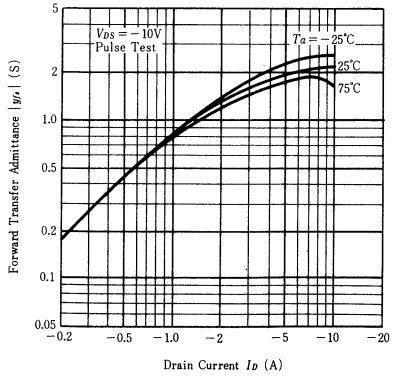
TYPICAL TRANSFER CHARACTERISTICS



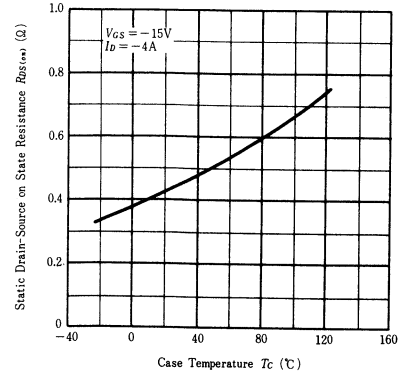
DRAIN - SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



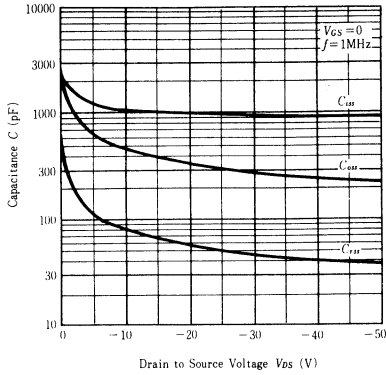
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



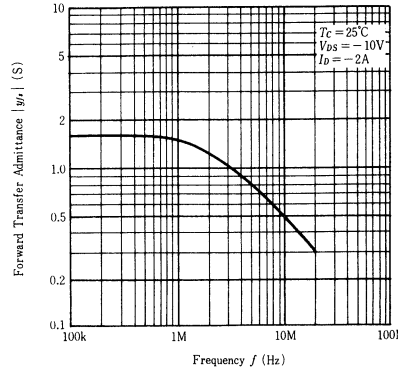
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



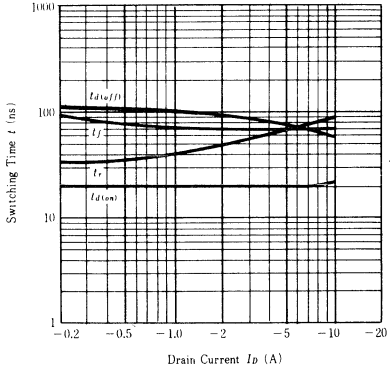
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



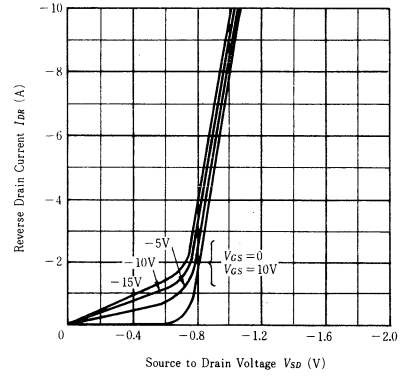
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



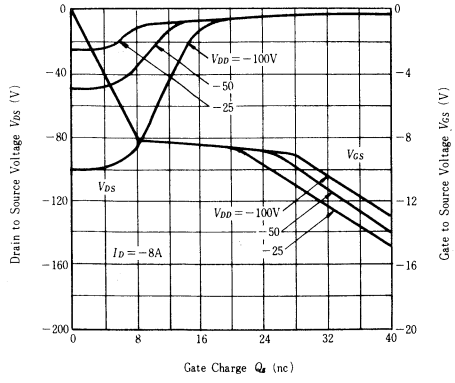
SWITCHING CHARACTERISTICS



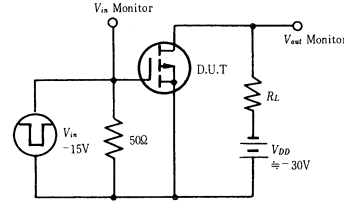
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



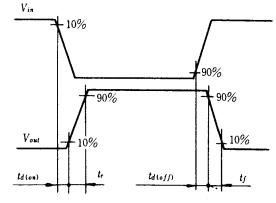
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



HITACHI

2SJ120Ⓛ, 2SJ120Ⓢ

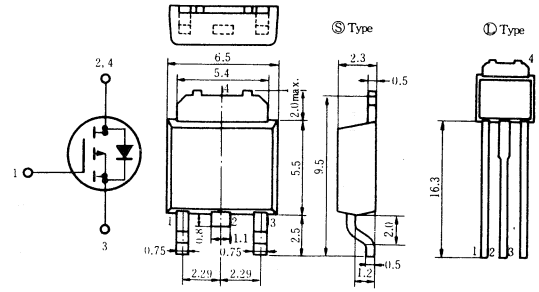
SILICON P-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLI

Complementary pair with 2SK416

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, and Bubble Memory Driver.



1. Gate
2., 4. Drain
3. Source

(Dimensions in mm)

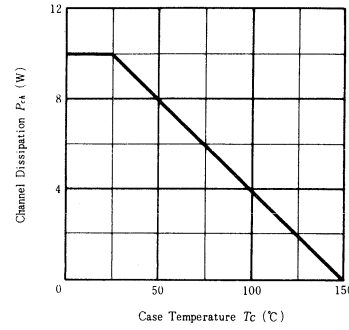
(DPAK)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	−40	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	−2	A
Drain Peak Current	$I_{D(peak)}$	−4	A
Body-Drain Diode Reverse Drain Current	I_{DR}	−2	A
Channel Dissipation	P_{ch}*	10	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

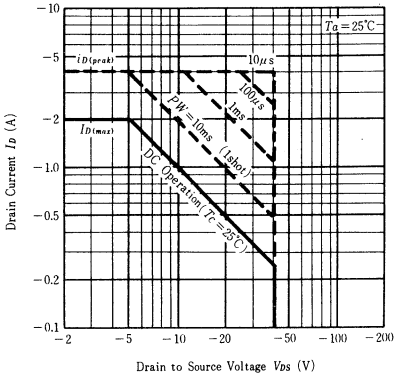


■ ELECTRICAL CHARACTERISTICS (T_a=25° C)

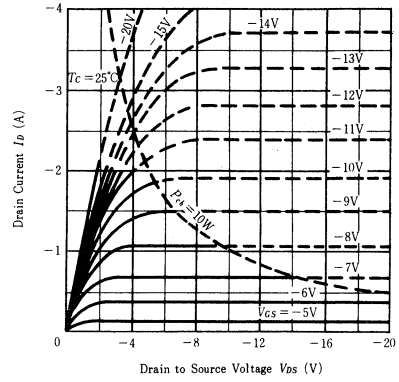
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−10mA, V_{GS}=0	−40	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=−35V, V_{GS}=0	—	—	−1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=−1mA, V_{DS}=−10V	−1.0	—	−4.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=−1A, V_{GS}=−15V*	—	1.2	1.5	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=−1A, V_{GS}=−15V*	—	−1.2	−1.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=−1A, V_{DS}=−10V*	0.1	0.25	—	S
Input Capacitance	C_{iss}	V_{DS}=−10V, V_{GS}=0, f=1MHz	—	150	—	pF
Output Capacitance	C_{oss}		—	150	—	pF
Reverse Transfer Capacitance	C_{rss}		—	25	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=−1A, V_{GS}=−15V R_L=30Ω	—	9	—	ns
Rise Time	t_r		—	25	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	17	—	ns
Fall Time	t_f		—	23	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=−1A, V_{GS}=0	—	−0.8	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=−1A, V_{GS}=0 di_F/dt=50A/μs	—	70	—	ns

*Pulse Test

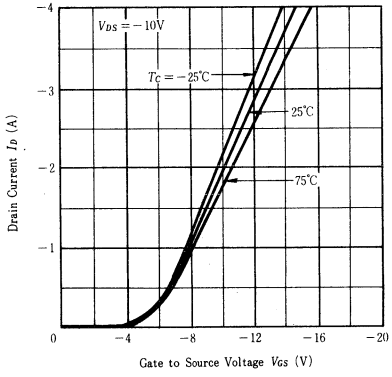
MAXIMUM SAFE OPERATION AREA



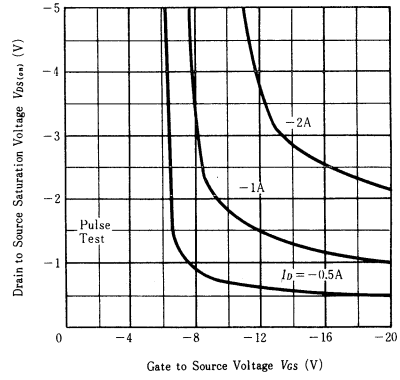
TYPICAL OUTPUT CHARACTERISTICS



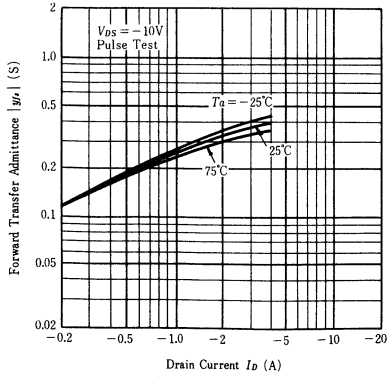
TYPICAL TRANSFER CHARACTERISTICS



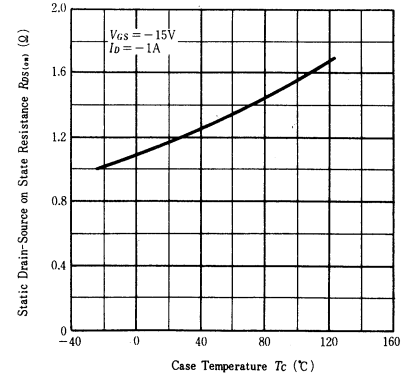
DRAIN TO SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



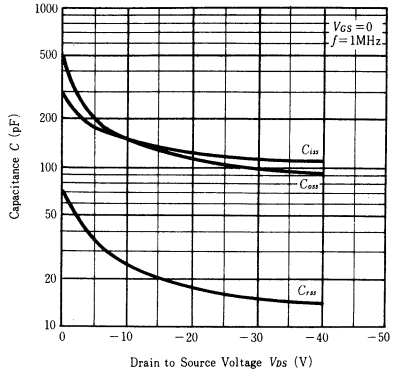
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



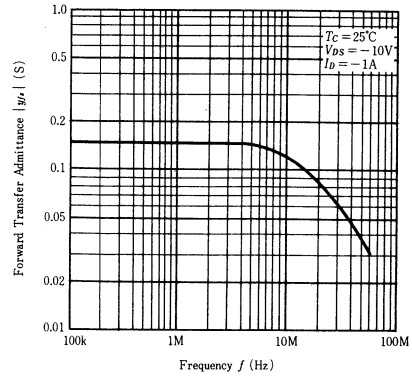
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



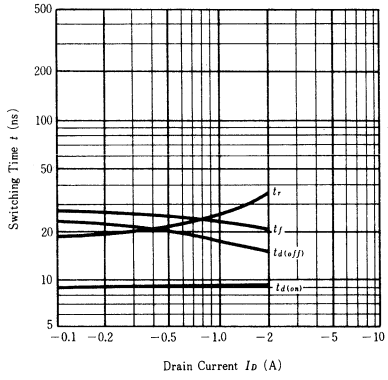
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



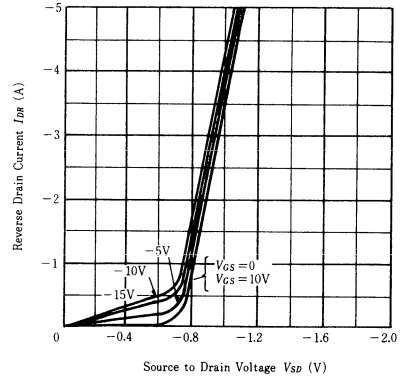
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



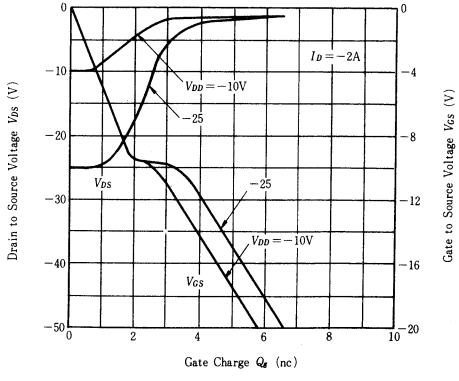
SWITCHING CHARACTERISTICS



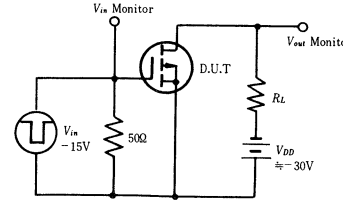
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



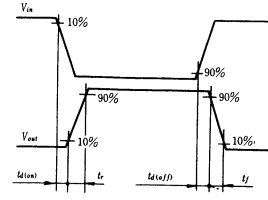
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS

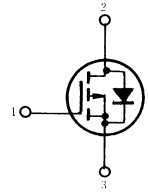


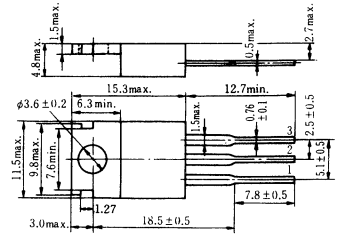
2SJ122

SILICON P-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

Complementary pair with 2SK428





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

(JEDEC TO-220AB)

■ FEATURES

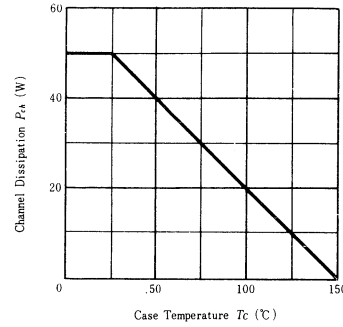
- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, PWM Amplifiers, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	−60	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	−10	A
Drain Peak Current	$I_{D(peak)}$	−15	A
Body-Drain Diode Reverse Drain Current	I_{DR}	−10	A
Channel Dissipation	P_{ch}*	50	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



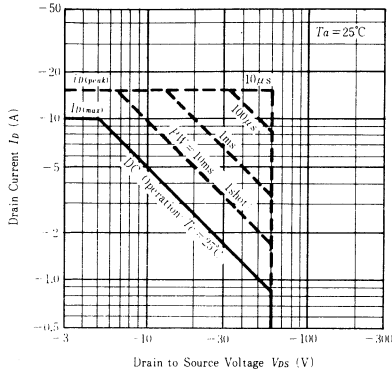
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−10mA, V_{GS}=0	−60	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=−50V, V_{GS}=0	—	—	−1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=−1mA, V_{DS}=−10V	−2.0	—	−5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=−5A, V_{GS}=−15V*	—	0.15	0.2	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=−5A, V_{GS}=−15V*	—	−0.75	−1.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=−5A, V_{DS}=−10V*	1.5	2.2	—	S
Input Capacitance	C_{iss}	V_{DS}=−10V, V_{GS}=0 f=1MHz	—	1200	—	pF
Output Capacitance	C_{oss}		—	1050	—	pF
Reverse Transfer Capacitance	C_{rss}		—	170	—	pF
Turn-on Time	$t_{d(on)}$	I_D=−2A, V_{GS}=−15V R_L=15Ω	—	20	—	ns
Rise Time	t_r		—	60	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	100	—	ns
Fall Time	t_f		—	100	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=−5A, V_{GS}=0	—	−0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=−5A, V_{GS}=0 di_F/dt=50A/μs	—	200	—	ns

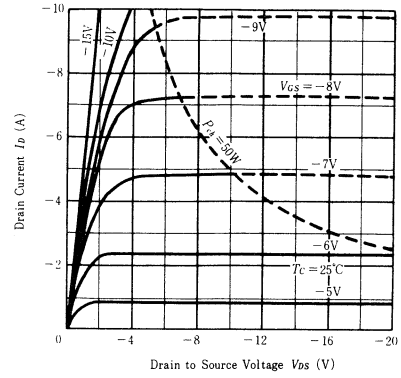
*Pulse Test

HITACHI

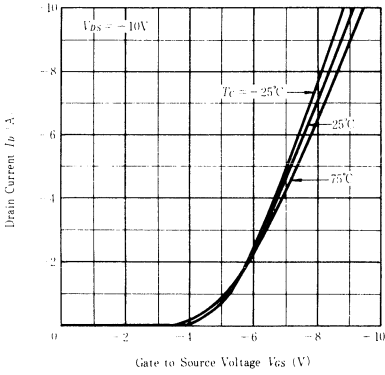
MAXIMUM SAFE OPERATION AREA



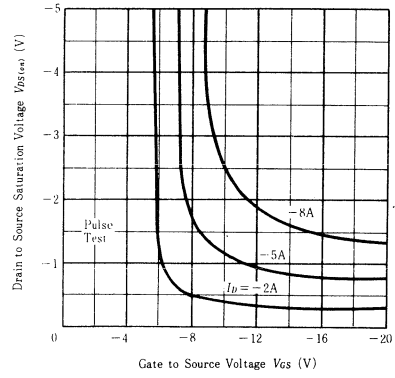
TYPICAL OUTPUT CHARACTERISTICS



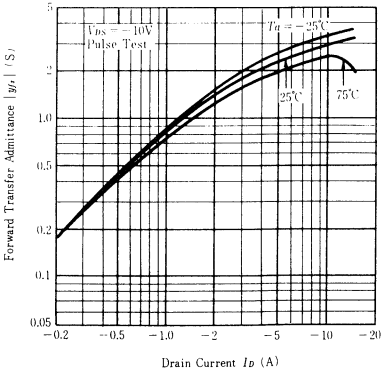
TYPICAL TRANSFER CHARACTERISTICS



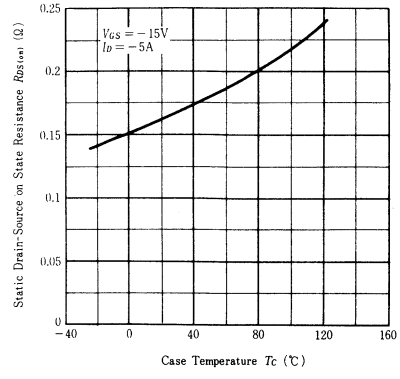
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



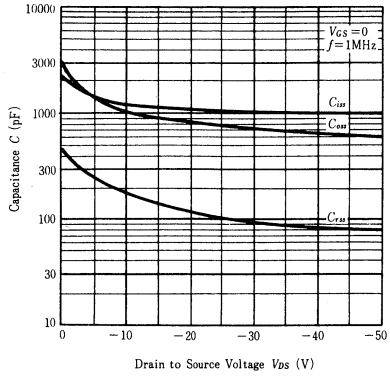
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



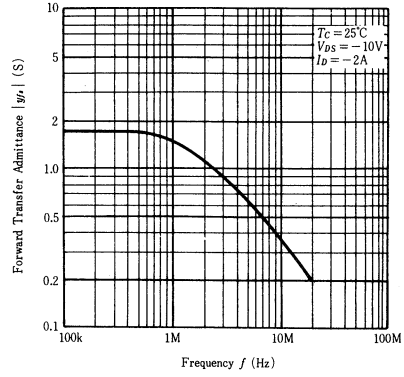
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



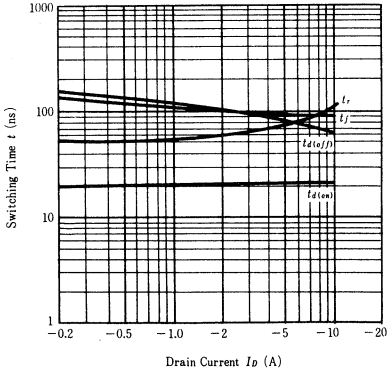
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



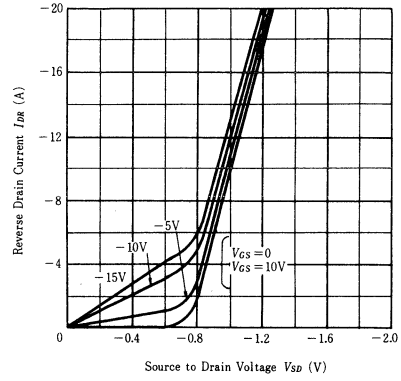
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



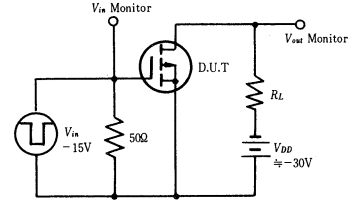
SWITCHING CHARACTERISTICS



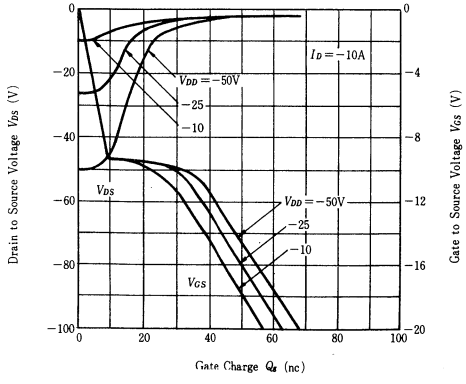
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



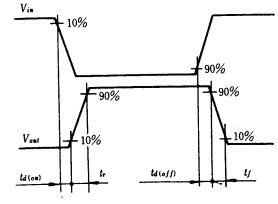
SWITCHING TIME TEST CIRCUIT



DYNAMIC INPUT CHARACTERISTICS



WAVEFORMS

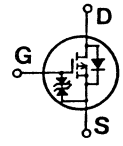


POWER MOS FET DII SERIES

2SJ127

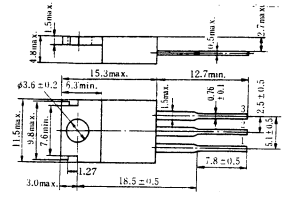
SILICON P CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

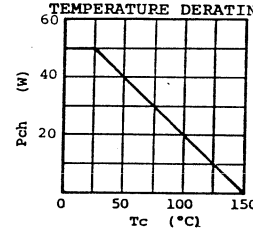
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	-120	V
Gate-Source Voltage	V_{GSS}	±15	V
Drain Current	I_D	-10	A
Drain Peak Current	$I_{D(pulse)}$*	-40	A
Body-Drain Diode Reverse Drain Current	I_{DR}	-10	A
Channel Dissipation	Pch**	50	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 ~ +150	°C

*PW≤10μs, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING

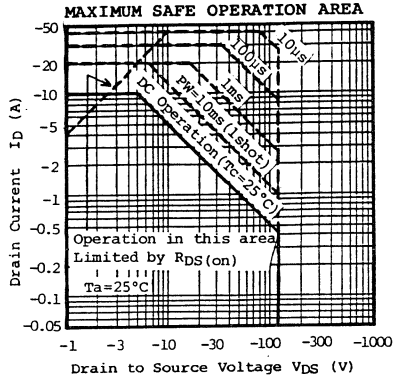


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

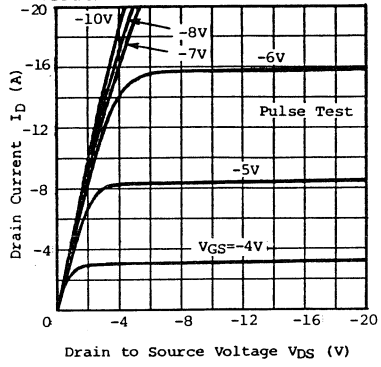
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D= -10mA, V_{GS}=0	-120	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±12V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V, V_{GS}=0	-	-	-250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=-1mA, V_{DS}=-10V	-2.0	-	-4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=-5A, V_{GS}=10V *	-	0.2	0.25	Ω
Foward Transfer Admittance	|yfs|	I_D=-5A, V_{DS}=-10V *	3.0	5.0	-	S
Input Capacitance	Ciss	V_{DS}=-10V, V_{GS}=0 f=1MHz	-	1450	-	pF
Output Capacitance	Coss		-	680	-	pF
Reverse Transfer Capacitance	Crss		-	175	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=-5A, V_{GS}=-10V R_L=6Ω	-	20	-	ns
Rise Time	t_r		-	120	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	240	-	ns
Fall Time	t_f		-	140	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=-10A, V_{GS}=0	-	-1.0	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=-10A, V_{GS}=0 dIF/dt=50 A/μs	-	250	-	ns

*Pulse Test

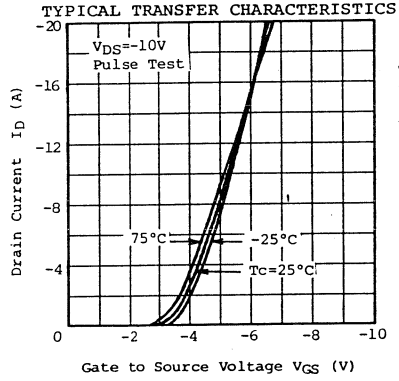
MAXIMUM SAFE OPERATION AREA



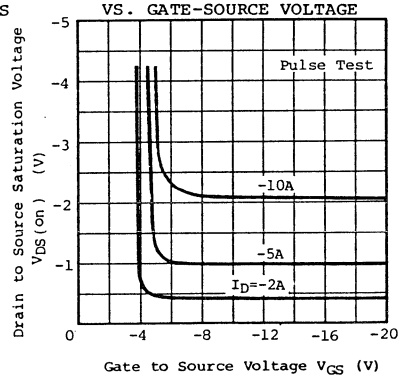
TYPICAL OUTPUT CHARACTERISTICS



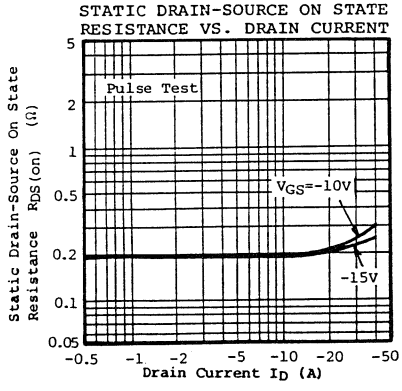
TYPICAL TRANSFER CHARACTERISTICS



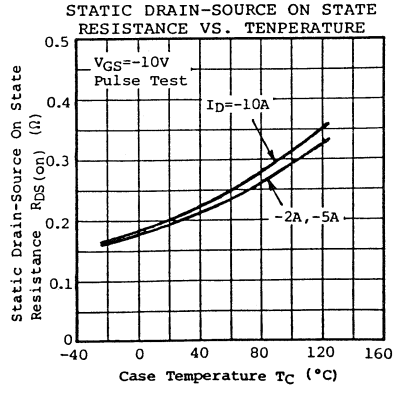
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



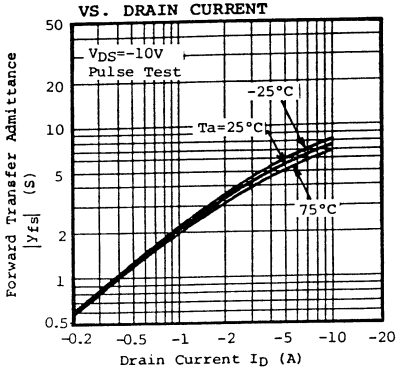
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



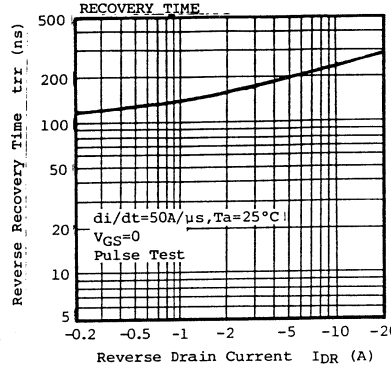
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



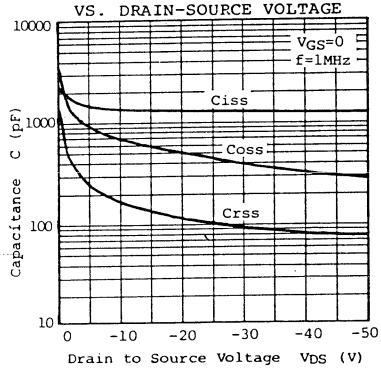
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



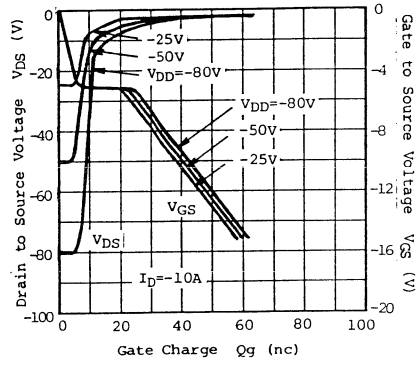
BODY DRAIN DIODE REVERSE RECOVERY TIME



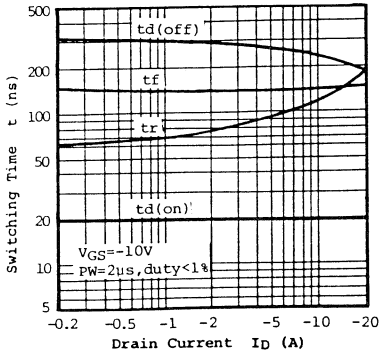
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



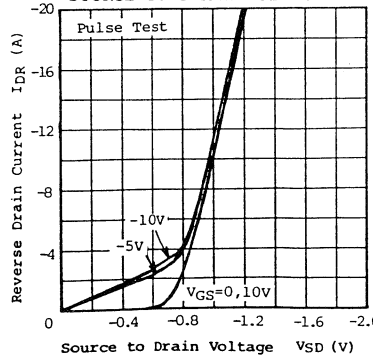
DYNAMIC INPUT CHARACTERISTICS



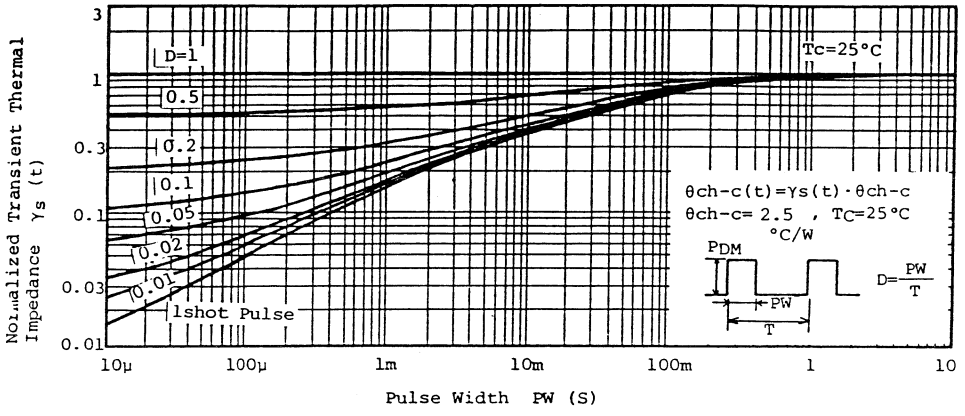
SWITCHING CHARACTERISTICS



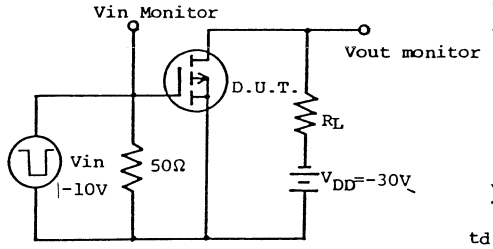
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



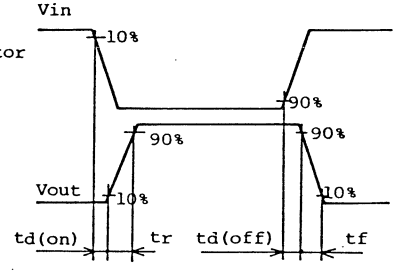
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



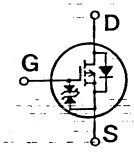
Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

POWER MOS FET DⅡ SERIES

2SJ130Ⓛ, 2SJ130Ⓢ

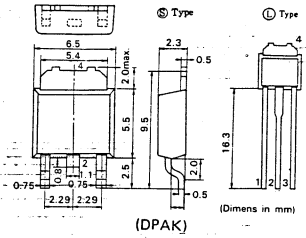
SILICON P CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls, and Ultrasonic Power Oscillators.



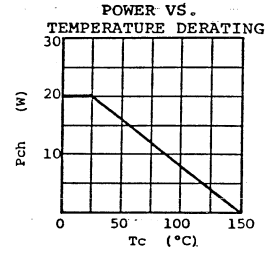
1. Gate
2. Drain
3. Source
4. Drain

(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	-300	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	-1	A
Drain Peak Current	$I_{D(pulse)}$	-2	A
Body-Drain Diode Reverse Drain Current	I_{DR}	-1	A
Channel Dissipation	Pch*	20	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 ~ +150	°C

*Value at Tc=25°C

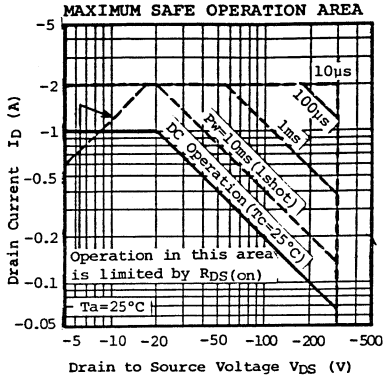


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

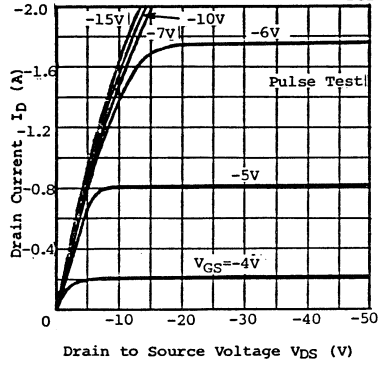
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=-10mA, V_{GS}=0	-300	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-240V, V_{GS}=0	-	-	-100	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=-1mA, V_{DS}=-10V	-2.0	-	-4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=-0.5A, V_{GS}=-10V *	-	6.0	8.5	Ω
Foward Transfer Admittance	$\|Yfs\|$	I_D=-0.5A, V_{DS}=-20V *	0.25	0.4	-	S
Input Capacitance	Ciss	V_{DS}=-10V, V_{GS}=0 f=1MHz	-	235	-	pF
Output Capacitance	Coss		-	65	-	pF
Reverse Transfer Capacitance	Crss		-	16	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=-0.5A, V_{GS}=-10V R_L=60Ω	-	10	-	ns
Rise Time	t_r		-	25	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	35	-	ns
Fall Time	t_f		-	45	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=-1A, V_{GS}=0	-	-0.9	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=-1A, V_{GS}=0 dI_F/dt=50 A/μs	-	200	-	ns

*Pulse Test

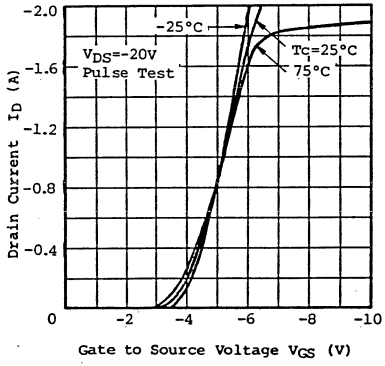
MAXIMUM SAFE OPERATION AREA



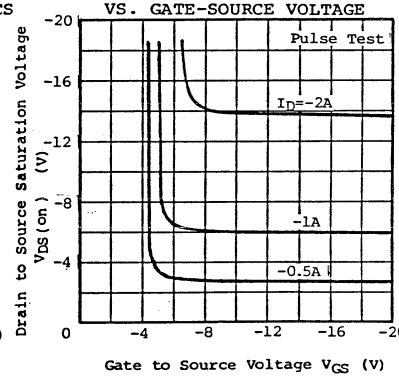
TYPICAL OUTPUT CHARACTERISTICS



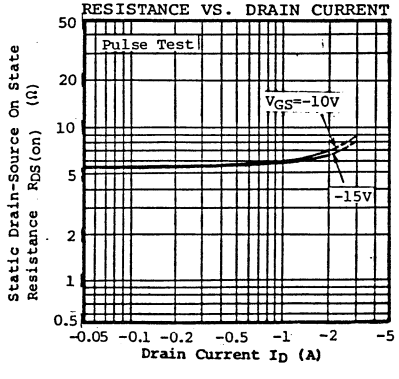
TYPICAL TRANSFER CHARACTERISTICS



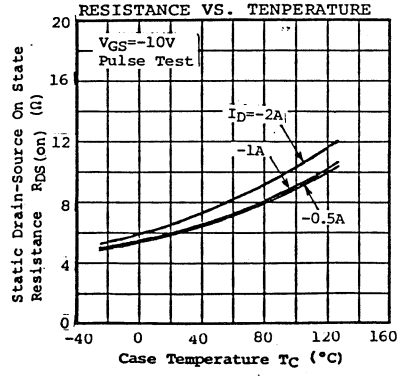
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



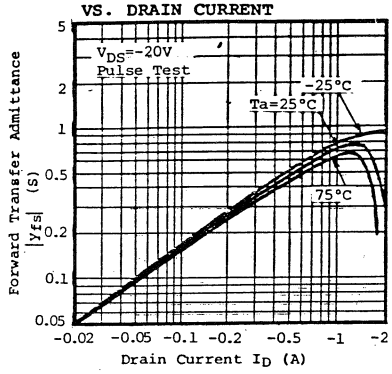
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



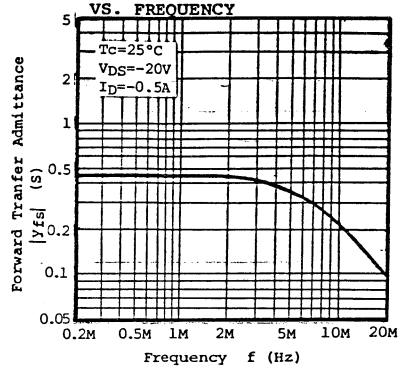
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



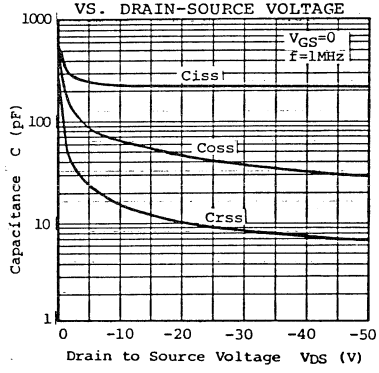
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



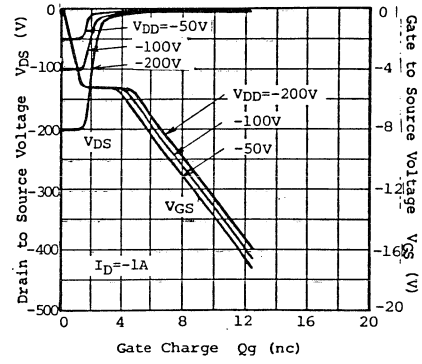
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



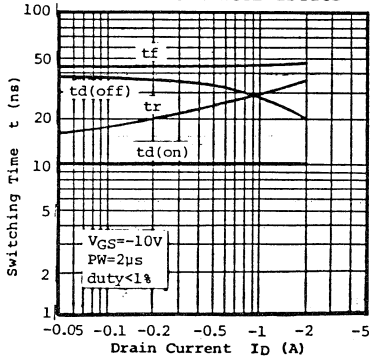
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



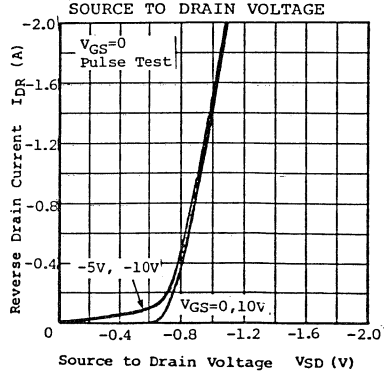
DYNAMIC INPUT CHARACTERISTICS



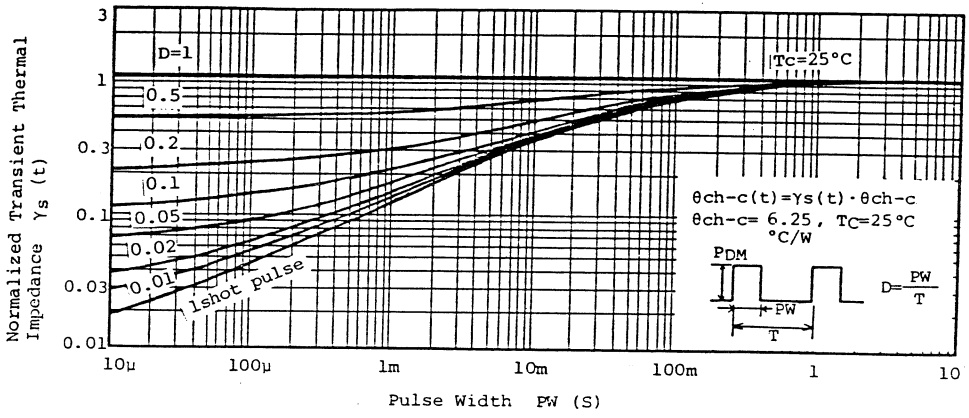
SWITCHING CHARACTERISTICS



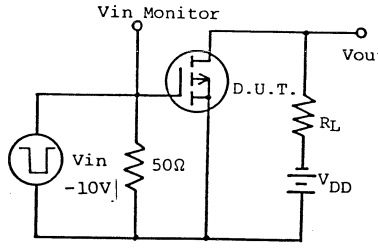
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



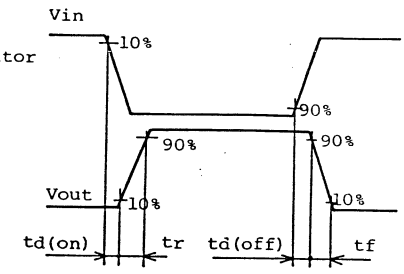
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

2SJ160, 2SJ161, 2SJ162

SILICON P-CHANNEL MOS FET

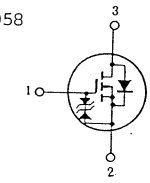
—Preliminary—

LOW FREQUENCY POWER AMPLIFIER

Complementary Pair with 2SK1056, 2SK1057, 2SK1058

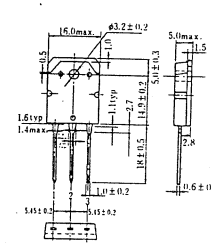
■ FEATURES

- High Power Gain.
- Excellent Frequency Response.
- High Speed Switching.
- Wide Area of Safe Operation.
- Enhancement-Mode.
- Good Complementary Characteristics.
- Equipped with Gate Protection Diodes.



1. Gate
2. Source (Flange)
3. Drain

(Dimensions in mm)



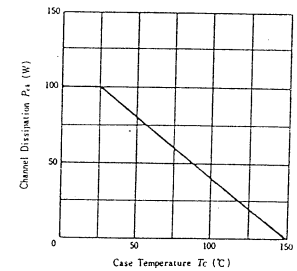
(TO-3P)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating			Unit
		2SJ160	2SJ161	2SJ162	
Drain-Source Voltage	V_{DSX}	−120	−140	−160	V
Gate-Source Voltage	V_{GSS}	±15			V
Drain Current	I_D	−7			A
Body-Drain Diode Reverse Drain Current	I_{DR}	−7			A
Channel Dissipation	P_{ch}*	100			W
Channel Temperature	T_{ch}	150			°C
Storage Temperature	T_{stg}	−55 ~ +150			°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



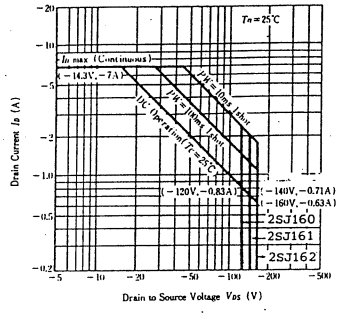
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SJ160	$V_{(BR)DSX}$	I_D=−10mA, V_{GS}=10V	−120	—	—	V
	2SJ161			−140	—	—	V
	2SJ162			−160	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	—	—	V
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=−100mA, V_{DS}=−10V	−0.15	—	−1.45	V
Drain-Source Saturation Voltage		$V_{DS(sat)}$	I_D=−7A, V_{GD}=0*	—	—	−12	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=−3A, V_{DS}=−10V*	0.7	1.0	1.4	S
Input Capacitance		C_{iss}	V_{GS}=5V, V_{DS}=−10V, f=1MHz	—	900	—	pF
Output Capacitance		C_{oss}		—	400	—	pF
Reverse Transfer Admittance		C_{rss}		—	40	—	pF
Turn-on Time		t_{on}	V_{DD}=−20V, I_D=−4A	—	230	—	ns
Turn-off Time		t_{off}		—	110	—	ns

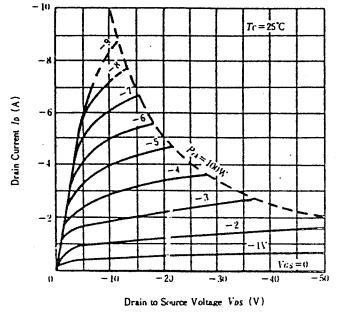
*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

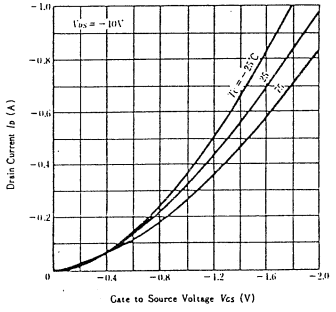
MAXIMUM SAFE OPERATION AREA



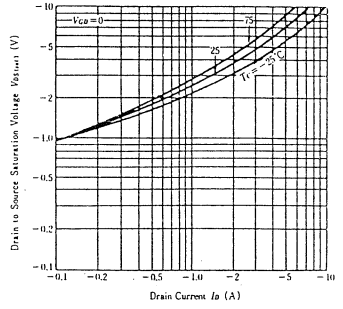
TYPICAL OUTPUT CHARACTERISTICS



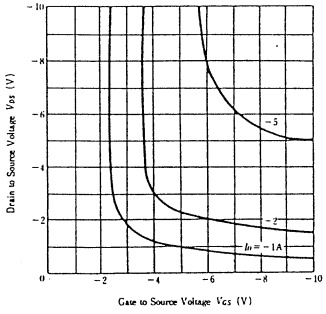
TYPICAL TRANSFER CHARACTERISTICS



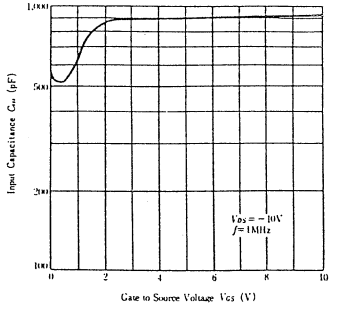
DRAIN TO SOURCE SATURATION VOLTAGE VS. DRAIN CURRENT



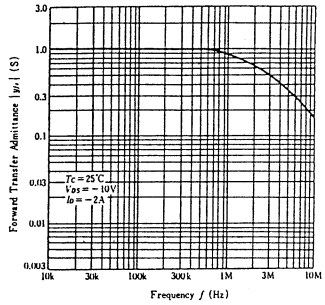
DRAIN TO SOURCE VOLTAGE VS. GATE TO SOURCE VOLTAGE



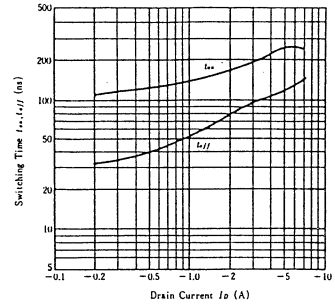
INPUT CAPACITANCE VS. GATE TO SOURCE VOLTAGE



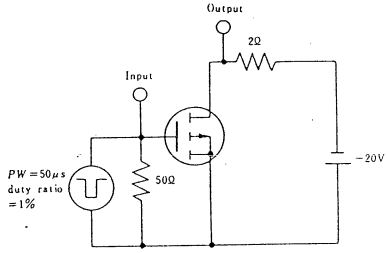
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



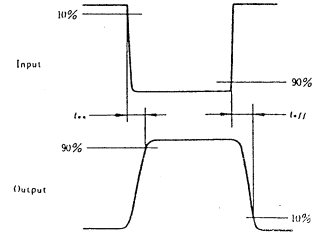
SWITCHING TIME VS. DRAIN CURRENT



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



2SK133, 2SK134, 2SK135

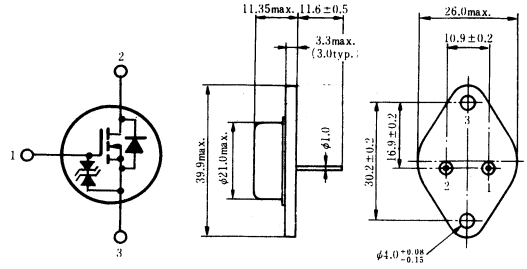
SILICON N-CHANNEL MOS FET

LOW FREQUENCY POWER AMPLIFIER

Complementary pair with 2SJ48, 2SJ49, 2SJ50

■ FEATURES

- High Power Gain.
- Excellent Frequency Response.
- High Speed Switching.
- Wide Area of Safe Operation.
- Enhancement-Mode.
- Good Complementary Characteristics.
- Equipped with Gate Protection Diodes.



1. Gate
2. Drain
3. Source (Case)

(Dimensions in mm)

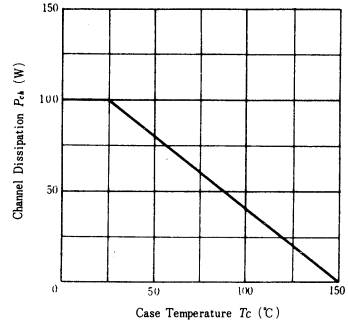
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Rating			Unit
		2SK133	2SK134	2SK135	
Drain-Source Voltage	V_{DSX}	120	140	160	V
Gate-Source Voltage	V_{GSS}	±14			V
Drain Current	I_D	7			A
Body-Drain Diode Reverse Drain Current	I_{DR}	7			A
Channel Dissipation	P_{ch}*	100			W
Channel Temperature	T_{ch}	150			°C
Storage Temperature	T_{stg}	−55 ~ +150			°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

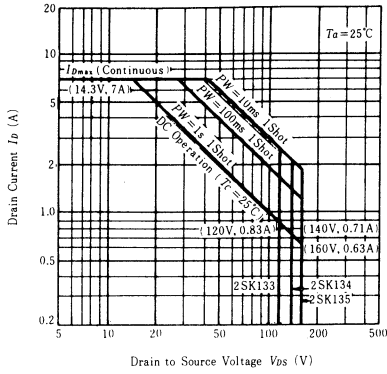


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

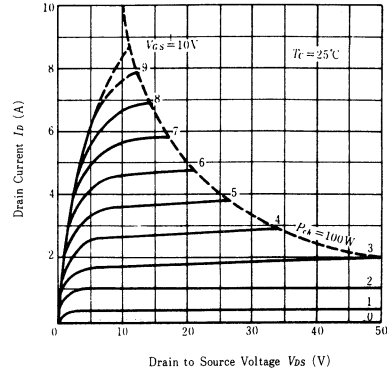
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK133	$V_{(BR)DSX}$	I_D=10mA, V_{GS}=−10V	120	—	—	V
	2SK134			140	—	—	V
	2SK135			160	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±14	—	—	V
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=100mA, V_{DS}=10V	0.15	—	1.45	V
Drain-Source Saturation Voltage		$V_{DS(sat)}$	I_D=7A, V_{GD}=0*	—	—	12	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	0.7	1.0	1.4	S
Input Capacitance		C_{iss}	V_{GS}=−5V, V_{DS}=10V, f=1MHz	—	600	—	pF
Output Capacitance		C_{oss}		—	350	—	pF
Reverse Transfer Capacitance		C_{rss}		—	10	—	pF
Turn-on Time		t_{on}	V_{DD}=20V, I_D=4A	—	180	—	ns
Turn-off Time		t_{off}		—	60	—	ns

*Pulse Test

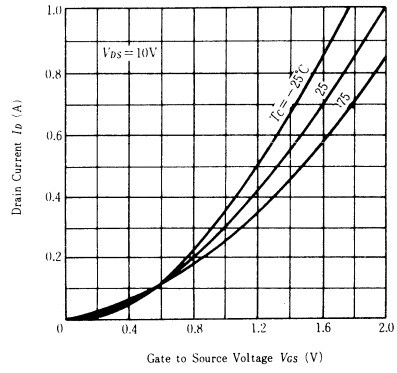
MAXIMUM SAFE OPERATION AREA



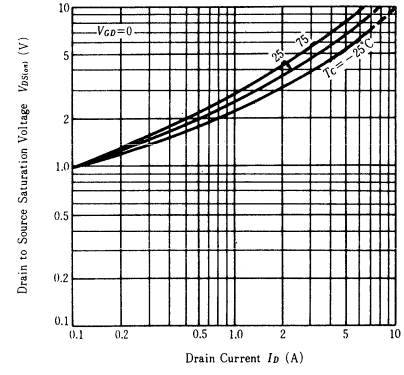
TYPICAL OUTPUT CHARACTERISTICS



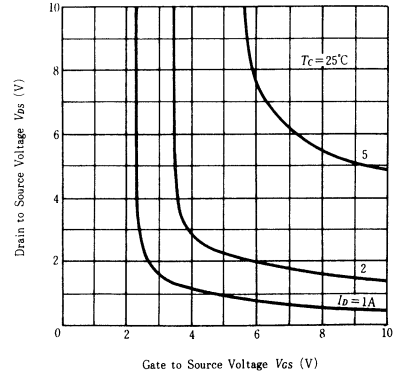
TYPICAL TRANSFER CHARACTERISTICS



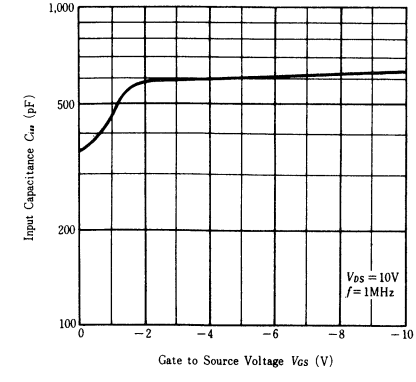
DRAIN - SOURCE SATURATION VOLTAGE VS. DRAIN CURRENT



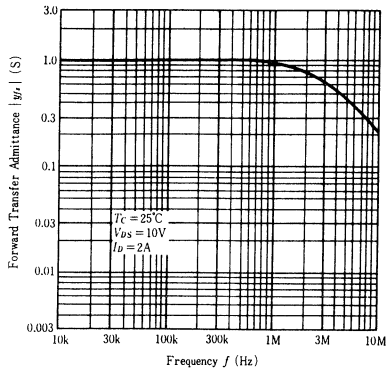
DRAIN - SOURCE VOLTAGE VS. GATE - SOURCE VOLTAGE



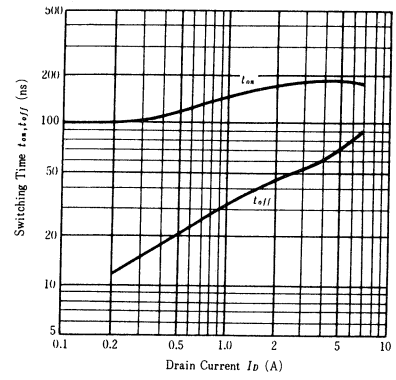
INPUT CAPACITANCE VS. GATE - SOURCE VOLTAGE



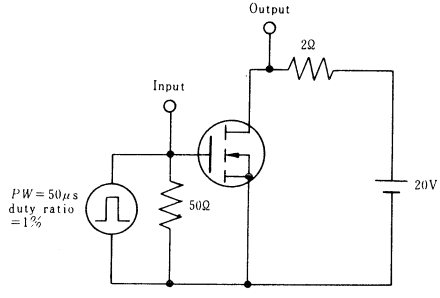
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



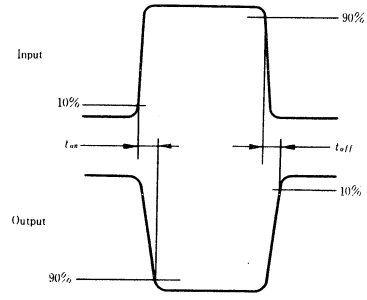
SWITCHING TIME VS. DRAIN CURRENT



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



2SK175,2SK176

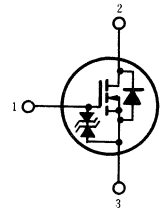
SILICON N-CHANNEL MOS FET

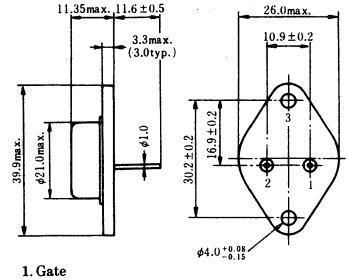
LOW FREQUENCY POWER AMPLIFIER

Complementary pair with 2SJ55, 2SJ56

■ FEATURES

- High Power Gain.
- Excellent Frequency Response.
- High Speed Switching.
- Wide Area of Safe Operation.
- Enhancement-Mode.
- Good Complementary Characteristics.
- Equipped with Gate Protection Diodes.





1. Gate
2. Drain
3. Source
(Case)

(Dimensions in mm)

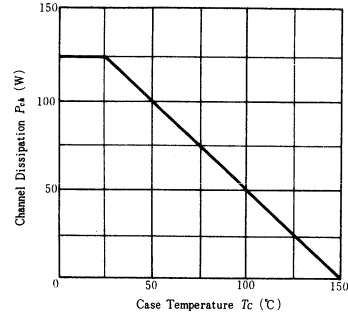
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SK175	2SK176	
Drain-Source Voltage	V_{DSX}	180	200	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	8		A
Body-Drain Diode Reverse Drain Current	I_{DR}	8		A
Channel Dissipation	P_{ch}*	125		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

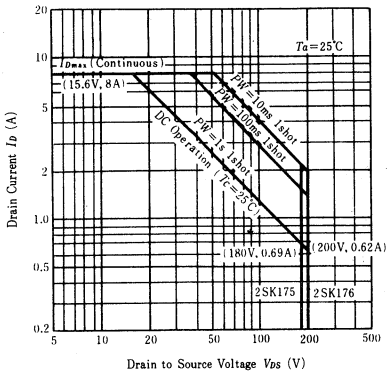


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

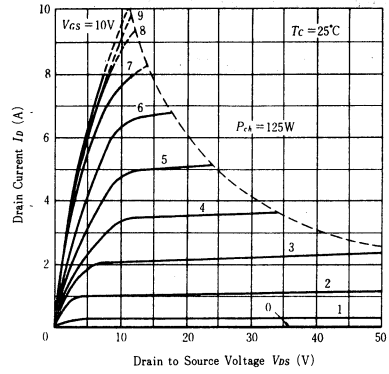
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK175	$V_{(BR)DSX}$	I_D=10mA, V_{GS}=−10V	180	—	—	V
	2SK176			200	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=100mA, V_{DS}=10V	0.15	—	1.45	V
Drain-Source Saturation Voltage		$V_{DS(sat)}$	I_D=8A, V_{GD}=0*	—	—	12	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	0.7	1.0	1.4	S
Input Capacitance		C_{iss}	V_{GS}=−5V, V_{DS}=10V, f=1MHz	—	800	—	pF
Output Capacitance		C_{oss}		—	600	—	pF
Reverse Transfer Capacitance		C_{rss}		—	15	—	pF
Turn-on Time		t_{on}	V_{DD}=30V, I_D=4A	—	250	—	ns
Turn-off Time		t_{off}		—	90	—	ns

*Pulse Test

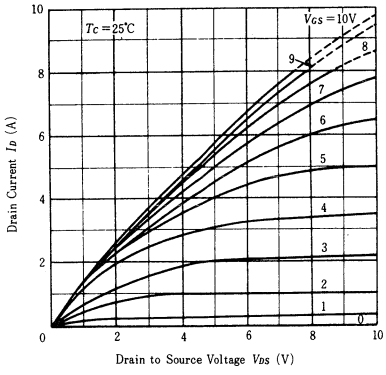
MAXIMUM SAFE OPERATION AREA



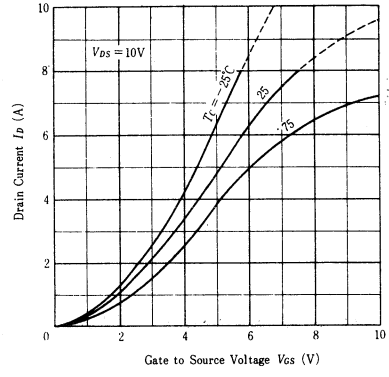
TYPICAL OUTPUT CHARACTERISTICS



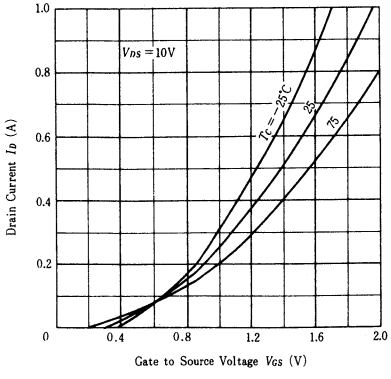
TYPICAL OUTPUT CHARACTERISTICS



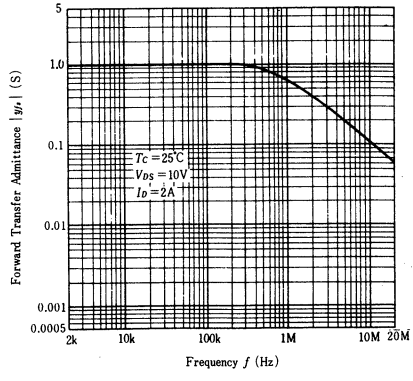
TYPICAL TRANSFER CHARACTERISTICS



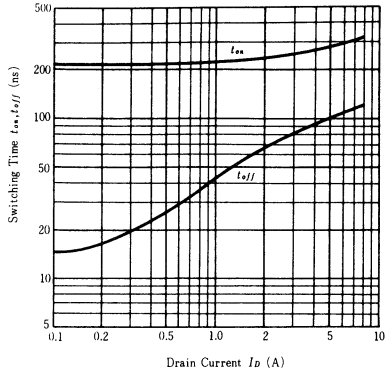
TYPICAL TRANSFER CHARACTERISTICS



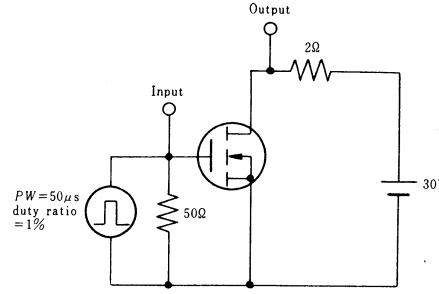
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME VS. DRAIN CURRENT

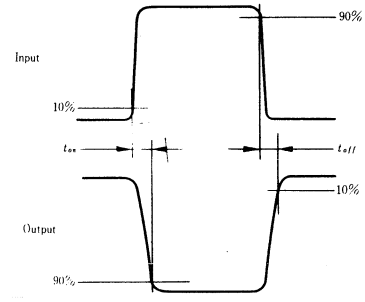


SWITCHING TIME TEST CIRCUIT



応 答 波 形
RESPONSE WAVEFORM

WAVEFORMS



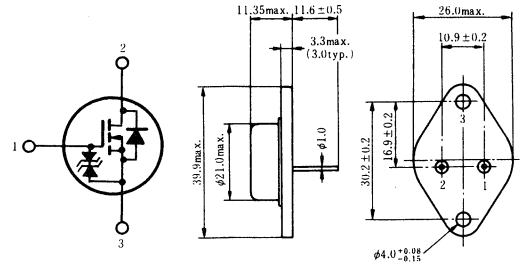
2SK176(H)

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- High Speed Switching.
- High Cutoff Frequency.
- Enhancement-Mode.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2. Drain
3. Source (Case)

(Dimensions in mm)

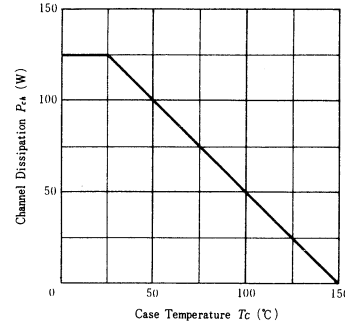
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	200	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Body-Drain Diode Reverse Drain Current	I_{DR}	8	A
Channel Dissipation	P_{ch}*	125	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

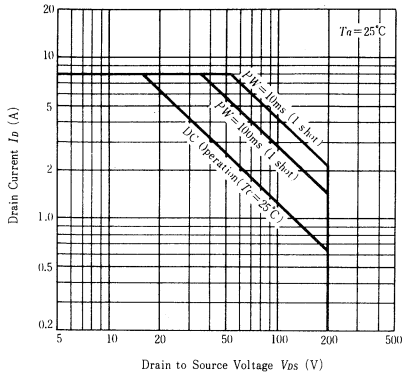


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

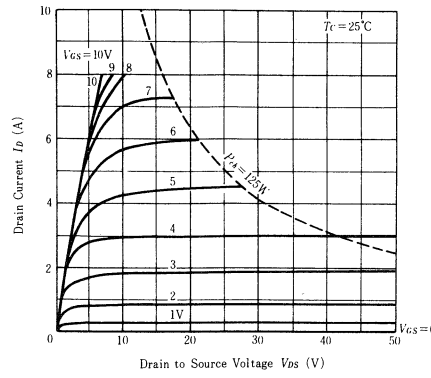
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	200	—	—	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=160V, V_{GS}=0	—	—	3.0	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=100mA, V_{DS}=10V	0.55	—	3.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=4A, V_{GS}=15V*	—	1.0	1.5	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=4A, V_{GS}=15V*	—	—	6.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	0.7	—	1.4	S
Input Capacitance	C_{iss}	V_{GS}=−5V, V_{DS}=10V, f=1MHz	—	800	—	pF
Output Capacitance	C_{oss}		—	600	—	pF
Turn-on Time	t_{on}	I_D=2A, V_{GS}=15V, R_L=15Ω	—	60	—	ns
Turn-off Time	$t_{d(off)}$		—	200	—	ns

*Pulse Test

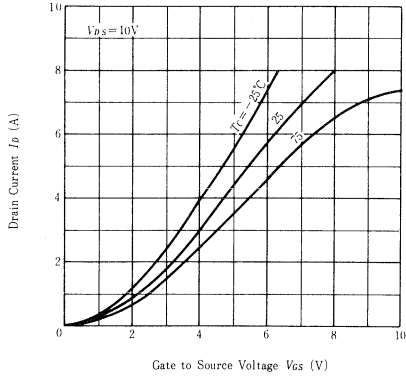
MAXIMUM SAFE OPERATION AREA



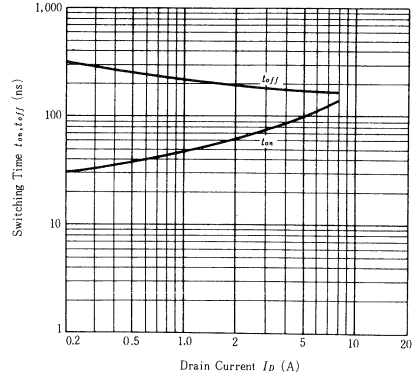
TYPICAL OUTPUT CHARACTERISTICS



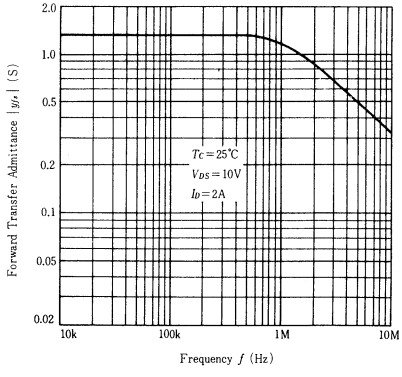
TYPICAL TRANSFER CHARACTERISTICS



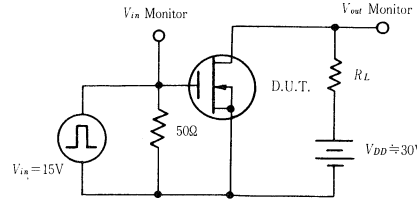
SWITCHING TIME VS. DRAIN CURRENT



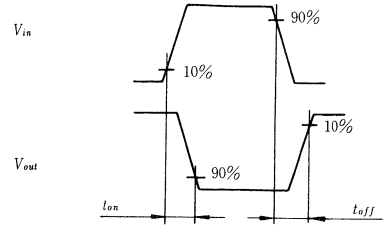
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



WAVEFORMS

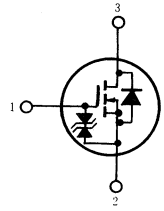


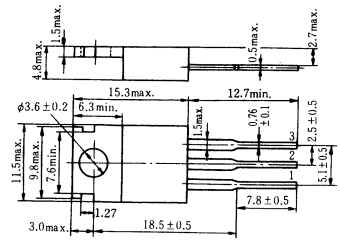
2SK213, 2SK214, 2SK215, 2SK216

SILICON N-CHANNEL MOS FET

HIGH FREQUENCY AND LOW FREQUENCY POWER AMPLIFIER, HIGH SPEED SWITCHING

Complementary Pair with 2SJ76, J77, J78, J79





1. Gate
2. Source (Flange)
3. Drain

(Dimensions in mm)

(JEDEC TO-220AB)

■ FEATURES

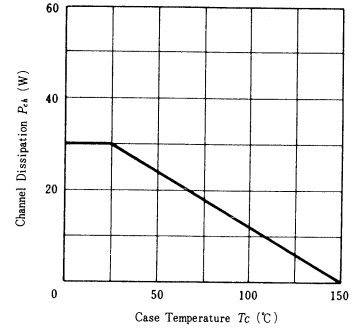
- Suitable for Direct Mounting.
- High Forward Transfer Admittance.
- Excellent Frequency Response.
- Enhancement-Mode.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Ratings				Unit
		2SK213	2SK214	2SK215	2SK216	
Drain-Source Voltage	V_{DSX}	140	160	180	200	V
Gate-Source Voltage	V_{GSS}	±15				V
Drain Current	I_D	500				mA
Body-Drain Diode Reverse Drain Current	I_{DR}	500				mA
Channel Dissipation	P_{ch}	1.75				W
	P_{ch}*	30				W
Channel Temperature	T_{ch}	150				°C
Storage Temperature	T_{stg}	−45 ~ +150				°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

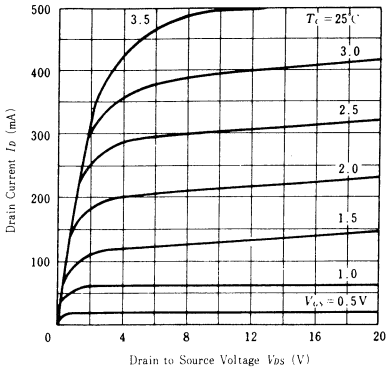


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

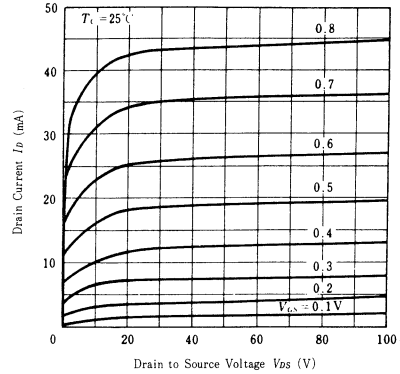
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK213	$V_{(BR)DSX}$	I_D=1mA, V_{GS}=−2V	140	—	—	V
	2SK214			160	—	—	V
	2SK215			180	—	—	V
	2SK216			200	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±10μA, V_{DS}=0	±15	—	—	V
Gate-Source Voltage		$V_{GS(on)}$	I_D=10mA, V_{DS}=10V*	0.2	—	1.5	V
Drain-Source Saturation Voltage		$V_{DS(sat)}$	I_D=10mA, V_{GD}=0*	—	—	2.0	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=10mA, V_{DS}=20V*	20	40	—	mS
Input Capacitance		C_{iss}	I_D=10mA, V_{DS}=10V, f=1MHz	—	90	—	pF
Reverse Transfer Capacitance		C_{rss}		—	2.2	—	pF

*Pulse Test

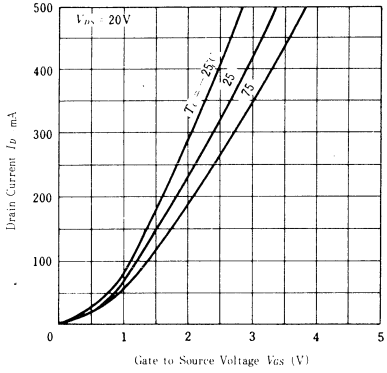
TYPICAL OUTPUT CHARACTERISTICS



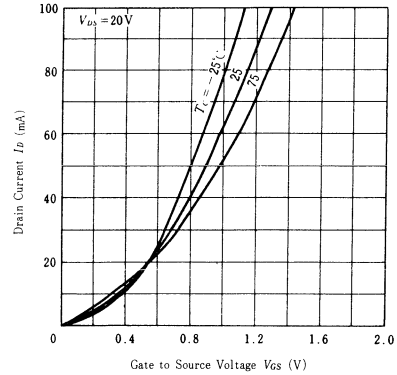
TYPICAL OUTPUT CHARACTERISTICS



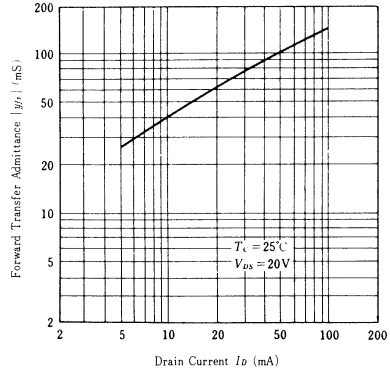
TYPICAL TRANSFER CHARACTERISTICS



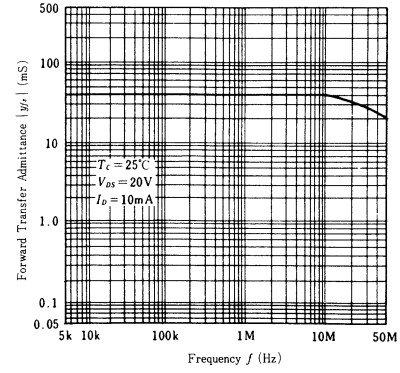
TYPICAL TRANSFER CHARACTERISTICS



FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



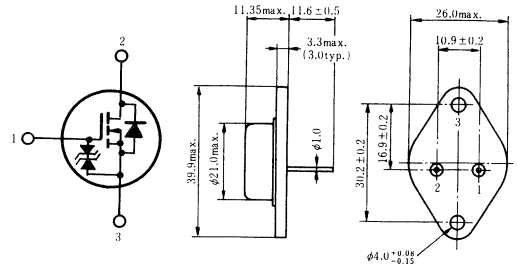
2SK220Ⓗ, 2SK221Ⓗ

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- High Speed Switching.
- High Cutoff Frequency.
- Enhancement-Mode.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2. Drain
3. Source (Case)

(Dimensions in mm)

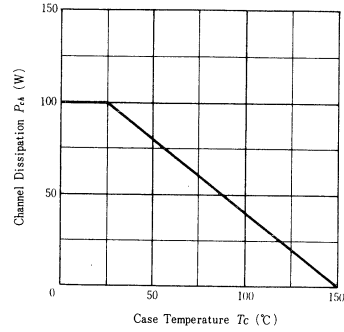
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SK220Ⓗ	2SK221Ⓗ	
Drain-Source Voltage	V_{DSS}	160	200	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	8		A
Body-Drain Diode Reverse Drain Current	I_{DR}	8		A
Channel Dissipation	P_{ch}*	100		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−65 ~ +150		°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

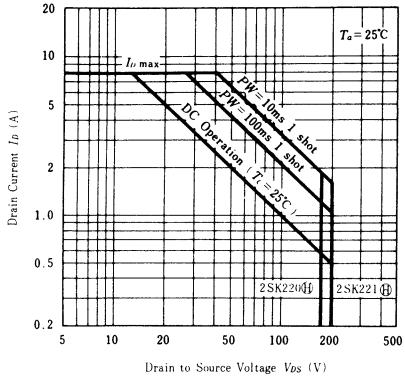


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

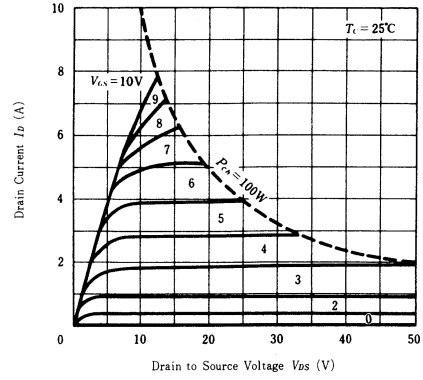
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK220Ⓗ	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	160	—	—	V
	2SK221Ⓗ			200	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Zero Gate Voltage Drain Current	2SK220Ⓗ	I_{DSS}	V_{DS}=120V, V_{GS}=0	—	—	1.0	mA
	2SK221Ⓗ		V_{DS}=160V V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=100mA, V_{DS}=10V	0.4	—	3.0	V
Static Drain-Source On State Resistance		$R_{DS(on)}$	I_D=4A, V_{GS}=15V*	—	1.0	1.5	Ω
Drain-Source Saturation Voltage		$V_{DS(on)}$	I_D=4A, V_{GS}=15V*	—	—	6.0	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	0.6	0.9	—	S
Input Capacitance		C_{iss}	V_{GS}=−5V, V_{DS}=10V, f=1MHz	—	600	—	pF
Output Capacitance		C_{oss}		—	300	—	pF
Turn-on Time		t_{on}	I_D=2A, V_{GS}=15V	—	25	—	ns
Turn-off Time		t_{off}		—	45	—	ns

*Pulse Test

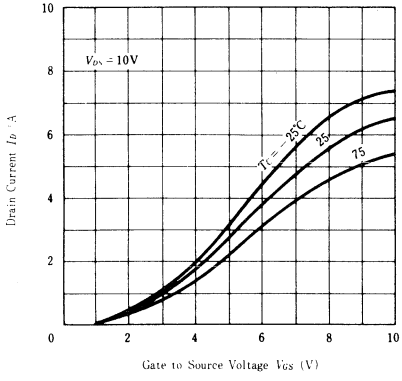
MAXIMUM SAFE OPERATION AREA



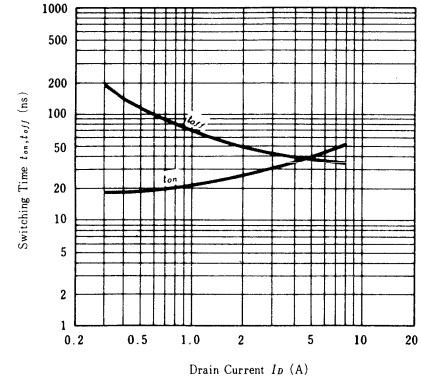
TYPICAL OUTPUT CHARACTERISTICS



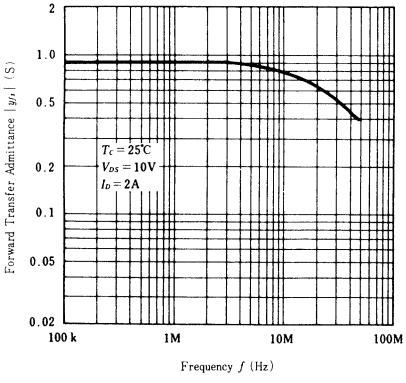
TYPICAL TRANSFER CHARACTERISTICS



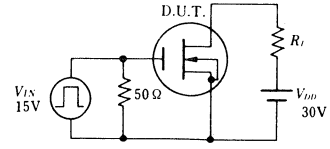
SWITCHING TIME VS. DRAIN CURRENT



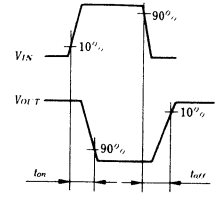
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



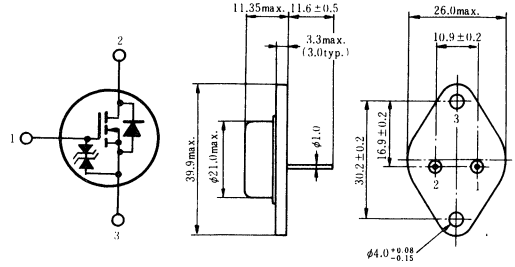
2SK258(H)

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- High Speed Switching.
- High Cutoff Frequency.
- Enhancement-Mode.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2. Drain
3. Source (Case)

(Dimensions in mm)

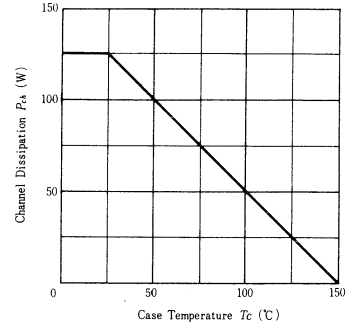
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	250	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Body-Drain Diode Reverse Drain Current	I_{DR}	8	A
Channel Dissipation	P_{ch}*	125	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

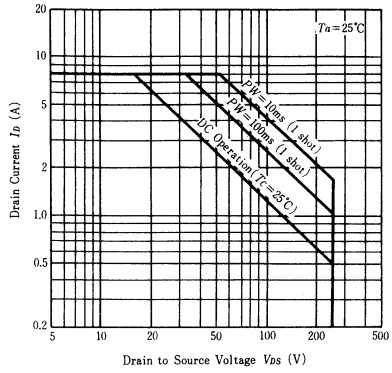


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

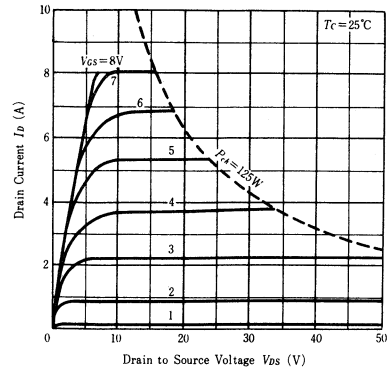
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	250	—	—	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=200V, V_{GS}=0	—	—	1.0	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=10mA, V_{DS}=10V	0.4	—	3.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=4A, V_{GS}=15V*	—	0.8	1.12	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=4A, V_{GS}=15V*	—	—	4.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	0.9	1.3	—	S
Input Capacitance	C_{iss}	V_{GS}=−5V, V_{DS}=10V, f=1MHz	—	800	—	pF
Output Capacitance	C_{oss}		—	350	—	pF
Turn-on Time	t_{on}	I_D=2A, V_{GS}=15V	—	25	—	ns
Turn-off Time	t_{off}		—	140	—	ns

*Pulse Test

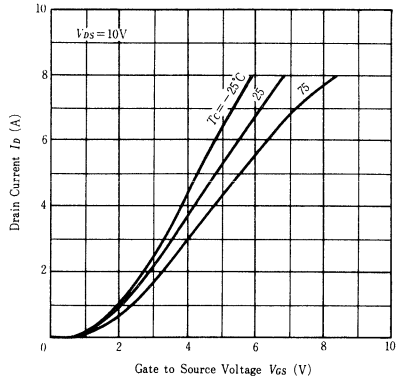
MAXIMUM SAFE OPERATION AREA



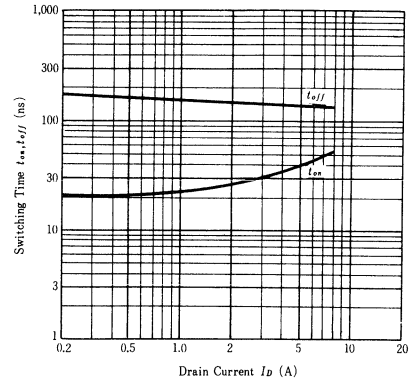
TYPICAL OUTPUT CHARACTERISTICS



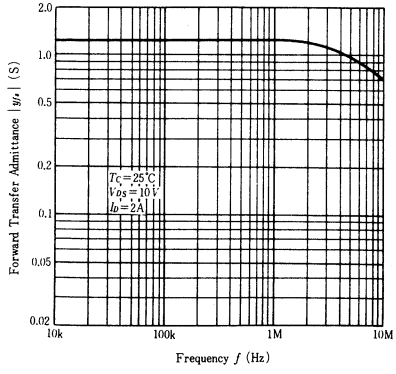
TYPICAL TRANSFER CHARACTERISTICS



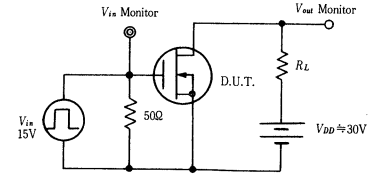
SWITCHING TIME VS. DRAIN CURRENT



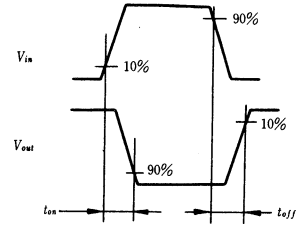
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



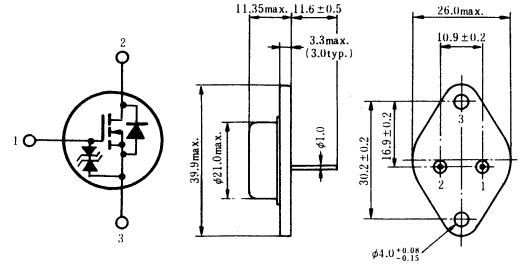
2SK259Ⓗ,2SK260Ⓗ

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- High Speed Switching.
- High Cutoff Frequency.
- High Breakdown Voltage.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2. Drain
3. Source (Case)

(Dimensions in mm)

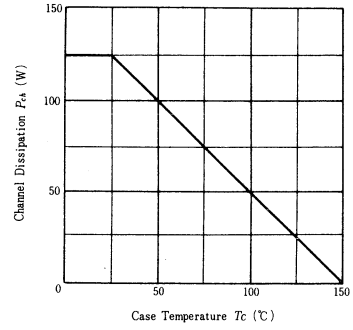
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SK259Ⓗ	2SK260Ⓗ	
Drain-Source Voltage	V_{DSS}	350	400	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	5		A
Drain Peak Current	$I_{D(peak)}$	10		A
Body-Drain Diode Reverse Drain Current	I_{DR}	5		A
Channel Dissipation	P_{ch}*	125		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−65 ~ +150		°C

*Value at T_c=25 °C

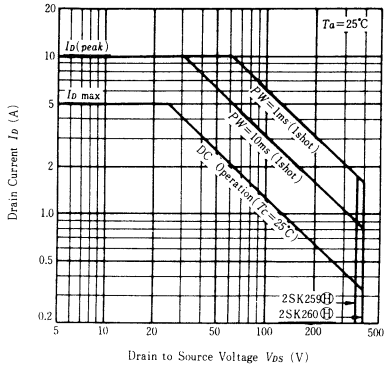
POWER VS. TEMPERATURE DERATING



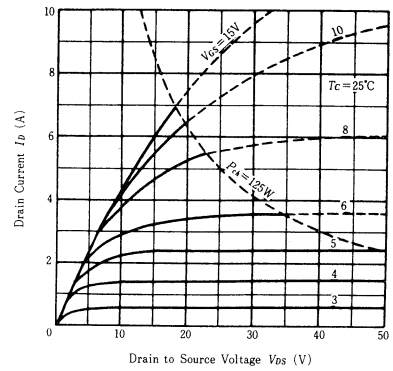
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK259Ⓗ	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	350	—	—	V
	2SK260Ⓗ			400	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Zero Gate Voltage Drain Current	2SK259Ⓗ	I_{DSS}	V_{DS}=280V, V_{GS}=0	—	—	1.0	mA
	2SK260Ⓗ		V_{DS}=320V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=10mA, V_{DS}=10V	0.4	—	3.0	V
Static Drain-Source On State Resistance		$R_{DS(on)}$	I_D=3A, V_{GS}=15V*	—	2.5	3.0	Ω
Drain-Source Saturation Voltage		$V_{DS(on)}$	I_D=3A, V_{GS}=15V*	—	7.5	9.5	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=3A, V_{DS}=20V*	0.6	1.0	—	S
Input Capacitance		C_{iss}	V_{GS}=−5V, V_{DS}=10V, f=1MHz	—	800	—	pF
Output Capacitance		C_{oss}		—	350	—	pF
Reverse Transfer Capacitance		C_{rss}	V_{GD}=−5V, f=1MHz	—	15	—	pF
Turn-on Time		t_{on}	I_D=2A, V_{GS}=15V	—	25	—	ns
Turn-off Time		t_{off}		—	140	—	ns

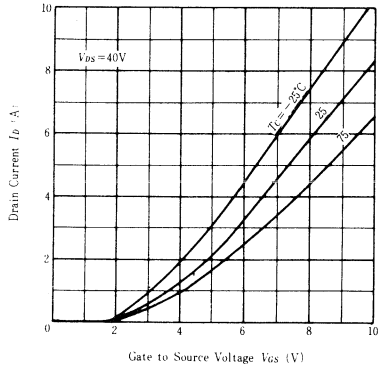
MAXIMUM SAFE OPERATION AREA



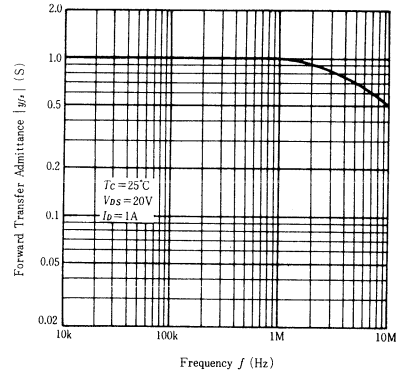
TYPICAL OUTPUT CHARACTERISTICS



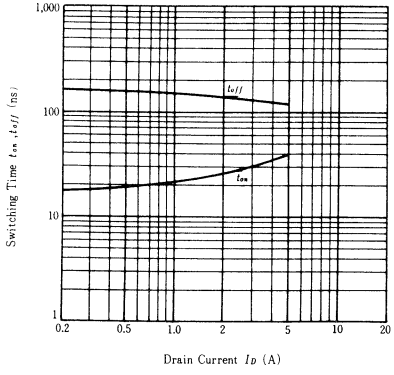
TYPICAL TRANSFER CHARACTERISTICS



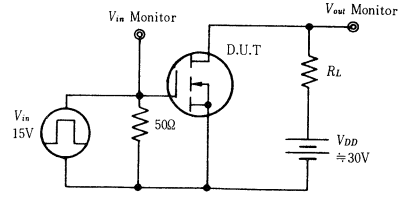
SWITCHING TIME VS. DRAIN CURRENT



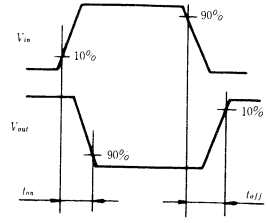
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



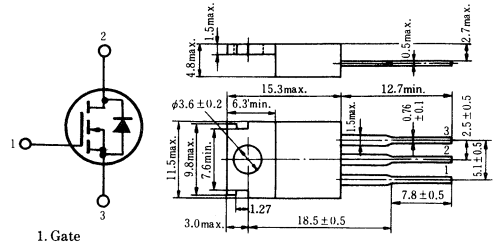
2SK294,2SK295

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

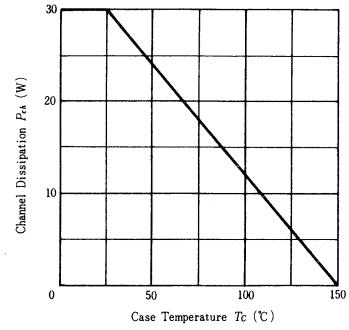
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SK294	2SK295	
Drain-Source Voltage	V_{DSS}	80	100	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	5		A
Drain Peak Current	$I_{D(peak)}$	10		A
Body-Drain Diode Reverse Drain Current	I_{DR}	5		A
Channel Dissipation	P_{ch}*	30		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

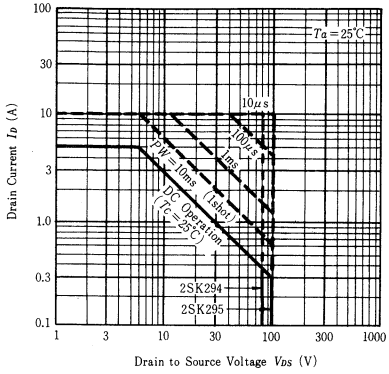


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

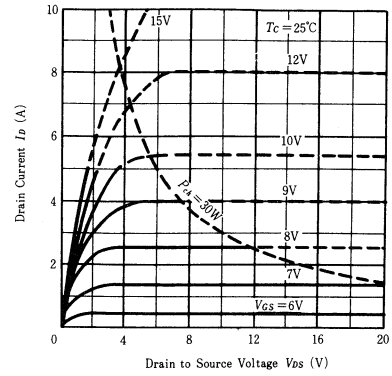
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK294	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	80	—	—	V
	2SK295			100	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	2SK294	I_{DSS}	V_{DS}=65V, V_{GS}=0	—	—	1	mA
	2SK295		V_{DS}=80V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	5.0	V
Static Drain-Source on State Resistance		$R_{DS(on)}$	I_D=3A, V_{GS}=15V*	—	0.4	0.56	Ω
Drain-Source Saturation Voltage		$V_{DS(on)}$	I_D=3A, V_{GS}=15V*	—	1.2	1.7	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	0.5	0.8	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	450	—	pF
Output Capacitance		C_{oss}		—	270	—	pF
Reverse Transfer Capacitance		C_{rss}		—	140	—	pF
Turn-On Delay Time		$t_{d(on)}$	I_D=2A, V_{GS}=15V, R_L=15Ω	—	12	—	ns
Rise Time		t_r		—	28	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	35	—	ns
Fall Time		t_f		—	35	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=3A, V_{GS}=0	—	1.0	—	V
Body-Drain Reverse Recovery Time		t_{rr}	I_F=3A, V_{GS}=0, di_F/dt=50A/μs	—	200	—	ns

*Pulse Test

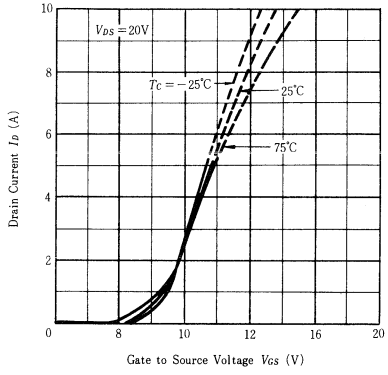
MAXIMUM SAFE OPERATION AREA



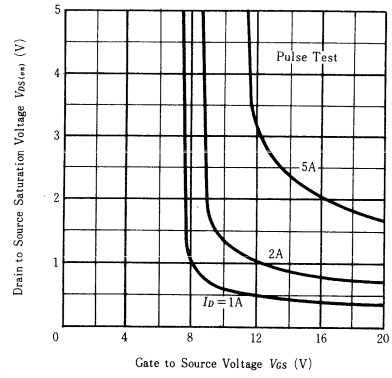
TYPICAL OUTPUT CHARACTERISTICS



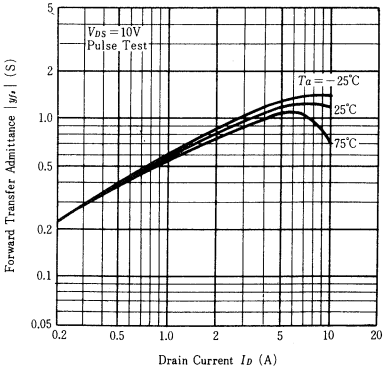
TYPICAL TRANSFER CHARACTERISTICS



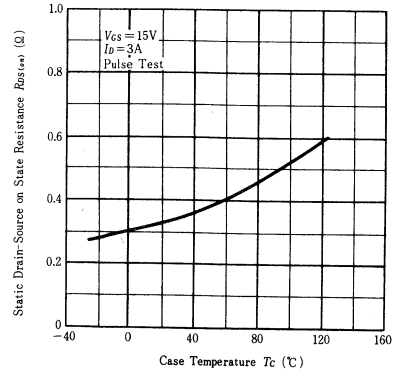
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



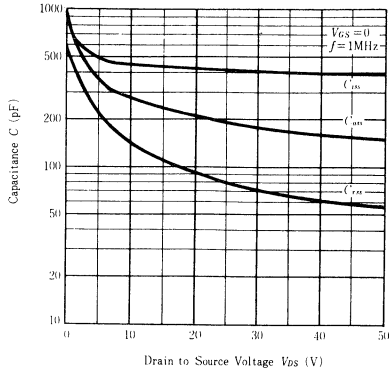
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



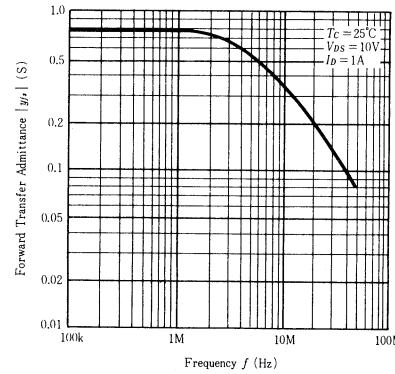
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



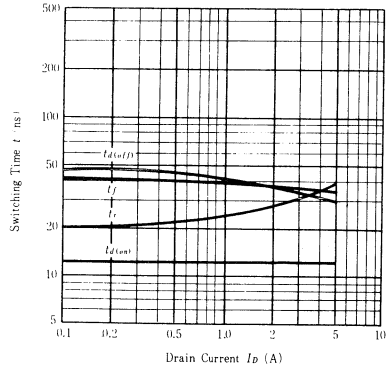
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



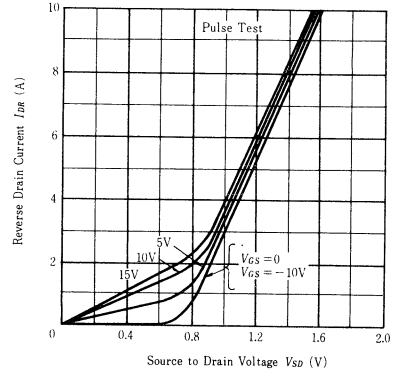
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



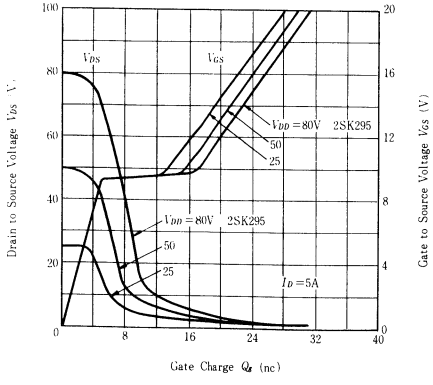
SWITCHING CHARACTERISTICS



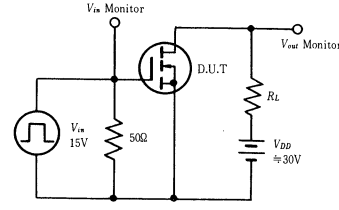
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



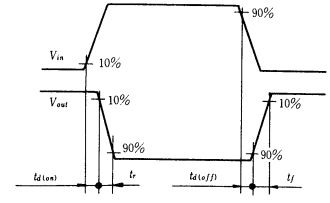
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



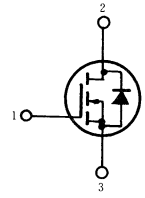
WAVEFORMS

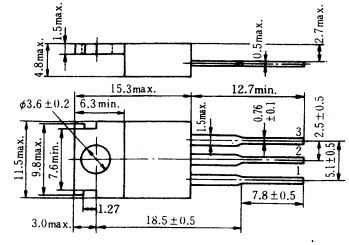


2SK296

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

(JEDEC TO-220AB)

■ FEATURES

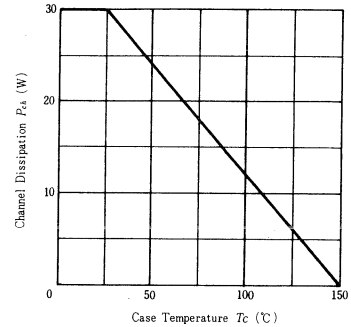
- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	300	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	1	A
Drain Peak Current	$I_{D(peak)}$	2	A
Body-Drain Diode Reverse Drain Current	I_{DR}	1	A
Channel Dissipation	P_{ch}*	30	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

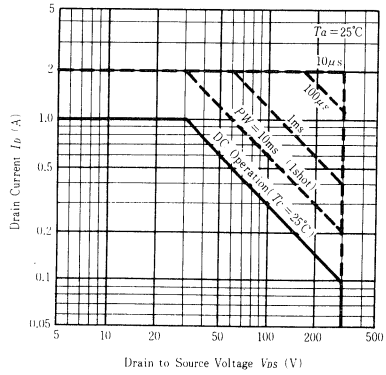


■ ELECTRICAL CHARACTERISTICS (T_a=25°C)

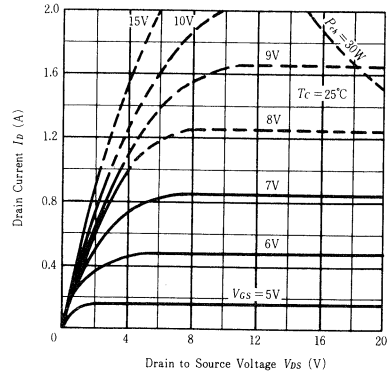
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	300	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=240V, V_{DS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	4.5	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=1A, V_{GS}=15V*	—	2.5	4.0	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=1A, V_{GS}=15V*	—	2.5	4.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=0.5A, V_{DS}=10V*	0.2	0.4	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	140	—	pF
Output Capacitance	C_{oss}		—	65	—	pF
Reverse Transfer Capacitance	C_{rss}		—	23	—	pF
Turn-on Time	$t_{d(on)}$	I_D=0.5A, V_{GS}=15V R_L=60Ω	—	6	—	ns
Rise Time	t_r		—	14	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	40	—	ns
Fall Time	t_f		—	30	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=1A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=1A, V_{GS}=0 di_F/dt=100A/μs	—	250	—	ns

*Pulse Test

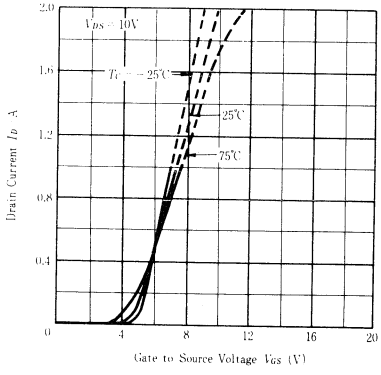
MAXIMUM SAFE OPERATION AREA



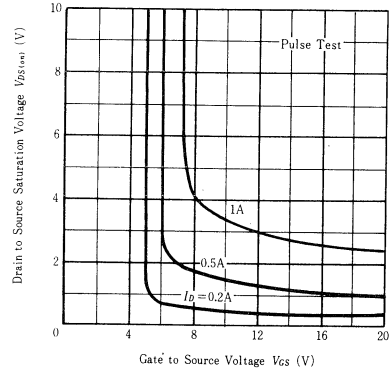
TYPICAL OUTPUT CHARACTERISTICS



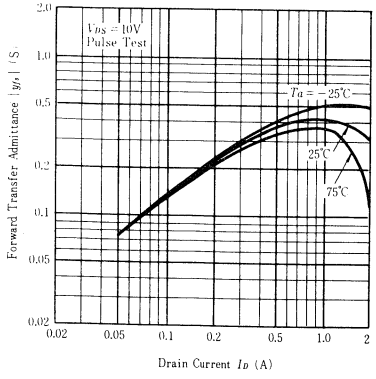
TYPICAL TRANSFER CHARACTERISTICS



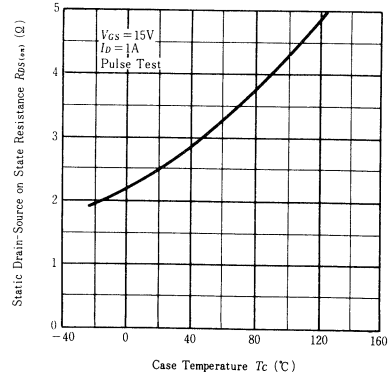
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



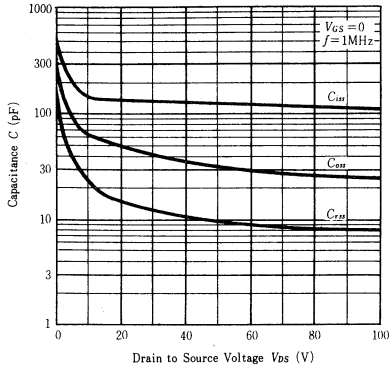
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



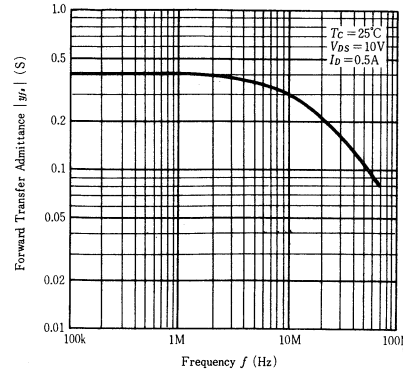
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



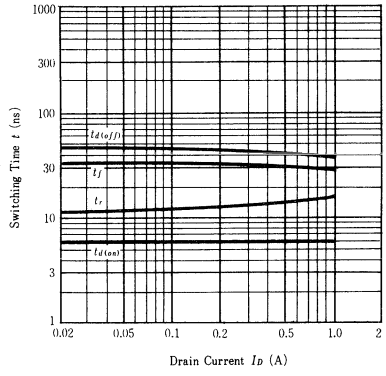
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



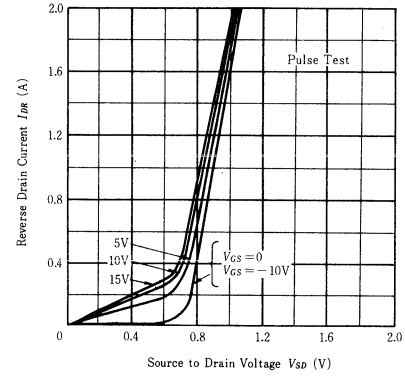
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



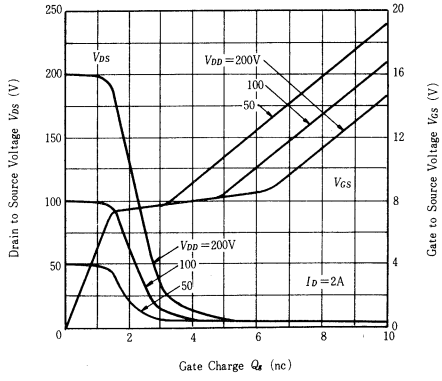
SWITCHING CHARACTERISTICS



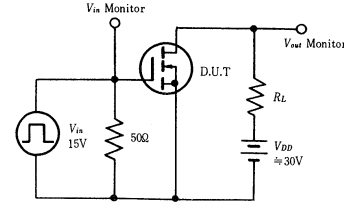
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



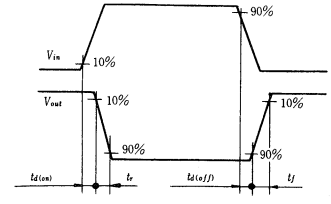
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



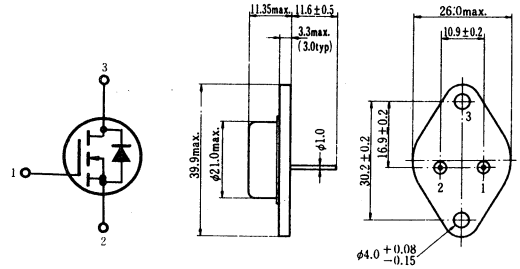
2SK298,2SK299

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2. Source
3. Drain (Case)

(Dimensions in mm)

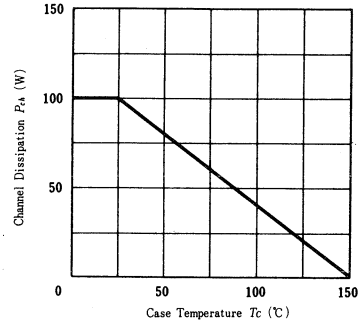
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SK298	2SK299	
Drain-Source Voltage	V_{DSS}	400	450	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	8		A
Drain Peak Current	$I_{D(peak)}$	12		A
Body-Drain Diode Reverse Drain Current	I_{DR}	8		A
Channel Dissipation	P_{ch}*	100		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING



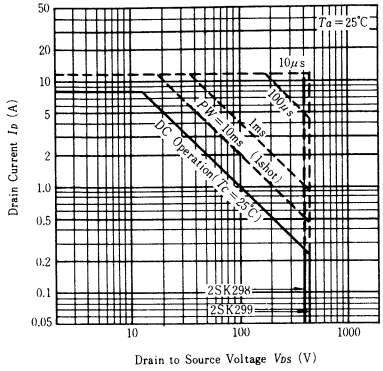
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK298	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	400	—	—	V
	2SK299			450	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	2SK298	I_{DSS}	V_{DS}=320V, V_{GS}=0	—	—	1	mA
	2SK299		V_{DS}=360V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	5.0	V
Static Drain-Source On State Resistance		$R_{DS(on)}$	I_D=4A, V_{GS}=15V*	—	1.1	1.75	Ω
Drain-Source Saturation Voltage		$V_{DS(on)}$	I_D=4A, V_{GS}=15V*	—	4.4	7.0	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=4A, V_{DS}=10V*	1.2	1.7	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	800	—	pF
Output Capacitance		C_{oss}		—	180	—	pF
Reverse Transfer Capacitance		C_{rss}		—	20	—	pF
Turn-on Time		$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	15	—	ns
Rise Time		t_r		—	35	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	85	—	ns
Fall Time		t_f		—	35	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=4A, V_{GS}=0	—	0.85	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=4A, V_{GS}=0 di_F/dt=100A/μs	—	400	—	ns

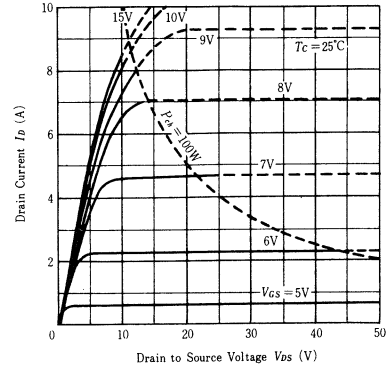
*Pulse Test

HITACHI

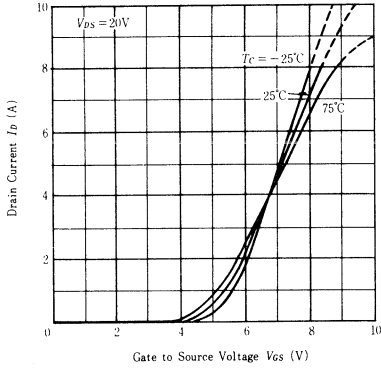
MAXIMUM SAFE OPERATION AREA



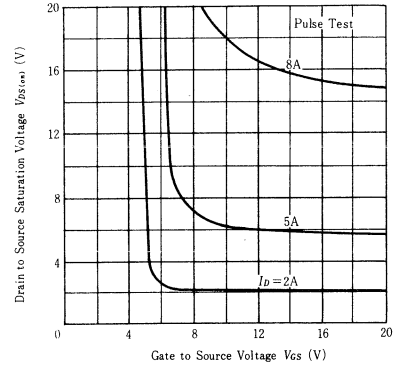
TYPICAL OUTPUT CHARACTERISTICS



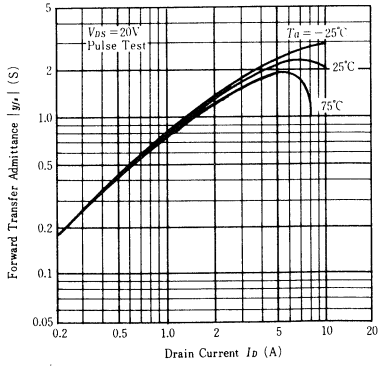
TYPICAL TRANSFER CHARACTERISTICS



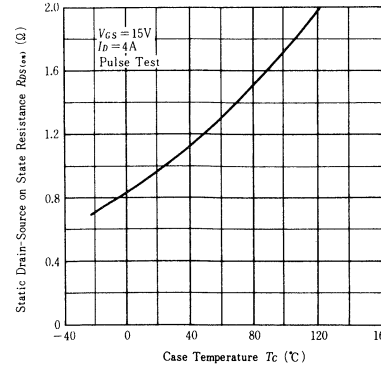
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



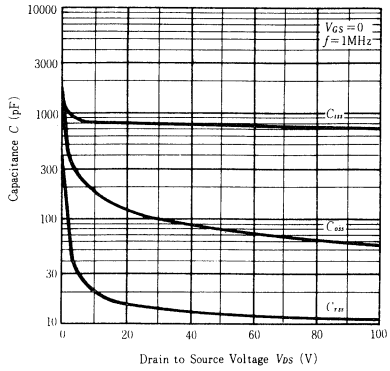
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



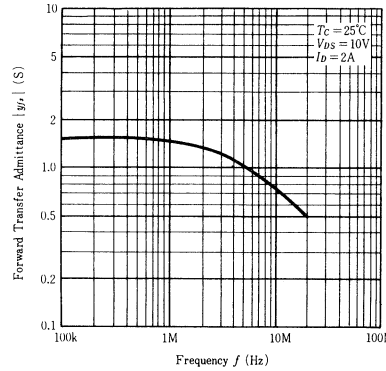
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



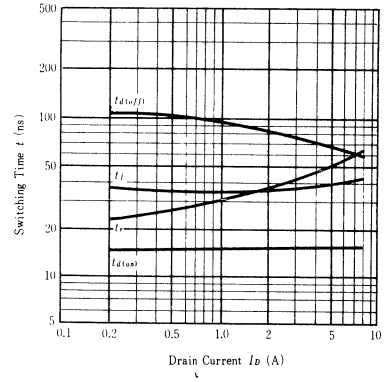
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



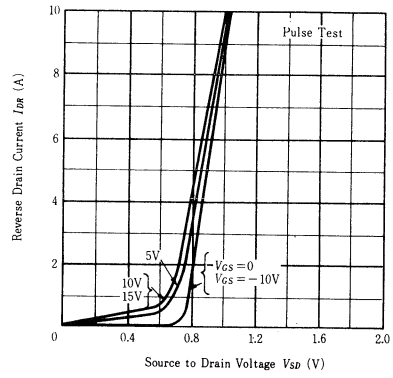
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



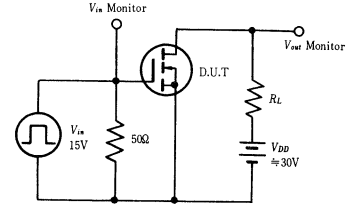
SWITCHING CHARACTERISTICS



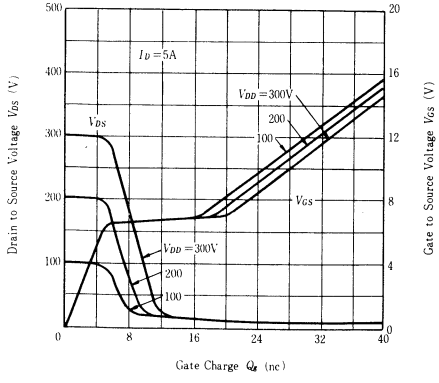
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



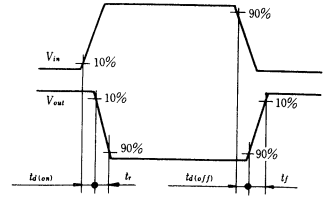
SWITCHING TIME TEST CIRCUIT



DYNAMIC INPUT CHARACTERISTICS



WAVEFORMS



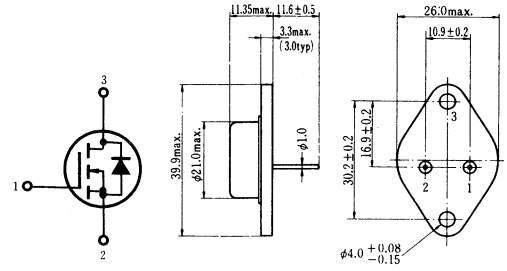
2SK308

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2. Source
3. Drain (Case)

(JEDEC TO-3)

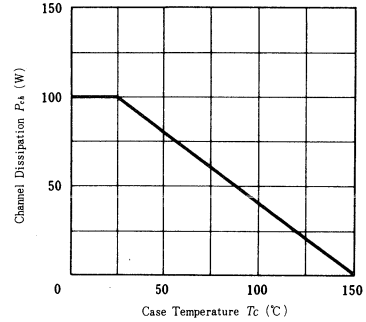
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	120	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	10	A
Drain Peak Current	$I_{D(peak)}$	15	A
Body-Drain Diode Reverse Drain Current	I_{DR}	10	A
Channel Dissipation	P_{ch}*	100	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

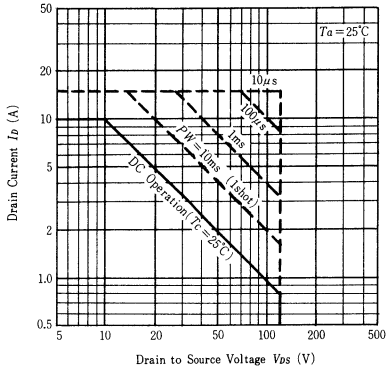


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

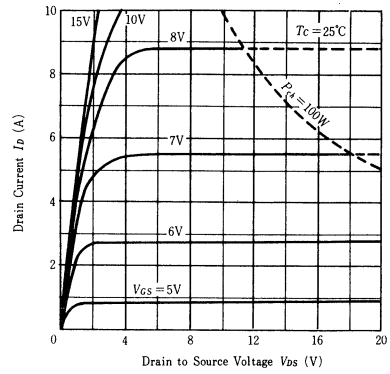
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	120	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	4.5	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	0.2	0.3	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	1.0	1.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=5A, V_{DS}=10V*	1.5	2.8	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	1130	—	pF
Output Capacitance	C_{oss}		—	650	—	pF
Reverse Transfer Capacitance	C_{rss}		—	80	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	10	—	ns
Rise Time	t_r		—	50	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	90	—	ns
Fall Time	t_f		—	70	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=5A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=5A, V_{GS}=0 di_F/dt=100A/μs	—	200	—	ns

*Pulse Test

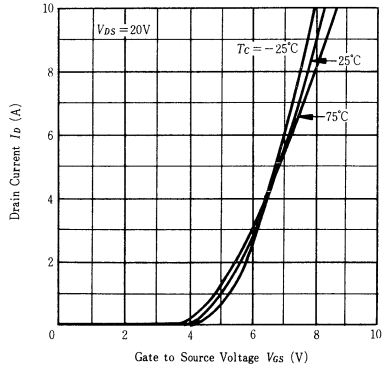
MAXIMUM SAFE OPERATION AREA



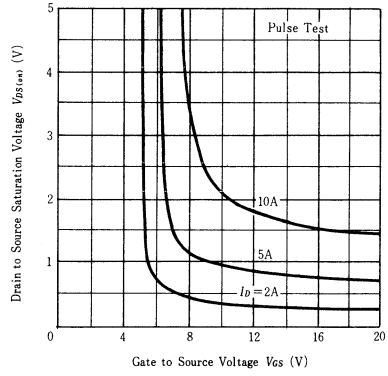
TYPICAL OUTPUT CHARACTERISTICS



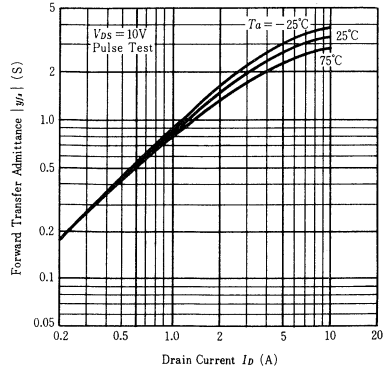
TYPICAL TRANSFER CHARACTERISTICS



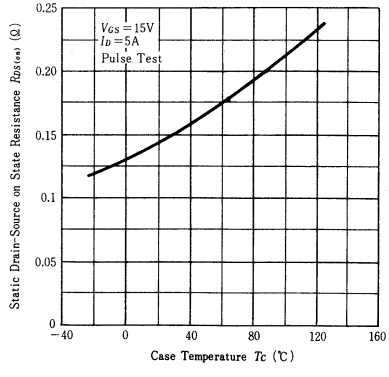
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



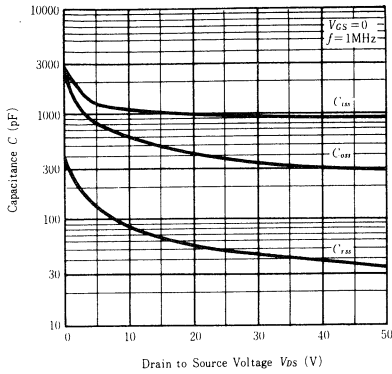
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



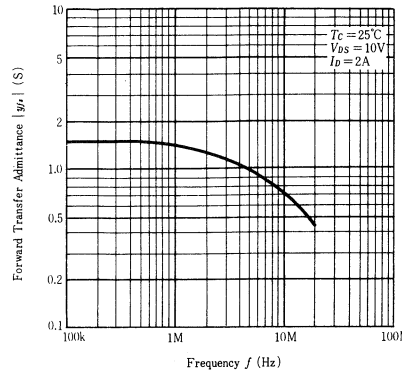
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



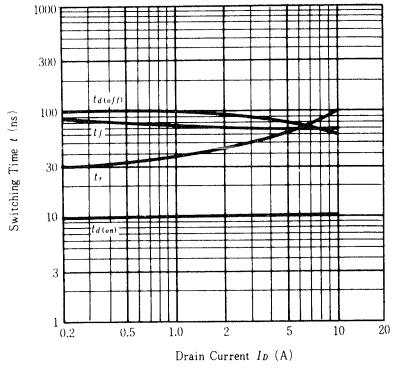
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



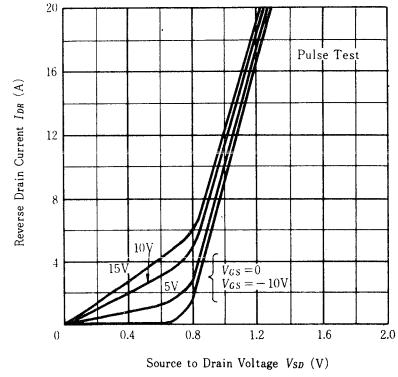
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



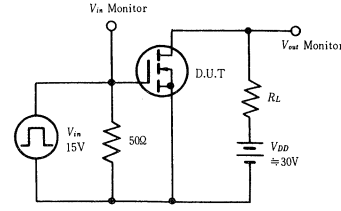
SWITCHING CHARACTERISTICS



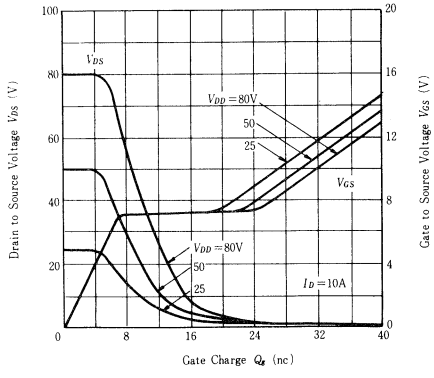
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



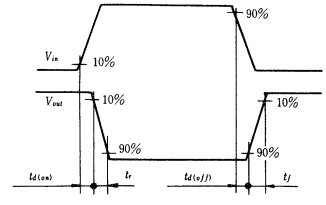
SWITCHING TIME TEST CIRCUIT



DYNAMIC INPUT CHARACTERISTICS



WAVEFORMS



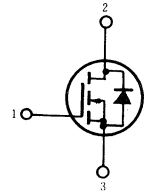
2SK310, 2SK311

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

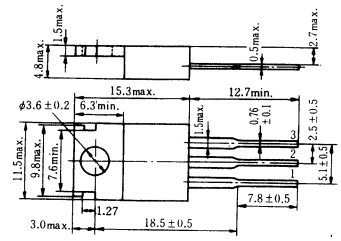
■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)



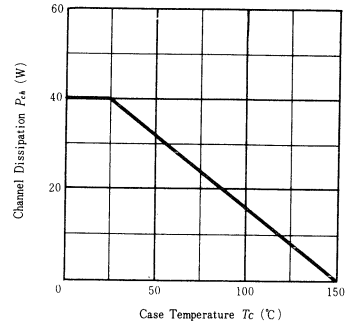
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SK310	2SK311	
Drain-Source Voltage	V_{DSS}	400	450	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	3		A
Drain Peak Current	$I_{D(peak)}$	6		A
Body-Drain Diode Reverse Drain Current	I_{DR}	3		A
Channel Dissipation	P_{ch}*	40		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



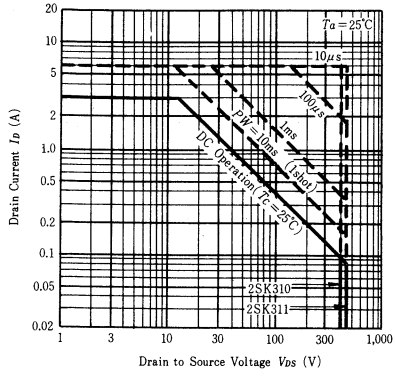
■ ELECTRICAL CHARACTERISTICS (T_a=25° C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK310	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	400	—	—	V
	2SK311			450	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	2SK310	I_{DSS}	V_{DS}=320V, V_{GS}=0	—	—	1	mA
	2SK311		V_{DS}=360V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	5.0	V
Static Drain-Source On State Resistance		$R_{DS(on)}$	I_D=2A, V_{GS}=15V*	—	2.5	4.0	Ω
Drain-Source Saturation Voltage		$V_{DS(on)}$	I_D=2A, V_{GS}=15V*	—	5.0	8.0	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=2A, V_{DS}=10V*	0.6	1.0	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	440	—	pF
Output Capacitance		C_{oss}		—	95	—	pF
Reverse Transfer Capacitance		C_{rss}		—	13	—	pF
Turn-on Delay Time		$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	9	—	ns
Rise Time		t_r		—	16	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	40	—	ns
Fall Time		t_f		—	30	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=2A, V_{GS}=0	—	0.85	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=2A, V_{GS}=0 di_F/dt=100A/μs	—	300	—	ns

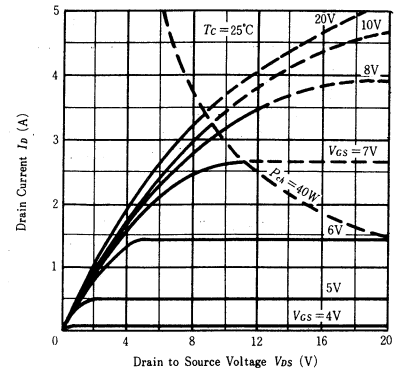
*Pulse Test

HITACHI

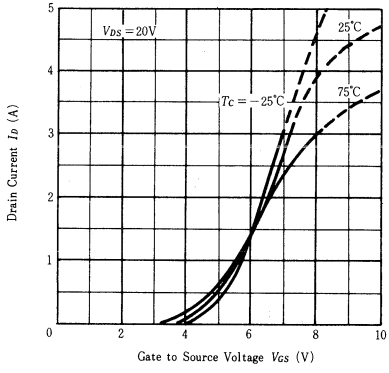
MAXIMUM SAFE OPERATION AREA



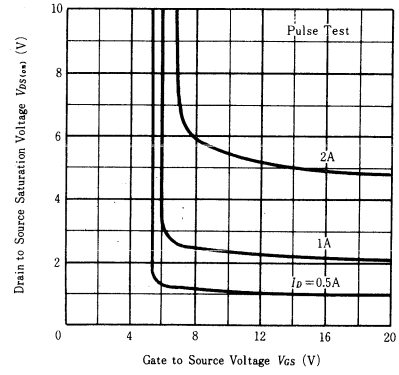
TYPICAL OUTPUT CHARACTERISTICS



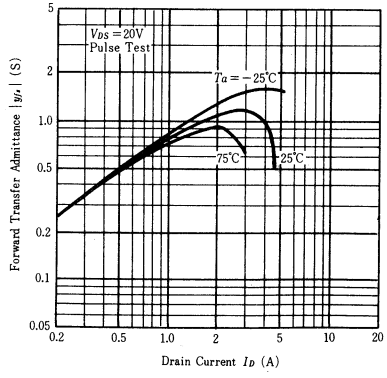
TYPICAL TRANSFER CHARACTERISTICS



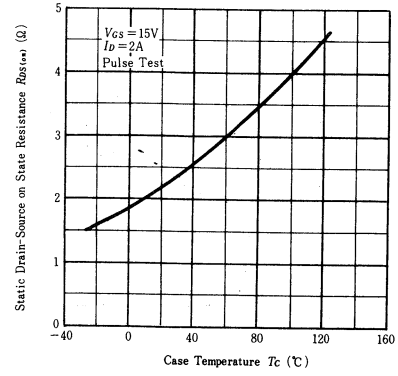
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



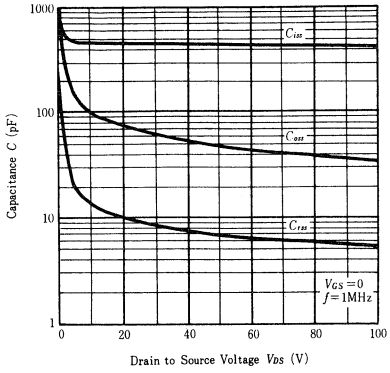
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



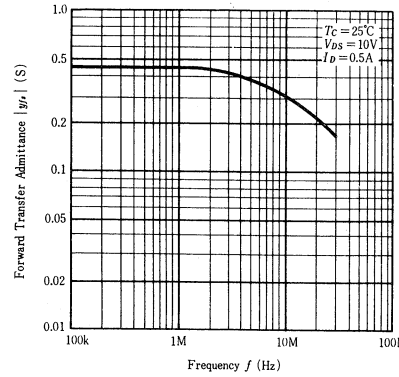
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



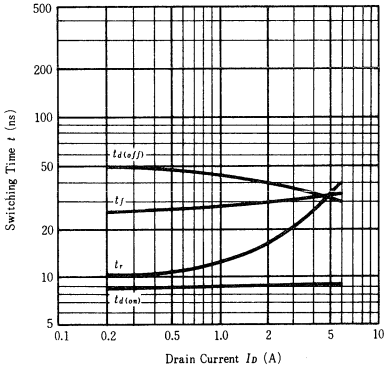
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



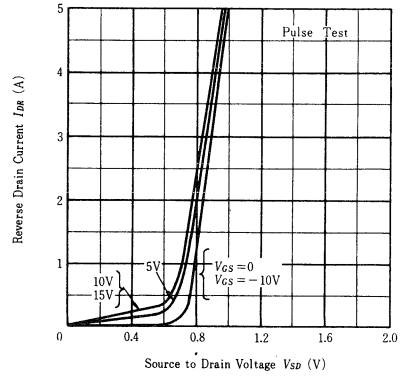
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



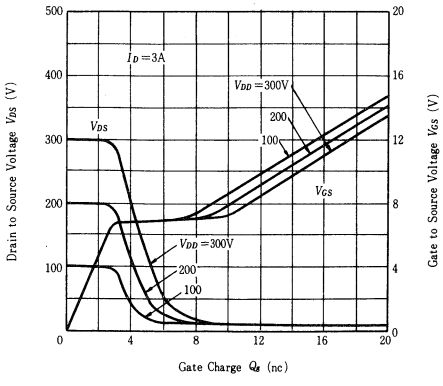
SWITCHING CHARACTERISTICS



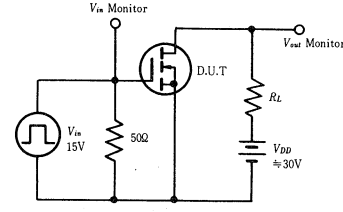
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



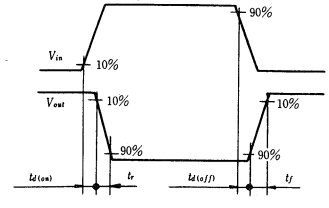
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



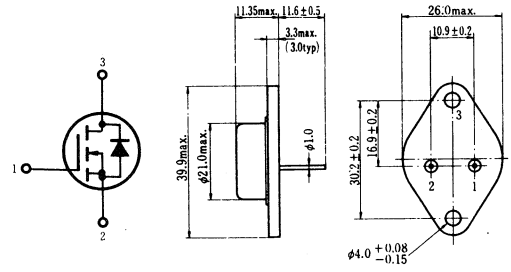
2SK312, 2SK313

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Control, and Ultrasonic Power Oscillators.



1. Gate
2. Source
3. Drain (Case)

(Dimensions in mm)

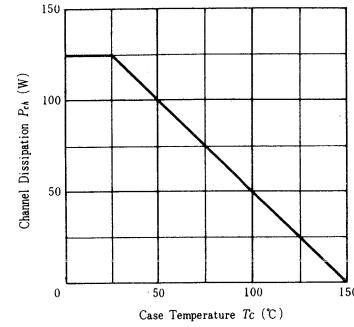
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SK312	2SK313	
Drain-Source Voltage	V_{DSS}	400	450	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	12		A
Drain Peak Current	$I_{D(peak)}$	18		A
Body-Drain Diode Reverse Drain Current	I_{DR}	12		A
Channel Dissipation	P_{ch}*	125		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

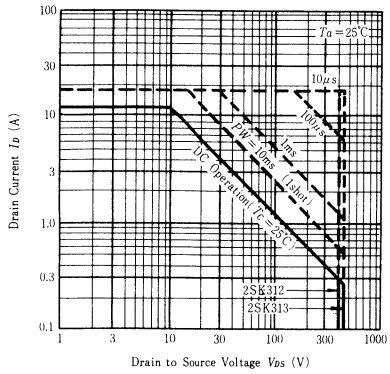


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

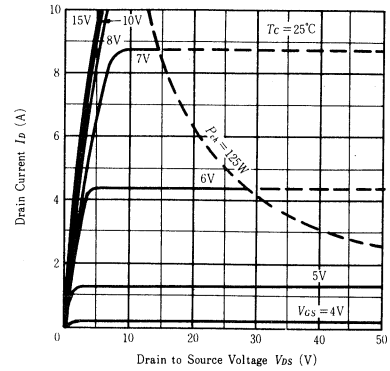
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK312	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	400	—	—	V
	2SK313			450	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	2SK312	I_{DSS}	V_{DS}=320V, V_{GS}=0	—	—	1	mA
	2SK313		V_{DS}=360V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	5.0	V
Static Drain-Source On State Resistance		$R_{DS(on)}$	I_D=6A, V_{GS}=15V*	—	0.67	0.9	Ω
Drain-Source Saturation Voltage		$V_{DS(on)}$	I_D=6A, V_{GS}=15V*	—	4.0	5.4	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=6A, V_{DS}=10V*	1.5	2.5	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	1500	—	pF
Output Capacitance		C_{oss}		—	330	—	pF
Reverse Transfer Capacitance		C_{rss}		—	35	—	pF
Turn-on Delay Time		$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	20	—	ns
Rise Time		t_r		—	50	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	140	—	ns
Fall Time		t_f		—	60	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=6A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=6A, V_{GS}=0 di_F/dt=100A/μs	—	400	—	ns

*Pulse Test

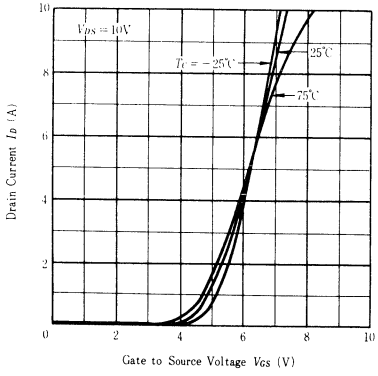
MAXIMUM SAFE OPERATION AREA



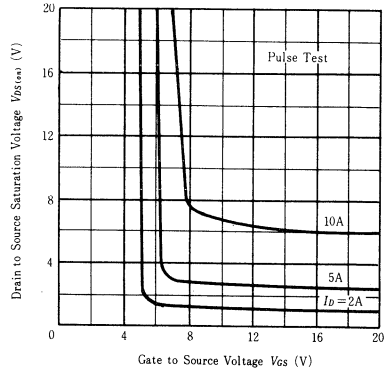
TYPICAL OUTPUT CHARACTERISTICS



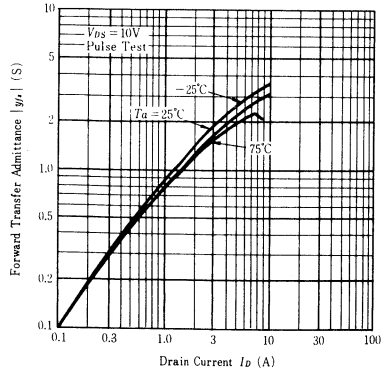
TYPICAL TRANSFER CHARACTERISTICS



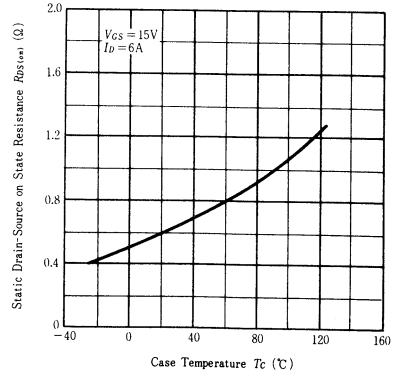
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



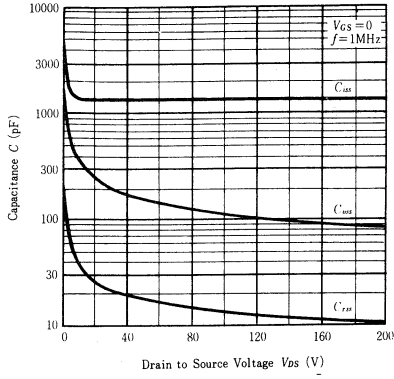
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



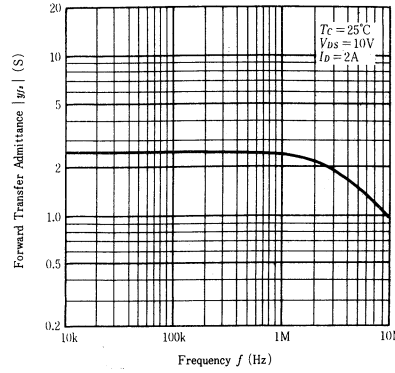
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



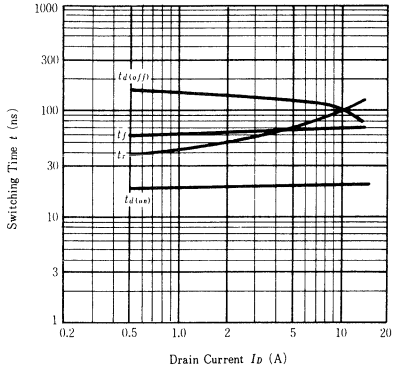
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



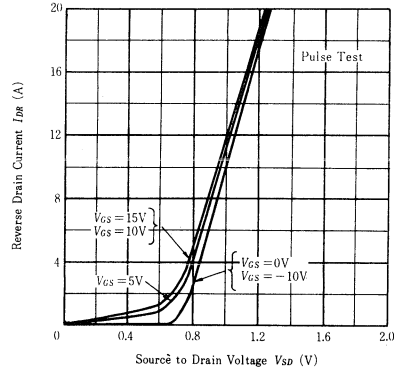
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



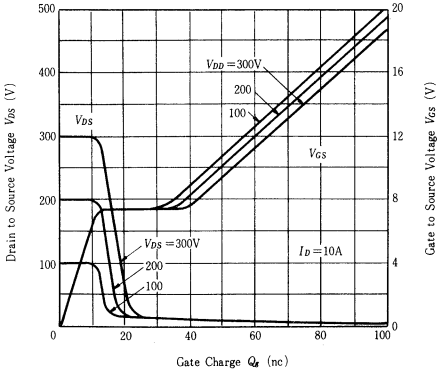
SWITCHING CHARACTERISTICS



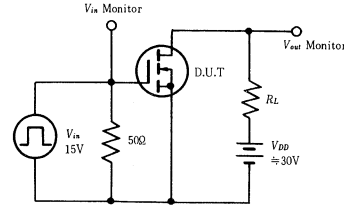
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



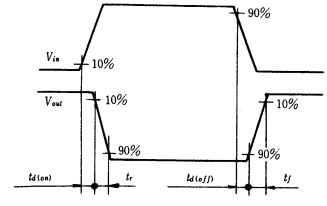
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



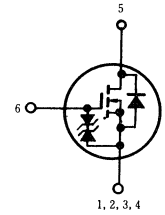
2SK317

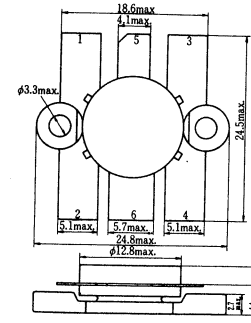
SILICON N-CHANNEL MOS FET

HF/VHF POWER AMPLIFIER

■ FEATURES

- High Breakdown Voltage.
- You Can Decrease Handling Current.
- Gate is Protected by Zenner Diodes.
- No Secondary-Breakdown.
- Wide Area of Safe Operation.
- Infinite VSWR.
- No Thermal Runaway.
- Simple Bias Circuitry.





1. Source
2. Source
3. Source
4. Source
5. Drain
6. Gate

(Dimensions in mm)

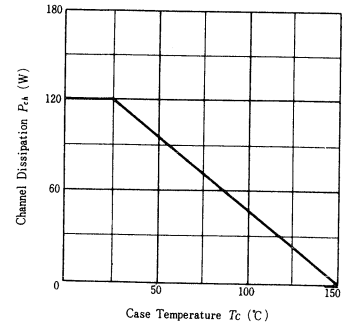
(RF-PAK)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	180	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Body-Drain Diode Reverse Drain Current	I_{DR}	8	A
Channel Dissipation	P_{ch}*	120	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING



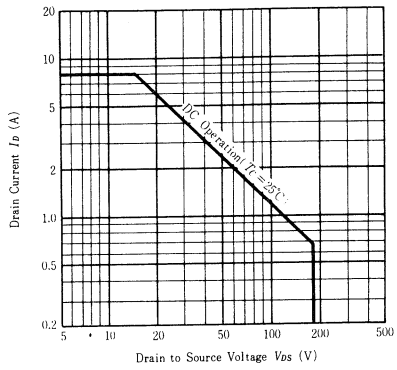
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Power Output	P_O	V_{DS}=80V, I_{DQ}=0.1A	120	—	—	W
Drain Efficiency	η	Pin=8W, f=100MHz	—	(80)	—	%
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	180	—	—	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=140V, V_{GS}=0	—	—	1.0	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V*	0.5	—	3.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=4A, V_{GS}=10V*	—	0.95	1.5	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=4A, V_{GS}=10V*	—	3.8	6.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=3A, V_{DS}=20V*	0.9	1.25	—	℧S
Input Capacitance	C_{iss}	V_{GS}=5V, V_{DS}=0, f=1MHz	—	600	—	pF
Output Capacitance	C_{oss}	V_{GS}=−5V, V_{DS}=50V, f=1MHz	—	90	—	pF
Reverse Transfer Capacitance	C_{rss}	V_{GD}=−50V, f=1MHz	—	0.5	—	pF

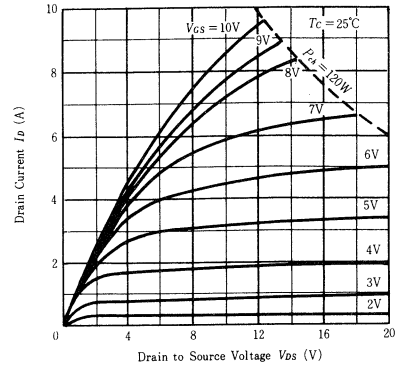
*Pulse Test

CAUTION: OPERATING HAZARDS
Beryllium Oxide Ceramics have been employed in these products.
Since dust or fume of the material is highly poison to the human body, please do not treat them mechanically or chemically in the manner which might expose them to the air. And it should never be thrown out with general industrial or domestic waste.

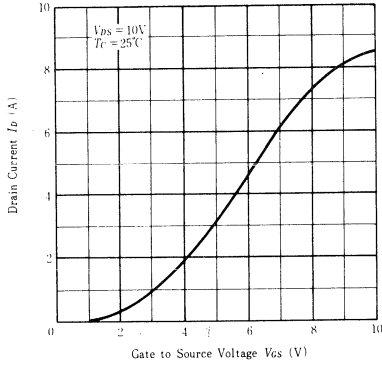
MAXIMUM SAFE OPERATION AREA



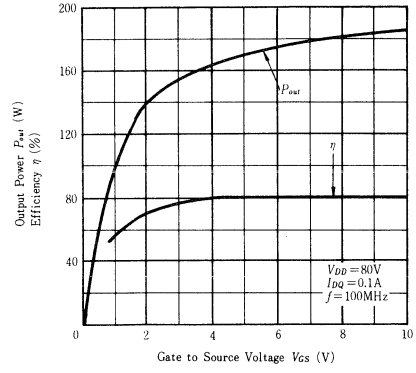
TYPICAL OUTPUT CHARACTERISTICS



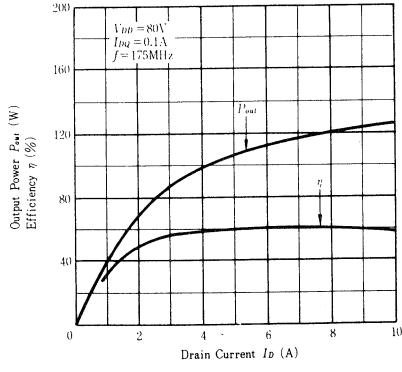
TYPICAL TRANSFER CHARACTERISTICS



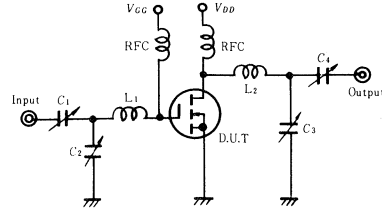
INPUT POWER VS. OUTPUT POWER (1)



INPUT POWER VS. OUTPUT POWER (2)



OUTPUT POWER TEST CIRCUIT

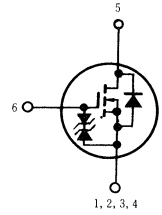


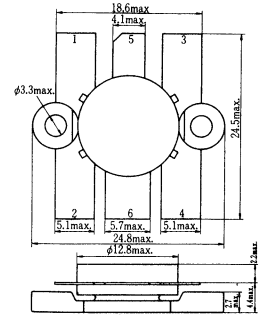
C_1=22pF, C_2=33pF, C_3=10pF, C_4=22pF
L_1, L_2; I_D=6mm, d=1mm
f=100MHz; L_1=3T, L_2=6T
f=175MHz; L_1=1T, L_2=3T

2SK318

SILICON N-CHANNEL MOS FET

HF/VHF POWER AMPLIFIER





1. Source
2. Source
3. Source
4. Source
5. Drain
6. Gate

(RF-PAK)

(Dimensions in mm)

■ FEATURES

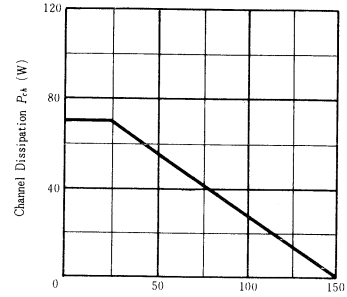
- High Breakdown Voltage.
- You Can Decrease Handling Current.
- Gate is Protected by Zenner Diodes.
- No Secondary-Breakdown.
- Wide Area of Safe Operation.
- Infinite VSWR.
- No Thermal Runaway.
- Simple Bias Circuitry.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	180	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	4	A
Body-Drain Diode Reverse Drain Current	I_{DR}	4	A
Channel Dissipation	P_{ch}*	70	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



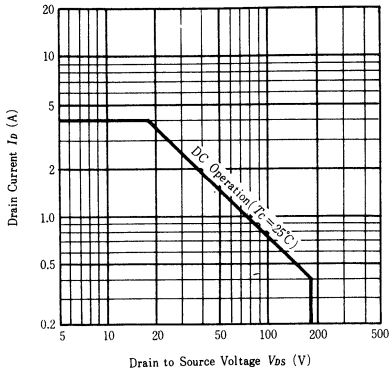
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Power Output	P_O	V_{DS}=80V, I_{DQ}=0.1A	60	90	—	W
Drain Efficiency	η	Pin=4W, f=100MHz	—	(80)	—	%
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	180	—	—	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=140V, V_{GS}=0	—	—	1.0	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	0.5	—	3.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=2A, V_{GS}=10V*	—	1.9	3.0	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=2A, V_{GS}=10V*	—	3.8	6.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=1.5A, V_{DS}=20V*	0.4	0.6	—	S
Input Capacitance	C_{iss}	V_{GS}=5V, V_{DS}=0, f=1MHz	—	300	—	pF
Output Capacitance	C_{oss}	V_{GS}=−5V, V_{DS}=50V, f=1MHz	—	45	—	pF
Reverse Transfer Capacitance	C_{rss}	V_{GD}=−50V, f=1MHz	—	0.3	—	pF

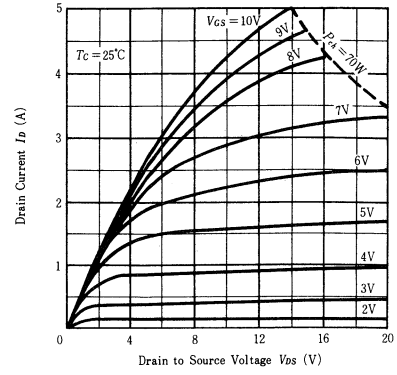
*Pulse Test

CAUTION: OPERATING HAZARDS
Beryllium Oxide Ceramics have been employed in these products.
Since dust or fume of the material is highly poison to the human body, please do not treat them mechanically or chemically in the manner which might expose them to the air. And it should never be thrown out with general industrial or domestic waste.

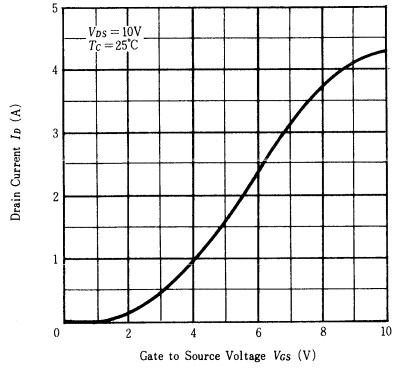
MAXIMUM SAFE OPERATION AREA



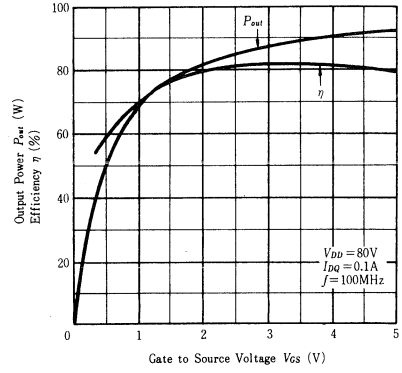
TYPICAL OUTPUT CHARACTERISTICS



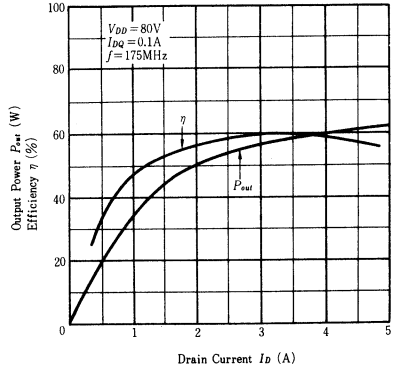
TYPICAL TRANSFER CHARACTERISTICS



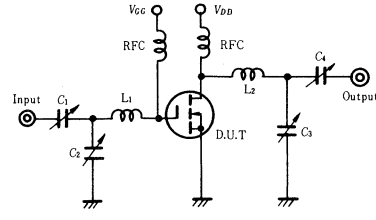
INPUT POWER VS. OUTPUT POWER (1)



INPUT POWER VS. OUTPUT POWER (2)



OUTPUT POWER TEST CIRCUIT



C_1 = 22pF, C_2 = 33pF, C_3 = 25pF, C_4 = 50pF
L_1, L_2; I_D = 6mm, d = 1mm
f = 100MHz; L_1 = 3T, L_2 = 5T
f = 175MHz; L_1 = 1T, L_2 = 3T

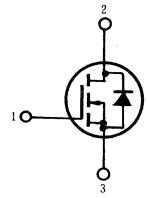
2SK319, 2SK320

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

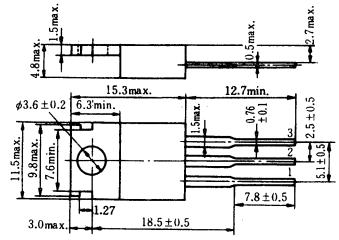
■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)



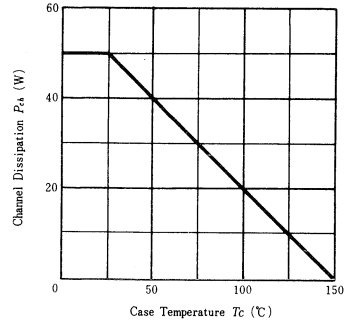
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SK319	2SK320	
Drain-Source Voltage	V_{DSS}	400	450	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	5		A
Drain Peak Current	$I_{D(peak)}$	10		A
Body-Drain Diode Reverse Drain Current	I_{DR}	5		A
Channel Dissipation	P_{ch}*	50		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING



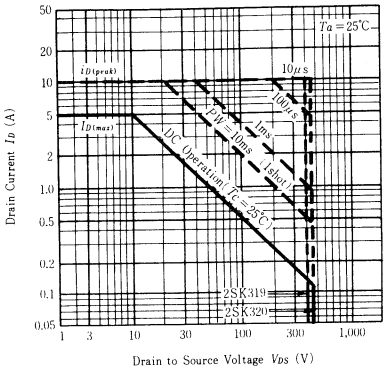
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK319	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	400	—	—	V
	2SK320			450	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	2SK319	I_{DSS}	V_{DS}=320V, V_{GS}=0	—	—	−1	mA
	2SK320		V_{DS}=360V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	5.0	V
Static Drain-Source On State Resistance		$R_{DS(on)}$	I_D=3A, V_{GS}=−15V*	—	1.1	1.83	Ω
Drain-Source Saturation Voltage		$V_{DS(on)}$	I_D=3A, V_{GS}=15V*	—	3.3	5.5	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	1.0	1.5	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	800	—	pF
Output Capacitance		C_{oss}		—	180	—	pF
Reverse Transfer Capacitance		C_{rss}		—	20	—	pF
Turn-on Delay Time		$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	15	—	ns
Rise Time		t_r		—	35	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	85	—	ns
Fall Time		t_f		—	35	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=3A, V_{GS}=0	—	0.85	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=3A, V_{GS}=0 di_F/dt=100A/μs	—	350	—	ns

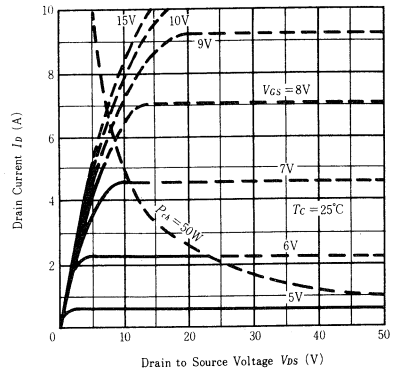
*Pulse Test

HITACHI

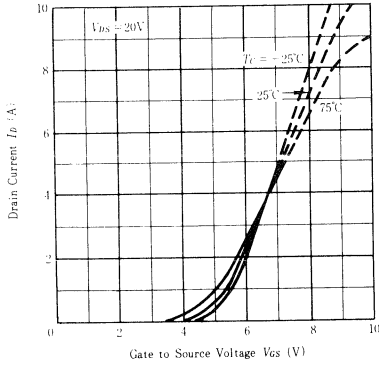
MAXIMUM SAFE OPERATION AREA



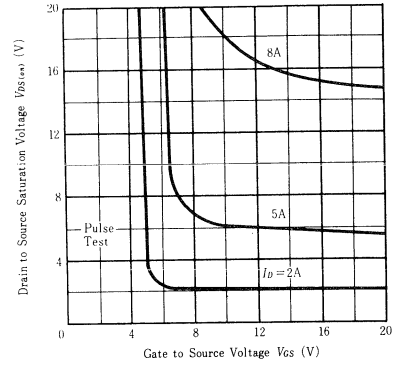
TYPICAL OUTPUT CHARACTERISTICS



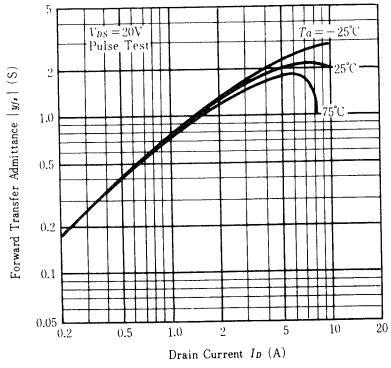
TYPICAL TRANSFER CHARACTERISTICS



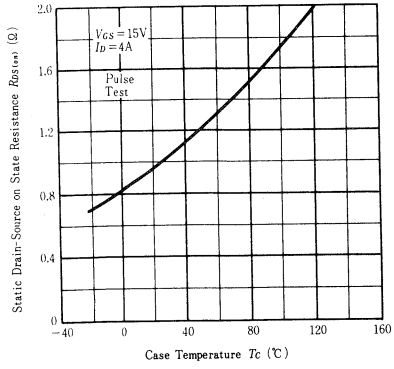
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



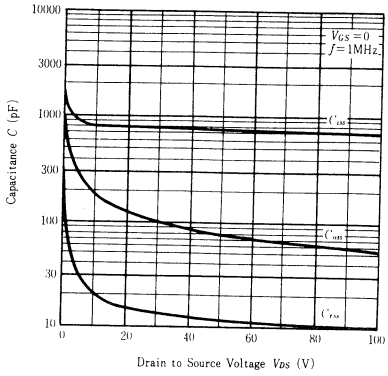
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



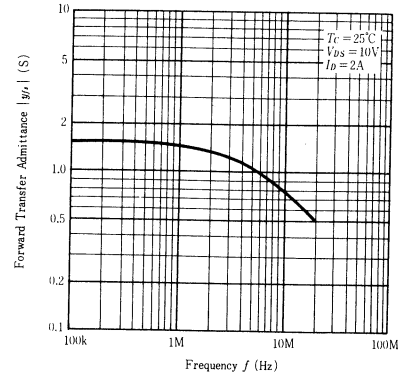
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



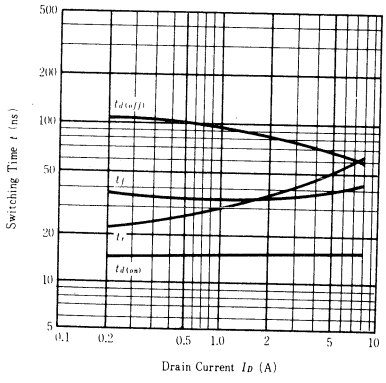
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



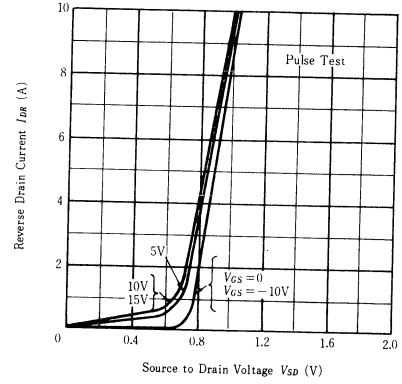
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



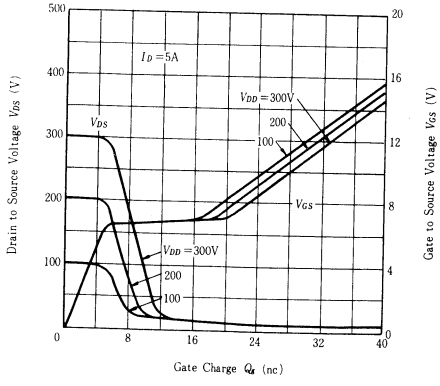
SWITCHING CHARACTERISTICS



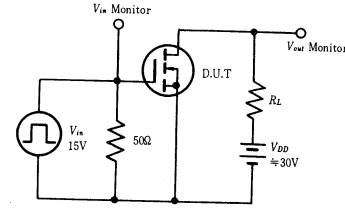
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



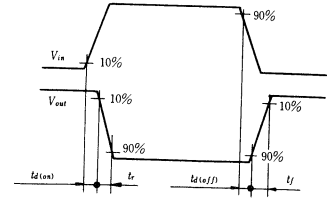
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



2SK345,2SK346

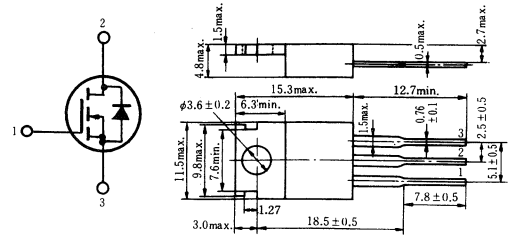
SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, LOW FREQUENCY POWER AMPLIFIER

Complementary pair with 2SJ101, 2SJ102

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- No Secondary Breakdown.
- Good Complementary Characteristics.
- Suitable for Switching Regulator, DC-DC Converter, and PWM Amplifier.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

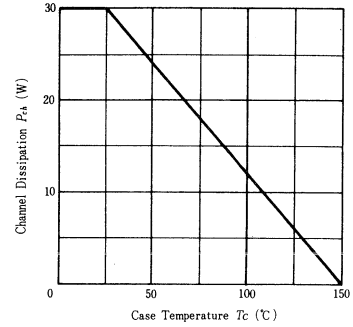
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Rating		Unit
		2SK345	2SK346	
Drain-Source Voltage	V_{DSS}	40	60	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	5		A
Drain Peak Current	$I_{D(peak)}$	10		A
Body-Drain Diode Reverse Drain Current	I_{DR}	5		A
Channel Dissipation	P_{ch}*	30		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

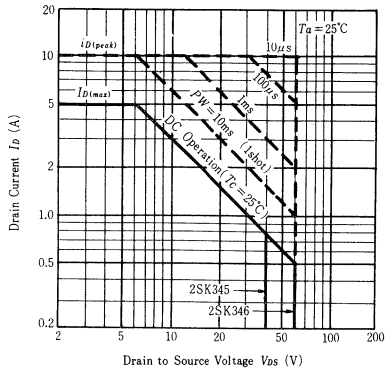


■ ELECTRICAL CHARACTERISTICS (T_a=25°C)

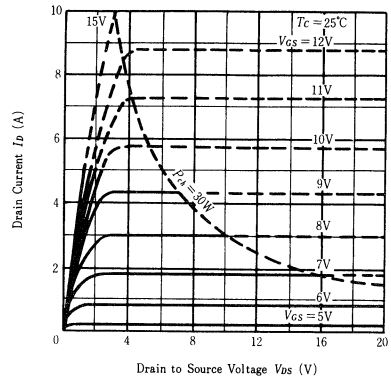
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK345	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	40	—	—	V
	2SK346			60	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	2SK345	I_{DSS}	V_{DS}=30V, V_{GS}=0	—	—	1	mA
	2SK346		V_{DS}=50V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	5.0	V
Static Drain-Source On State Resistance		$R_{DS(on)}$	I_D=3A, V_{GS}=15V*	—	0.3	0.4	Ω
Drain-Source Saturation Voltage		$V_{DS(on)}$	I_D=3A, V_{GS}=15V*	—	0.9	1.2	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	0.5	0.9	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	350	—	pF
Output Capacitance		C_{oss}		—	290	—	pF
Reverse Transfer Capacitance		C_{rss}		—	80	—	pF
Turn-on Delay Time		$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	12	—	ns
Rise Time		t_r		—	28	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	30	—	ns
Fall Time		t_f		—	40	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=3A, V_{GS}=0	—	0.85	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=3A, V_{GS}=0 di_F/dt=500A/μs	—	160	—	ns

*Pulse Test

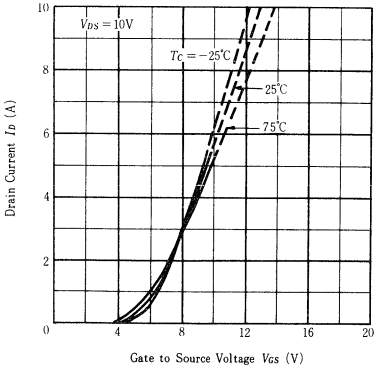
MAXIMUM SAFE OPERATION AREA



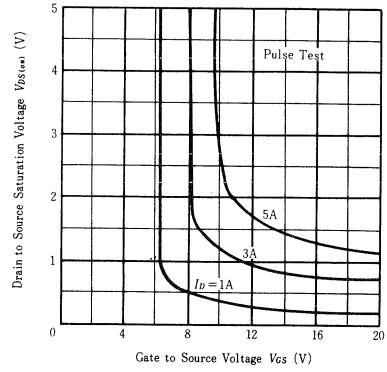
TYPICAL OUTPUT CHARACTERISTICS



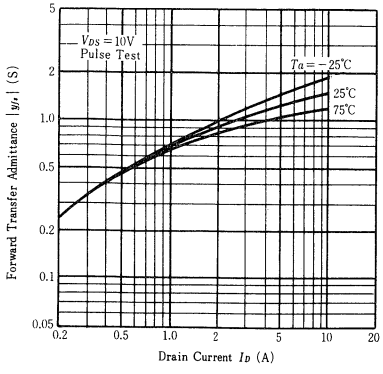
TYPICAL TRANSFER CHARACTERISTICS



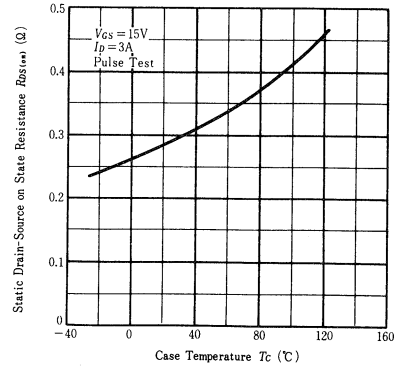
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



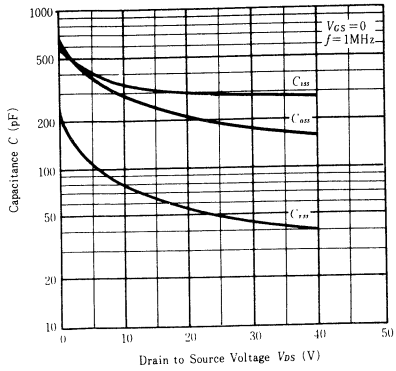
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



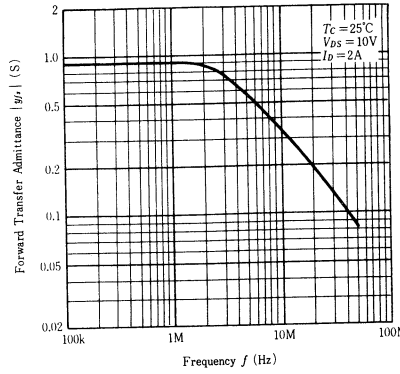
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



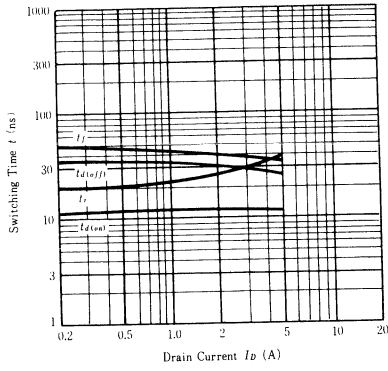
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



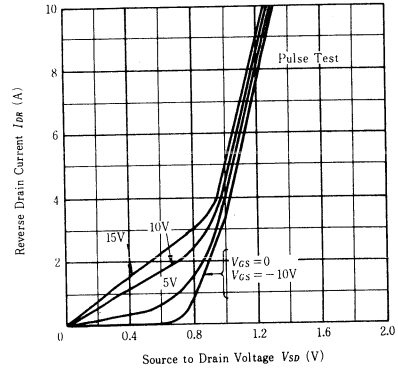
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



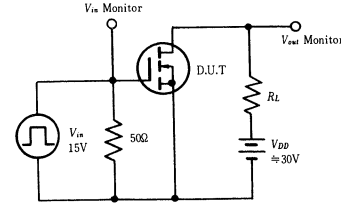
SWITCHING CHARACTERISTICS



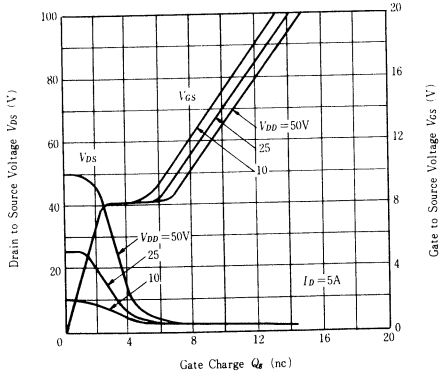
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



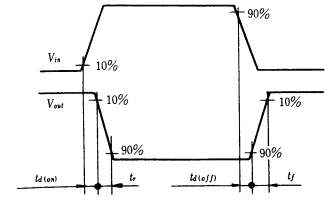
SWITCHING TIME TEST CIRCUIT



DYNAMIC INPUT CHARACTERISTICS



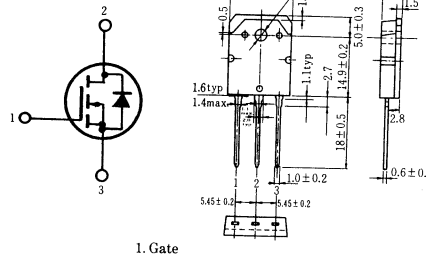
WAVEFORMS



2SK349, 2SK350

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

(TO-3P)

■ FEATURES

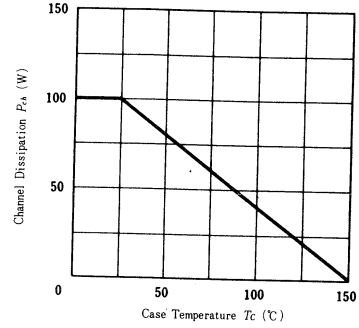
- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Control, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SK349	2SK350	
Drain-Source Voltage	V_{DSS}	400	450	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	10		A
Drain Peak Current	$I_{D(peak)}$	15		A
Body-Drain Diode Reverse Drain Current	I_{DR}	10		A
Channel Dissipation	P_{ch}*	100		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



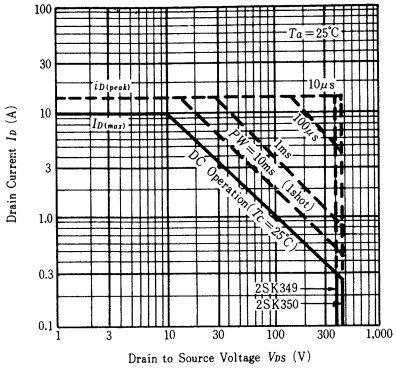
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK349	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	400	—	—	V
	2SK350			450	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	2SK349	I_{DSS}	V_{DS}=320V, V_{GS}=0	—	—	1	mA
	2SK350		V_{DS}=360V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	5.0	V
Static Drain-Source On State Resistance		$R_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	0.67	0.9	Ω
Drain-Source Saturation Voltage		$V_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	3.3	4.5	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=5A, V_{DS}=10V*	1.3	2.5	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	1500	—	pF
Output Capacitance		C_{oss}		—	330	—	pF
Reverse Transfer Capacitance		C_{rss}		—	35	—	pF
Turn-on Delay Time		$t_{d(on)}$	I_D=2A, V_{GS}=15V, R_L=15Ω	—	20	—	ns
Rise Time		t_r		—	50	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	140	—	ns
Fall Time		t_f		—	60	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=5A, V_{GS}=0	—	0.85	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=5A, V_{GS}=0, di_F/dt=100A/μs	—	400	—	ns

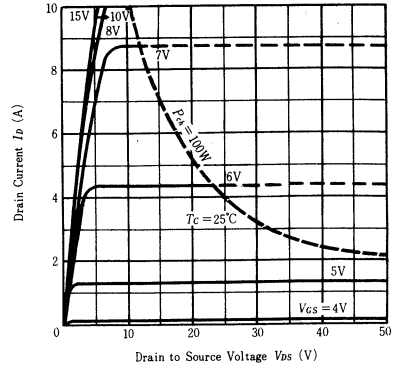
*Pulse Test

HITACHI

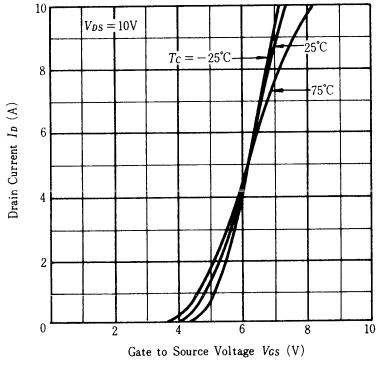
MAXIMUM SAFE OPERATION AREA



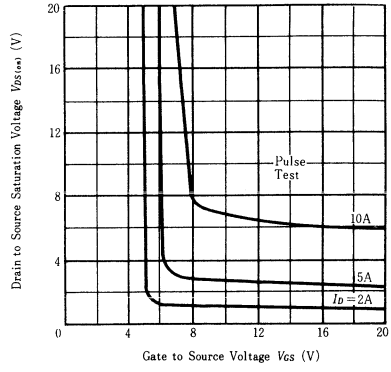
TYPICAL OUTPUT CHARACTERISTICS



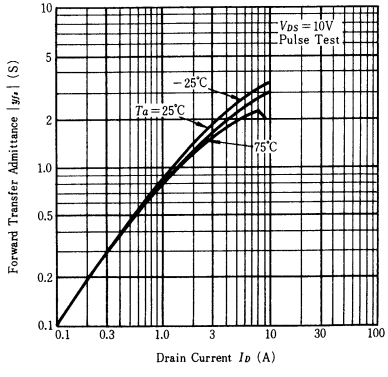
TYPICAL TRANSFER CHARACTERISTICS



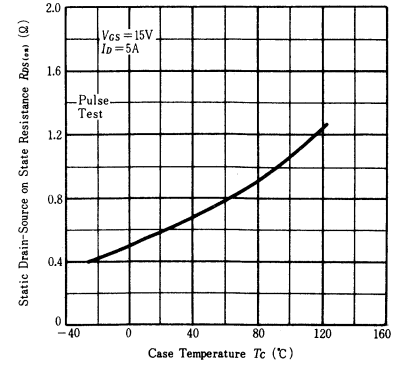
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



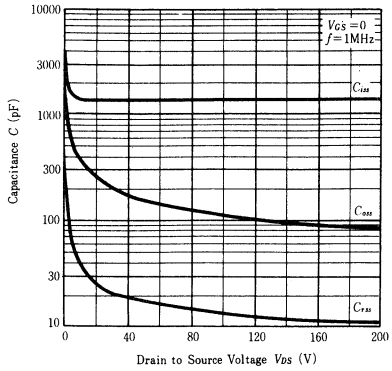
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



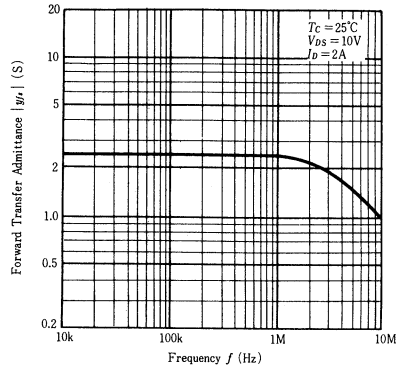
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



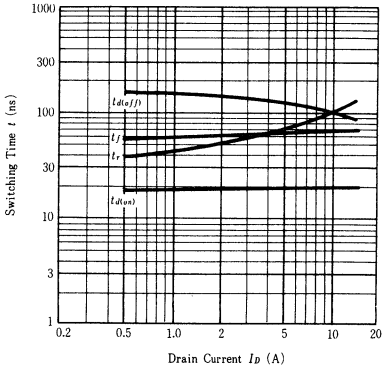
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



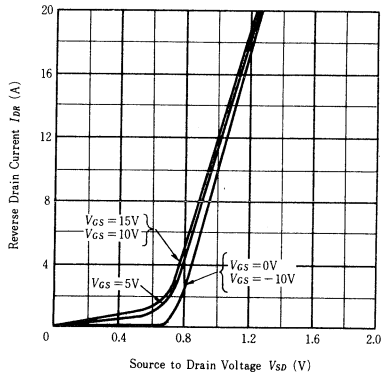
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



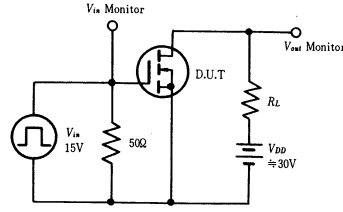
SWITCHING CHARACTERISTICS



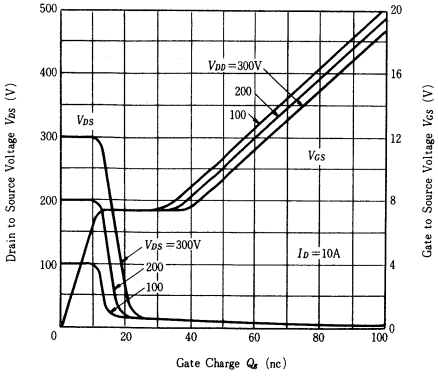
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



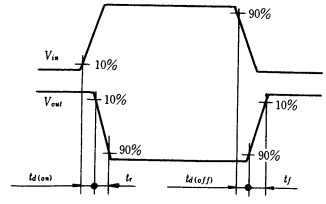
SWITCHING TIME TEST CIRCUIT



DYNAMIC INPUT CHARACTERISTICS



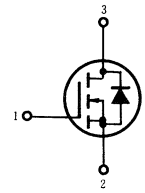
WAVEFORMS

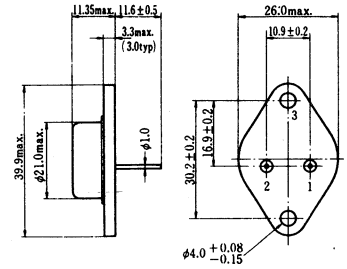


2SK351

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER





1. Gate
2. Source
3. Drain (Case)

(Dimensions in mm)

(JEDEC TO-3)

■ FEATURES

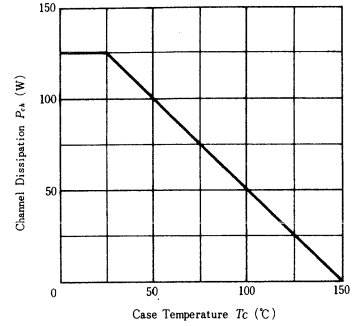
- High Breakdown Voltage.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	800	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	5	A
Drain Peak Current	$I_{D(peak)}$	10	A
Body-Drain Diode Reverse Drain Current	I_{DR}	5	A
Channel Dissipation	P_{ch}*	125	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

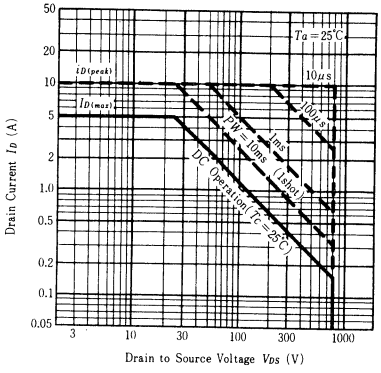


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

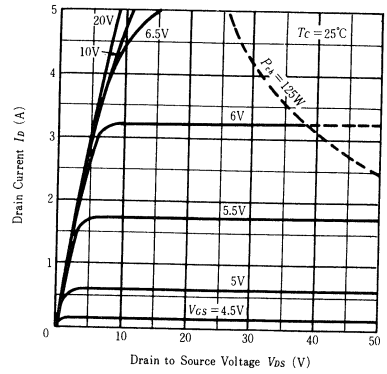
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	800	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=640V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=3A, V_{GS}=15V*	—	1.7	3.0	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=3A, V_{GS}=15V*	—	5.0	9.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	1.0	2.0	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	1900	—	pF
Output Capacitance	C_{oss}		—	320	—	pF
Reverse Transfer Capacitance	C_{rss}		—	40	—	pF
Turn-on Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	30	—	ns
Rise Time	t_r		—	70	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	220	—	ns
Fall Time	t_f		—	80	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=3A, V_{GS}=0	—	0.8	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=3A, V_{GS}=0 di_F/dt=100A/μs	—	600	—	ns

*Pulse Test

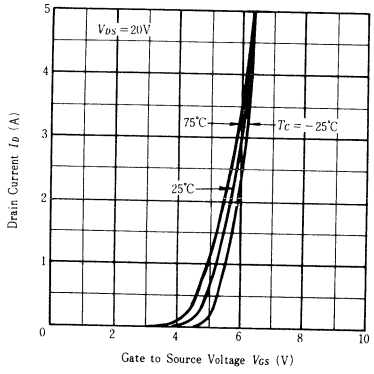
MAXIMUM SAFE OPERATION AREA



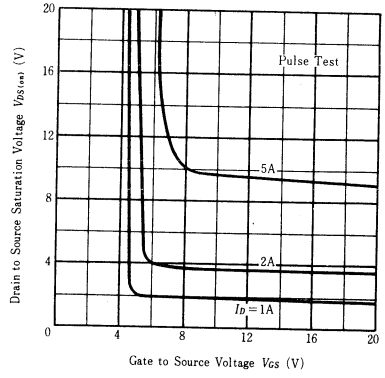
TYPICAL OUTPUT CHARACTERISTICS



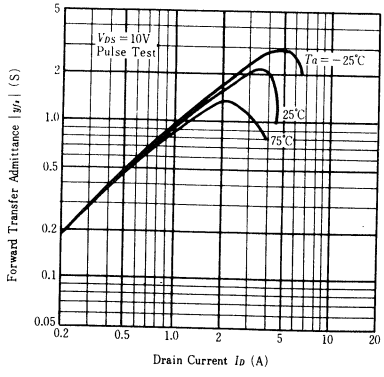
TYPICAL TRANSFER CHARACTERISTICS



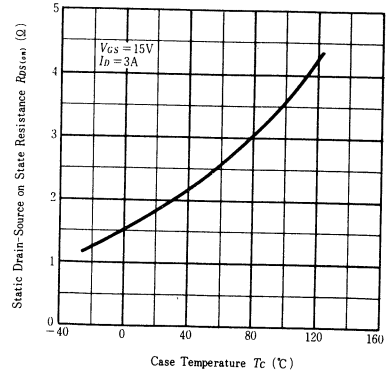
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



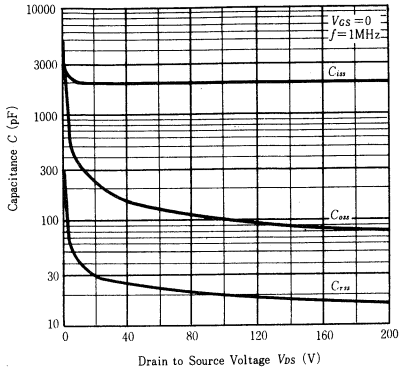
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



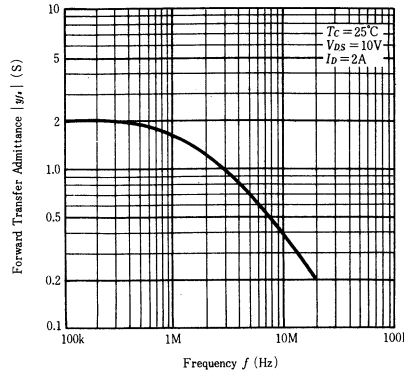
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



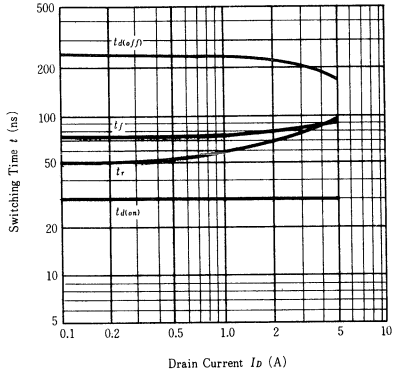
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



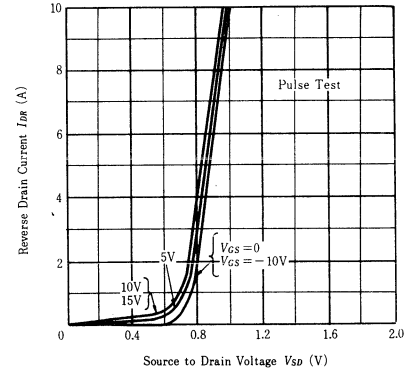
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



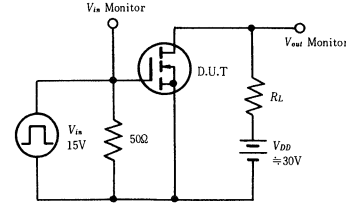
SWITCHING CHARACTERISTICS



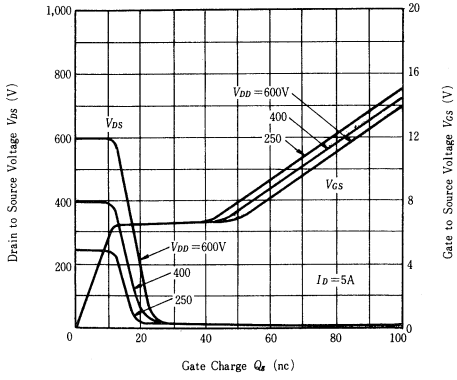
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



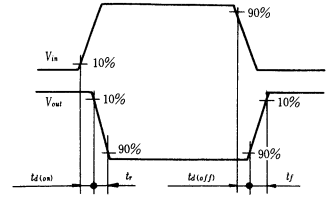
SWITCHING TIME TEST CIRCUIT



DYNAMIC INPUT CHARACTERISTICS



WAVEFORMS



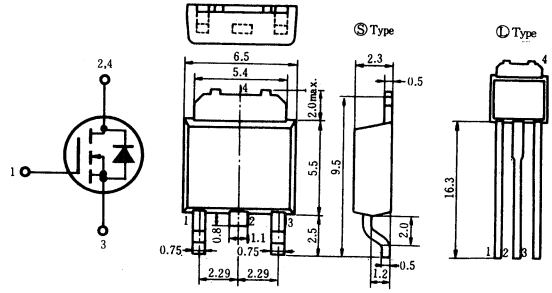
2SK375Ⓛ,2SK375Ⓢ

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Small Package.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2., 4. Drain
3. Source
(Dimensions in mm)

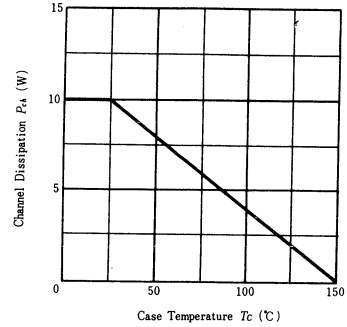
(DPAK)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	300	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	1	A
Drain Peak Current	$I_{D(peak)}$	2	A
Body-Drain Diode Reverse Drain Current	I_{DR}	1	A
Channel Dissipation	P_{ch}*	10	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING



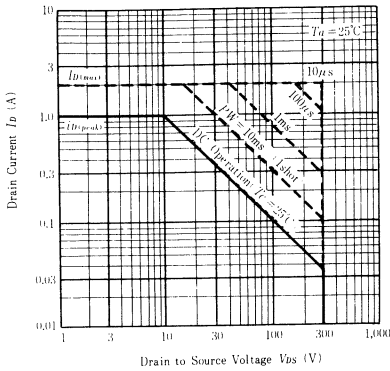
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	300	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=240V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=1A, V_{GS}=15V*	—	2.5	4.0	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=1A, V_{GS}=15V*	—	2.5	4.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=0.5A, V_{DS}=10V*	0.2	0.4	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	140	—	pF
Output Capacitance	C_{oss}		—	65	—	pF
Reverse Transfer Capacitance	C_{rss}		—	23	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=0.5A, V_{GS}=15V, R_L=60Ω	—	6	—	ns
Rise Time	t_r		—	14	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	40	—	ns
Fall Time	t_f		—	30	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=1A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=1A, V_{GS}=0, di_F/dt=100A/μs	—	250	—	ns

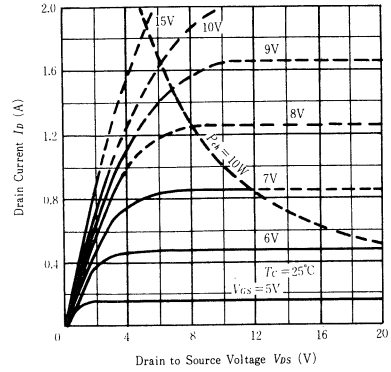
*Pulse Test

HITACHI

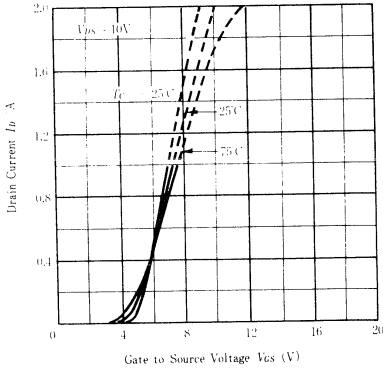
MAXIMUM SAFE OPERATION AREA



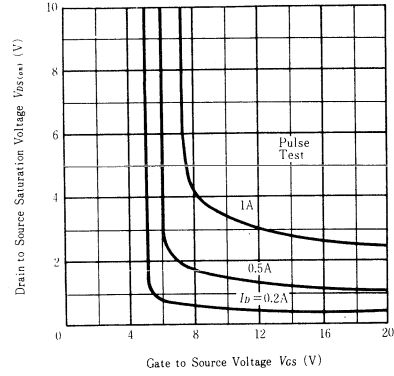
TYPICAL OUTPUT CHARACTERISTICS



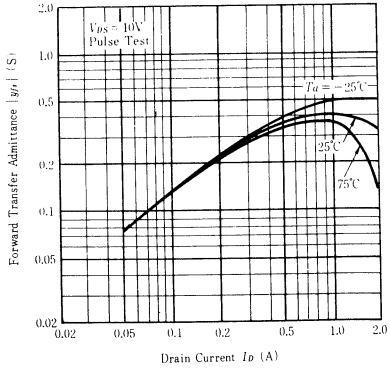
TYPICAL TRANSFER CHARACTERISTICS



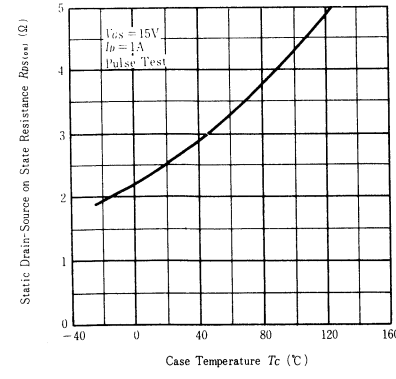
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



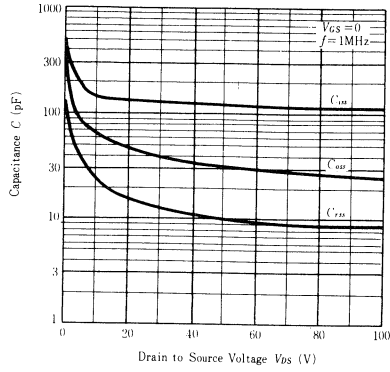
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



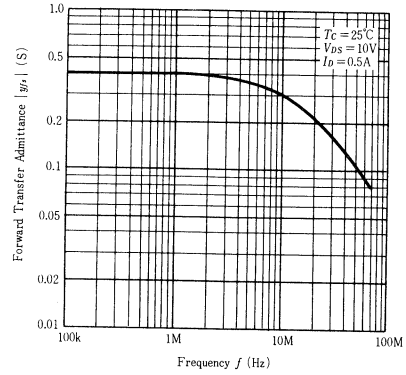
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



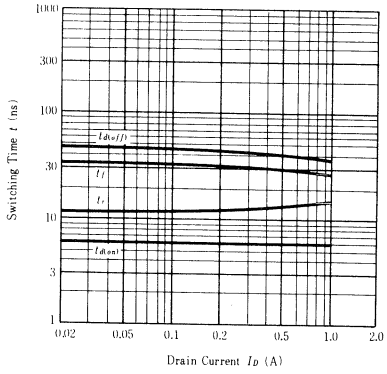
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



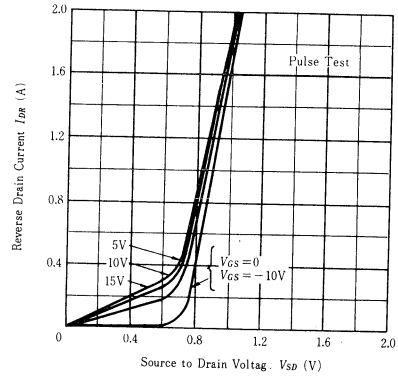
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



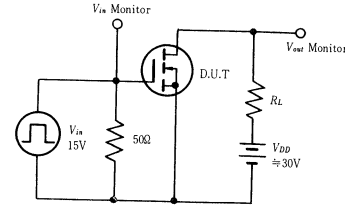
SWITCHING CHARACTERISTICS



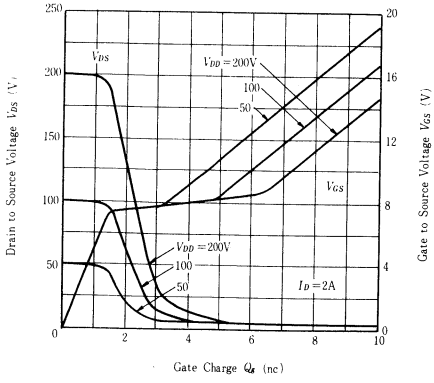
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



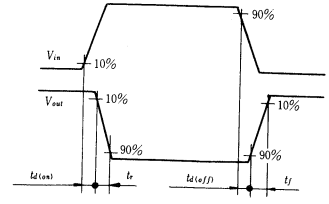
SWITCHING TIME TEST CIRCUIT



DYNAMIC INPUT CHARACTERISTICS



WAVEFORMS



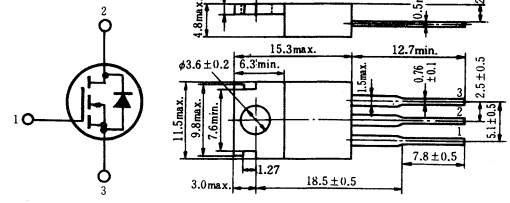
2SK382

SILICON P-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

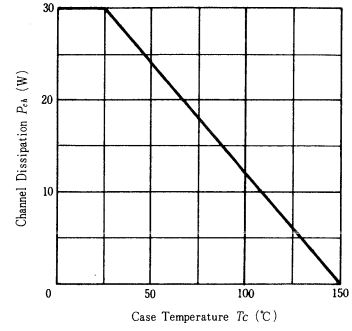
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	500	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	2	A
Drain Peak Current	$I_{D(peak)}$	5	A
Body-Drain Diode Reverse Drain Current	I_{DR}	2	A
Channel Dissipation	P_{ch}*	30	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

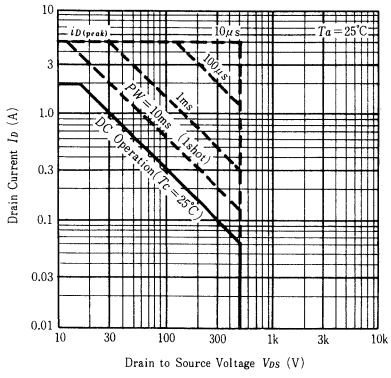


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

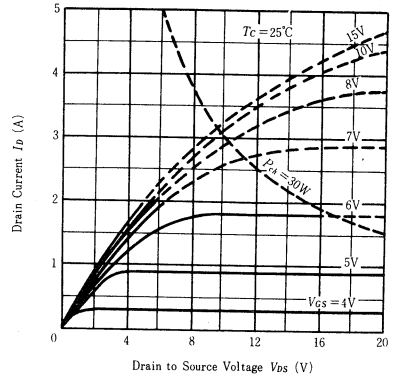
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	500	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=400V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=1A, V_{GS}=15V*	—	2.5	4.0	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=1A, V_{GS}=15V*	—	2.5	4.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=1A, V_{DS}=10V*	0.4	0.7	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	440	—	pF
Output Capacitance	C_{oss}		—	95	—	pF
Reverse Transfer Capacitance	C_{rss}		—	13	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	7	—	ns
Rise Time	t_r		—	18	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	45	—	ns
Fall Time	t_f		—	25	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=1A, V_{GS}=0	—	0.8	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=1A, V_{GS}=0 di_F/dt=100A/μs	—	300	—	ns

*Pulse Test

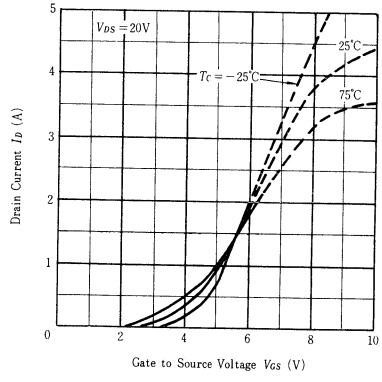
MAXIMUM SAFE OPERATION AREA



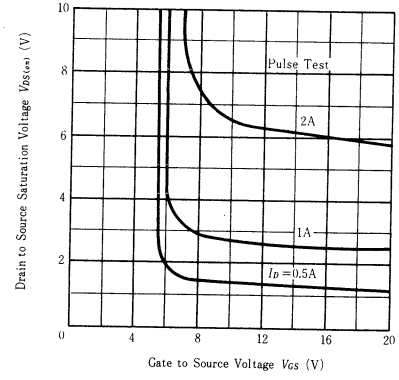
TYPICAL OUTPUT CHARACTERISTICS



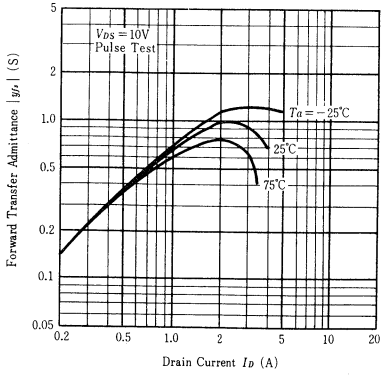
TYPICAL TRANSFER CHARACTERISTICS



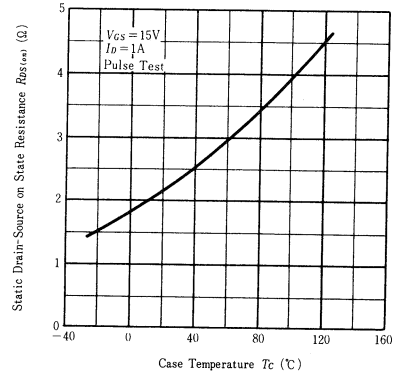
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



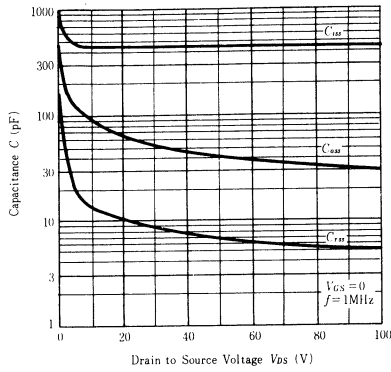
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



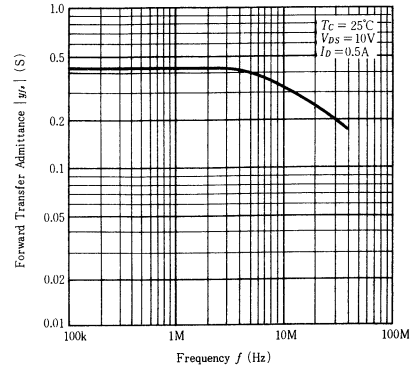
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



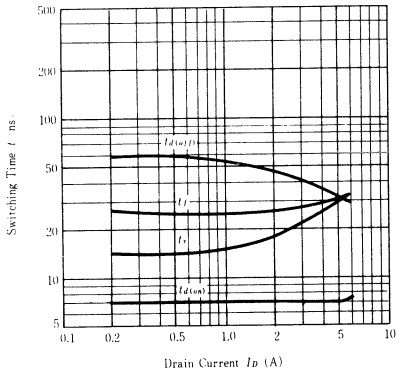
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



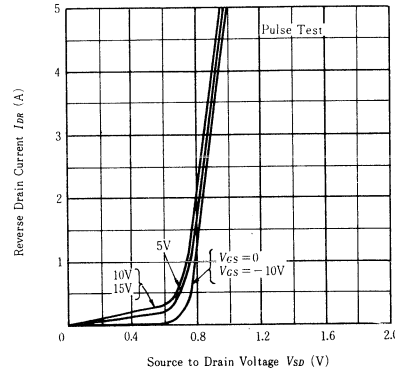
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



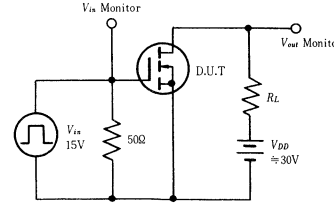
SWITCHING CHARACTERISTICS



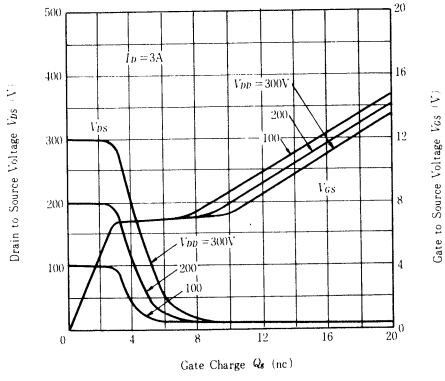
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



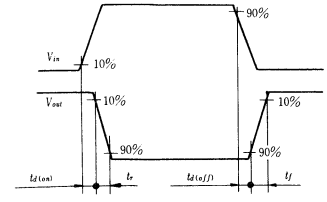
SWITCHING TIME TEST CIRCUIT



DYNAMIC INPUT CHARACTERISTICS



WAVEFORMS



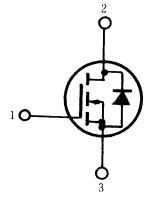
2SK383

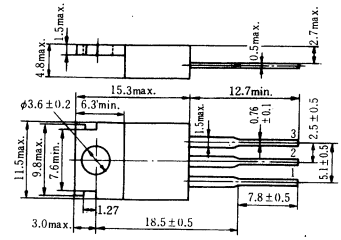
SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

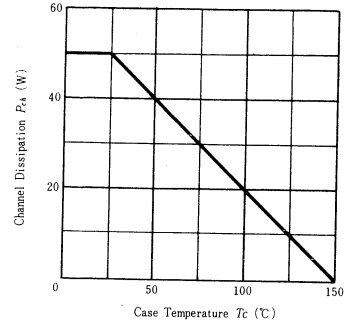
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	10	A
Drain Peak Current	$I_{D(peak)}$	15	A
Body-Drain Diode Reverse Drain Current	I_{DR}	10	A
Channel Dissipation	P_{ch}*	50	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



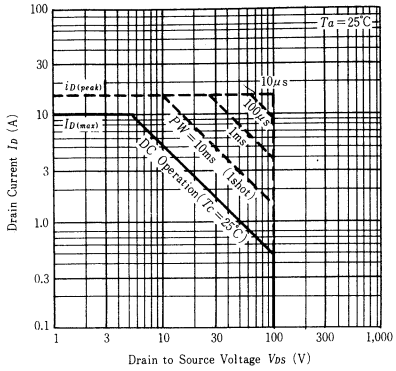
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	100	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	0.15	0.18	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	0.75	0.9	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=5A, V_{DS}=10V*	1.5	2.8	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	1100	—	pF
Output Capacitance	C_{oss}		—	600	—	pF
Reverse Transfer Capacitance	C_{rss}		—	80	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	10	—	ns
Rise Time	t_r		—	50	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	90	—	ns
Fall Time	t_f		—	70	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=5A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=5A, V_{GS}=0 di_F/dt=100A/μs	—	200	—	ns

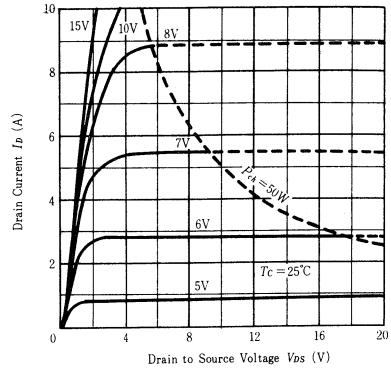
*Pulse Test

HITACHI

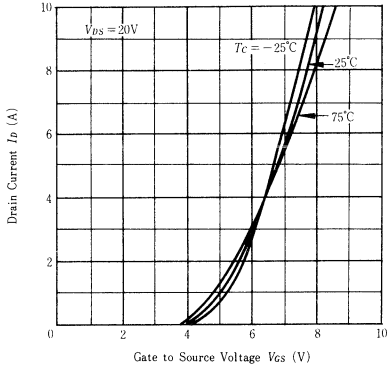
MAXIMUM SAFE OPERATION AREA



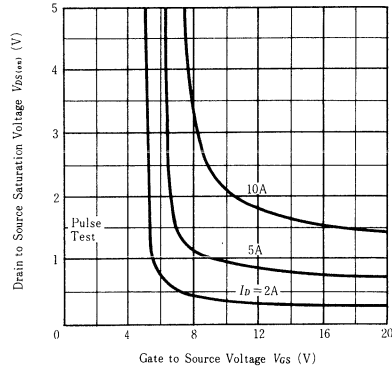
TYPICAL OUTPUT CHARACTERISTICS



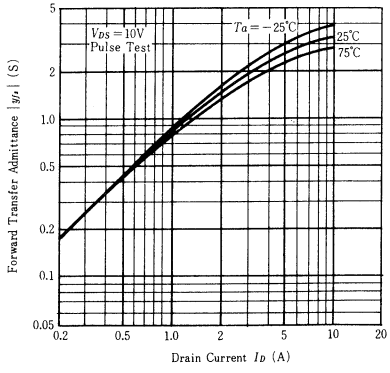
TYPICAL TRANSFER CHARACTERISTICS



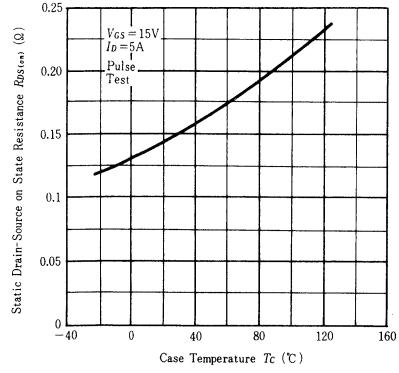
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



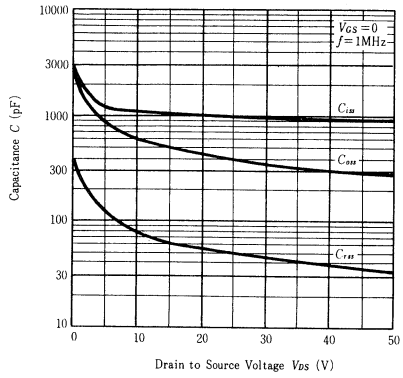
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



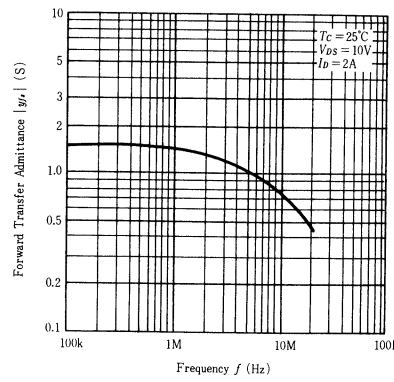
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



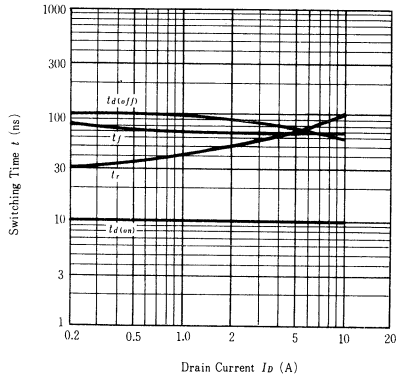
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



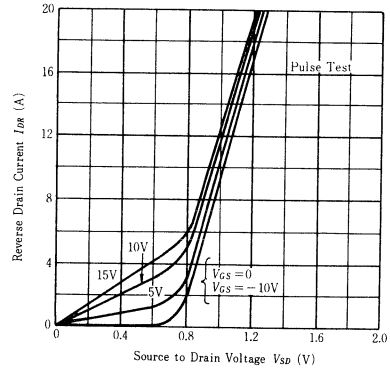
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



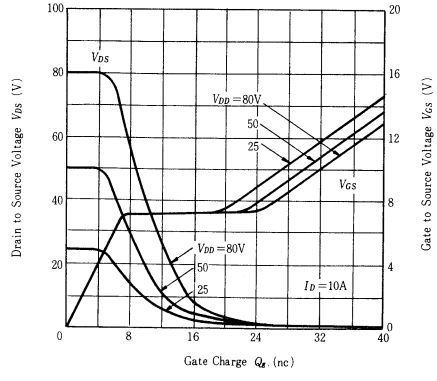
SWITCHING CHARACTERISTICS



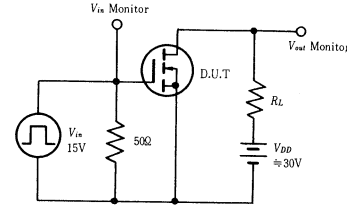
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



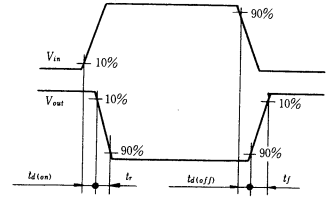
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



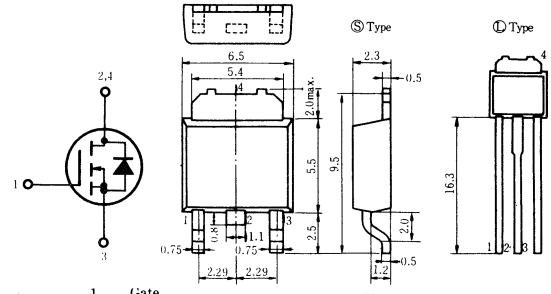
2SK384Ⓛ,2SK384Ⓢ

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Small Package.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2., 4. Drain
3. Source

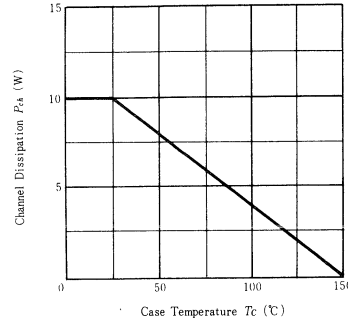
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	500	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	0.3	A
Drain Peak Current	$I_{D(peak)}$	0.6	A
Body-Drain Diode Reverse Drain Current	I_{DR}	0.3	A
Channel Dissipation	P_{ch}*	10	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

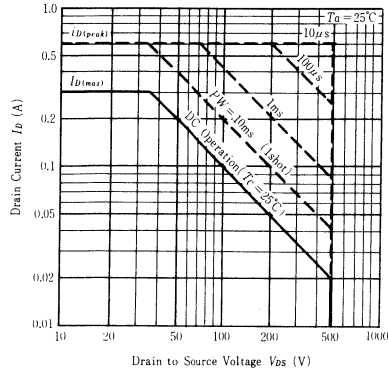


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

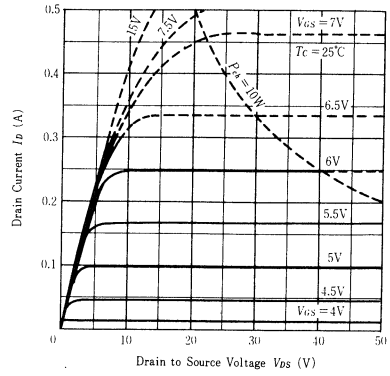
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	500	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=400V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=0.2A, V_{GS}=15V*	—	25	50	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=0.2A, V_{GS}=15V*	—	5.0	10	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=0.2A, V_{DS}=10V*	60	100	—	mS
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	70	—	pF
Output Capacitance	C_{oss}		—	15	—	pF
Reverse Transfer Capacitance	C_{rss}		—	5	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=0.2A, V_{GS}=15V R_L=150Ω	—	7	—	ns
Rise Time	t_r		—	13	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	11	—	ns
Fall Time	t_f		—	9	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=0.2A, V_{GS}=0	—	0.8	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=0.2A, V_{GS}=0 di_F/dt=100A/μs	—	280	—	ns

*Pulse Test

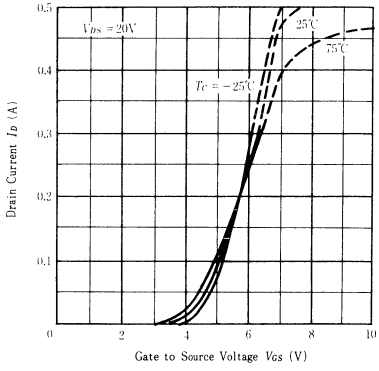
MAXIMUM SAFE OPERATION AREA



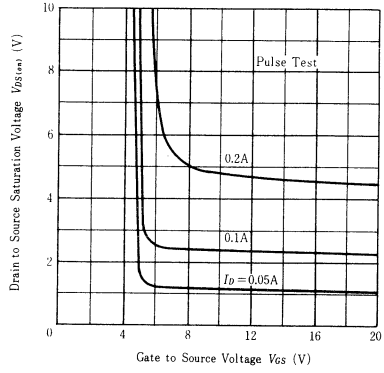
TYPICAL OUTPUT CHARACTERISTICS



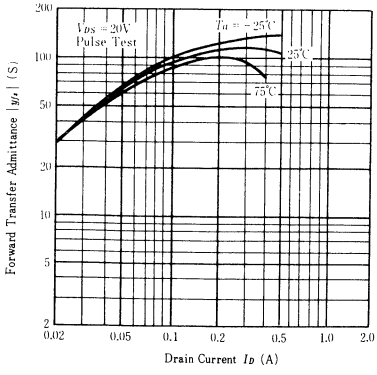
TYPICAL TRANSFER CHARACTERISTICS



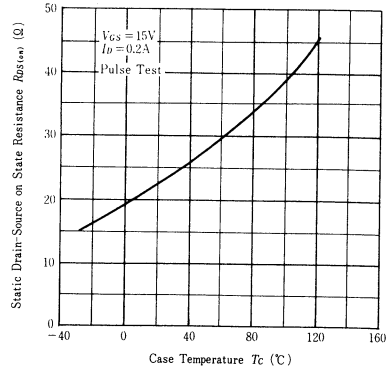
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



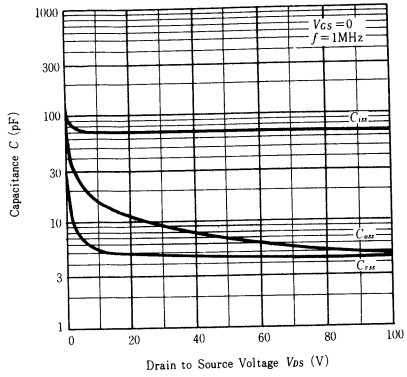
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



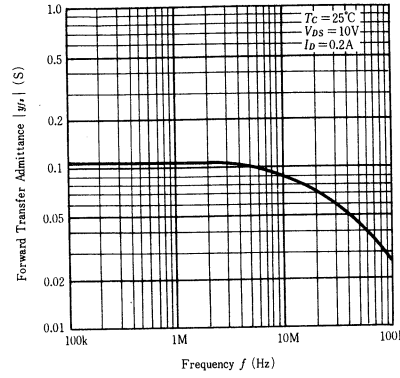
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



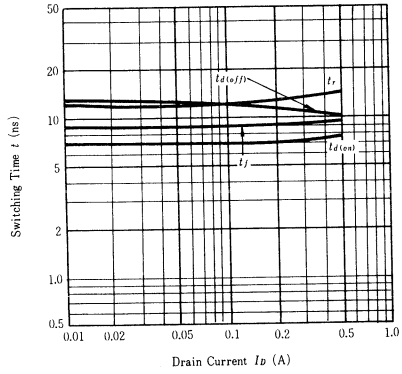
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



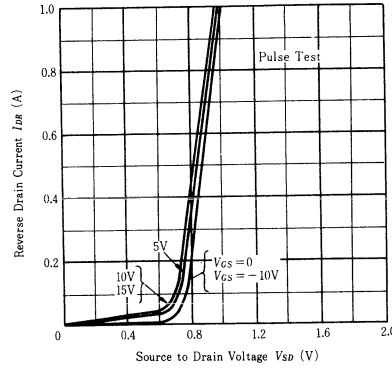
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



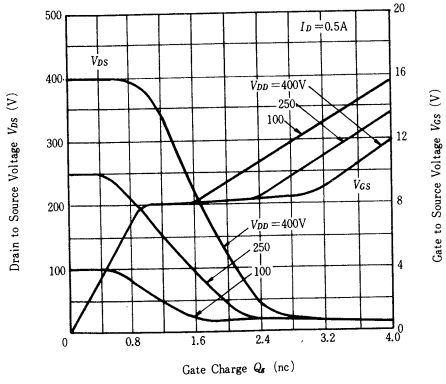
SWITCHING CHARACTERISTICS



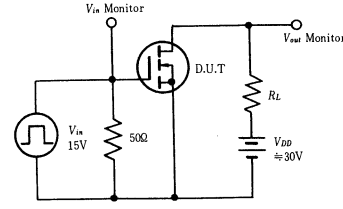
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



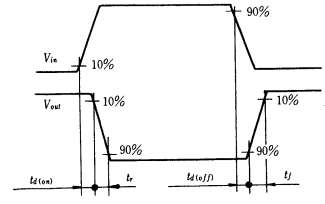
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS

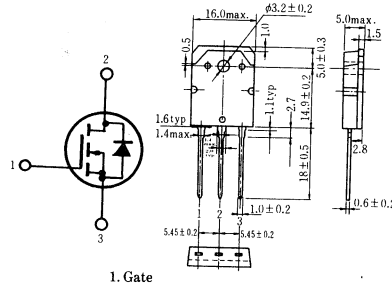


2SK399

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

Complementary pair with 2SJ113



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

(TO-3P)

■ FEATURES

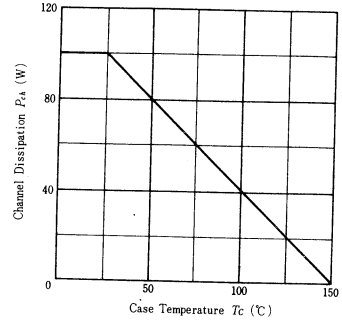
- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Control, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	10	A
Drain Peak Current	$I_{D(peak)}$	15	A
Body-Drain Diode Reverse Drain Current	I_{DR}	10	A
Channel Dissipation	P_{ch}*	100	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



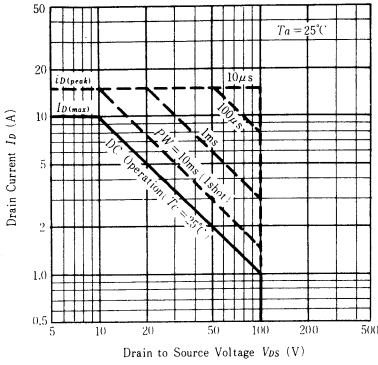
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	100	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	0.20	0.25	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	1.0	1.25	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=5A, V_{DS}=10V*	1.5	2.0	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	800	—	pF
Output Capacitance	C_{oss}		—	500	—	pF
Reverse Transfer Capacitance	C_{rss}		—	70	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	15	—	ns
Rise Time	t_r		—	35	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	60	—	ns
Fall Time	t_f		—	50	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=5A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=5A, V_{GS}=0 di_F/dt=50A/μs	—	300	—	ns

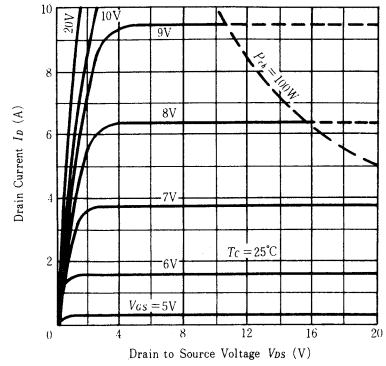
*Pulse Test

HITACHI

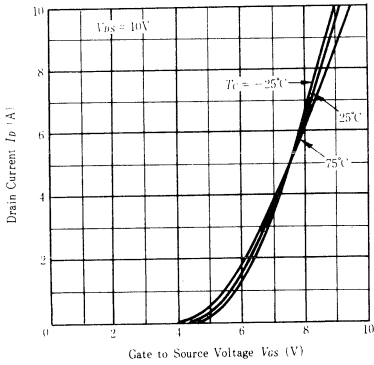
MAXIMUM SAFE OPERATION AREA



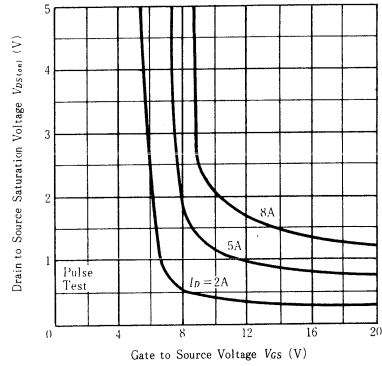
TYPICAL OUTPUT CHARACTERISTICS



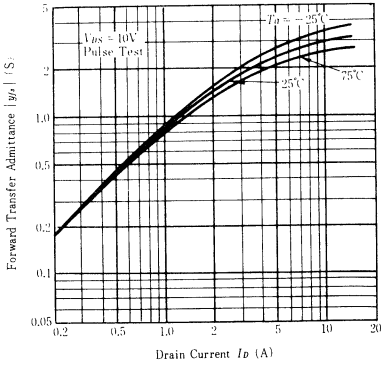
TYPICAL TRANSFER CHARACTERISTICS



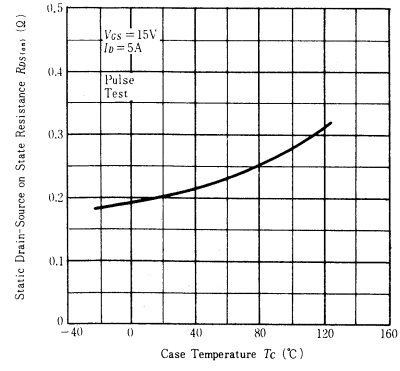
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



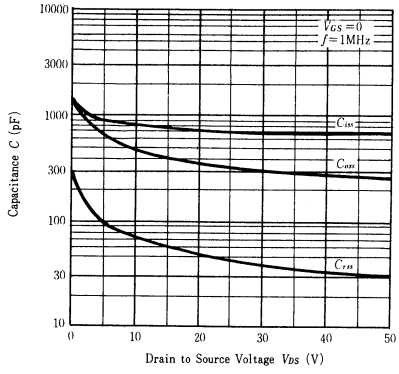
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



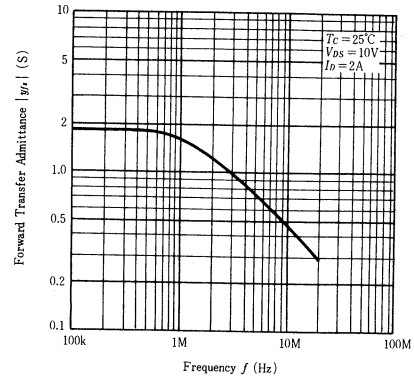
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



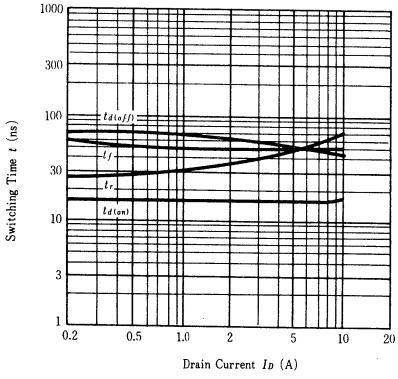
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



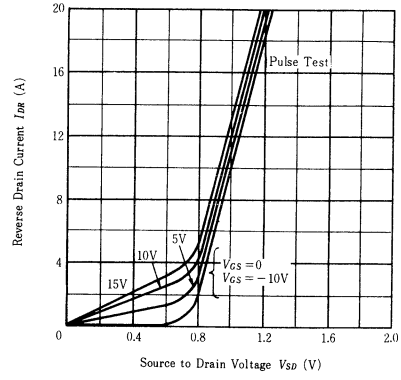
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



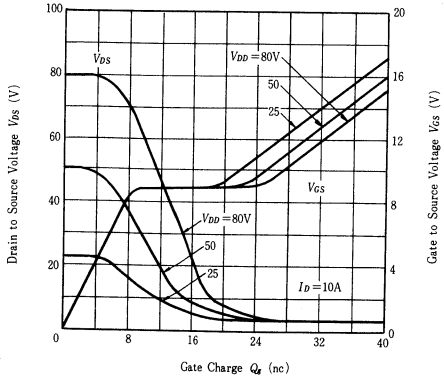
SWITCHING CHARACTERISTICS



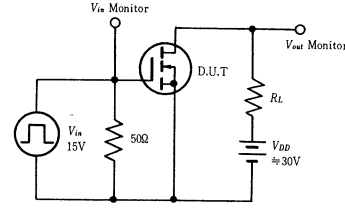
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



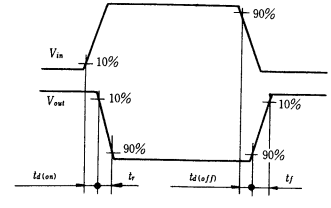
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS

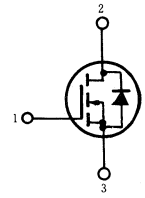


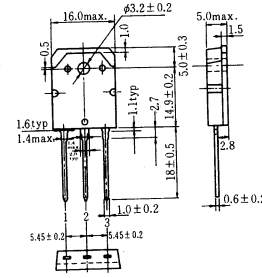
2SK400

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

Complementary pair with 2SJ114





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

(TO-3P)

■ FEATURES

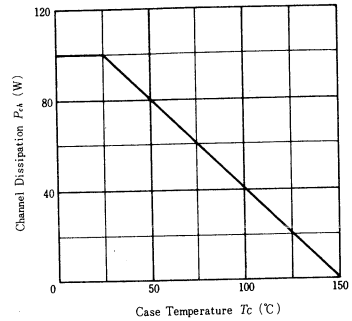
- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	200	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Drain Peak Current	$I_{D(peak)}$	12	A
Body-Drain Diode Reverse Drain Current	I_{DR}	8	A
Channel Dissipation	P_{ch}*	100	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

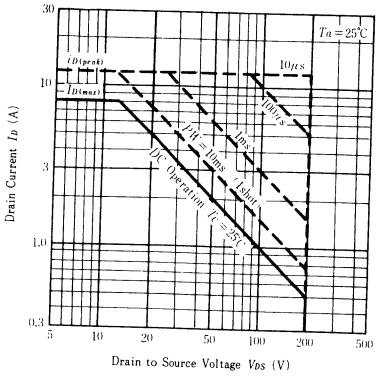


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

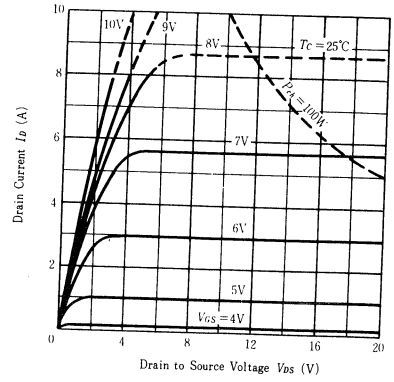
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	200	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=160V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=4A, V_{GS}=15V*	—	0.5	0.7	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=4A, V_{GS}=15V*	—	2.0	2.8	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=4A, V_{DS}=10V*	1.0	1.8	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	750	—	pF
Output Capacitance	C_{oss}		—	300	—	pF
Reverse Transfer Capacitance	C_{rss}		—	60	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	15	—	ns
Rise Time	t_r		—	25	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	70	—	ns
Fall Time	t_f		—	40	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=4A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=4A, V_{GS}=0 di_F/dt=50A/μs	—	300	—	ns

*Pulse Test

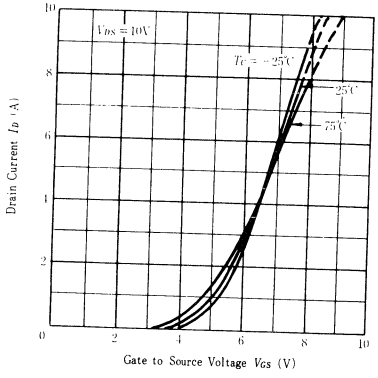
MAXIMUM SAFE OPERATION AREA



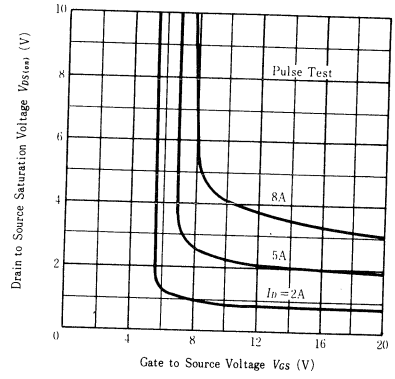
TYPICAL OUTPUT CHARACTERISTICS



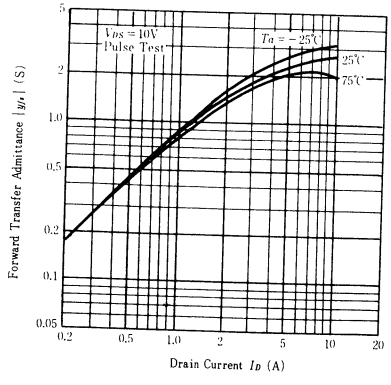
TYPICAL TRANSFER CHARACTERISTICS



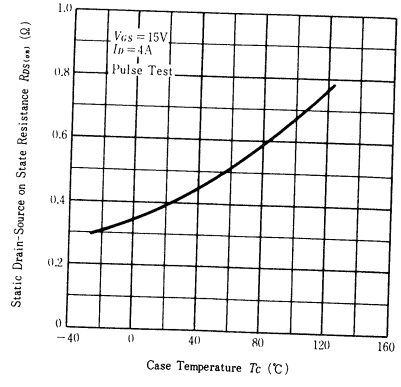
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



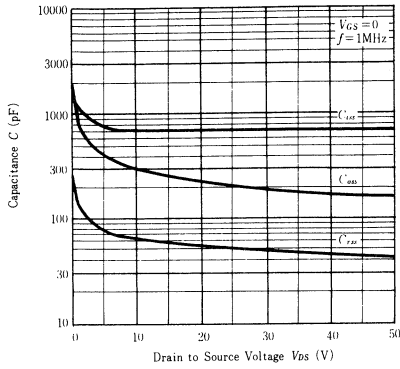
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



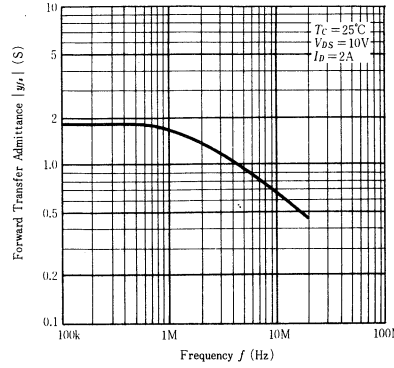
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



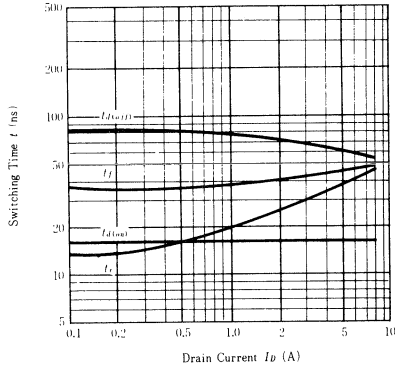
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



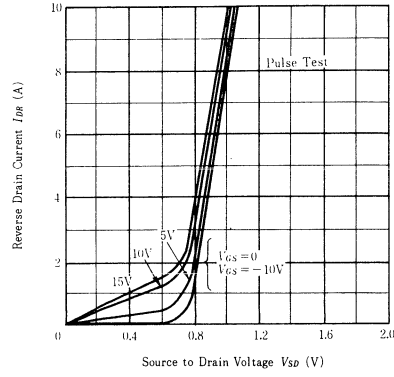
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



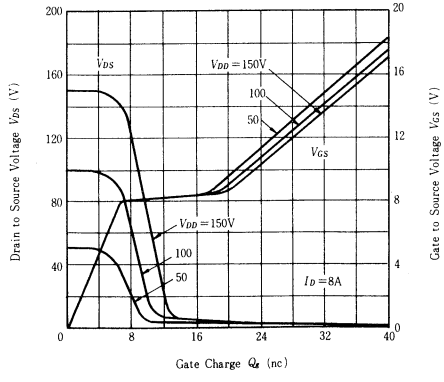
SWITCHING CHARACTERISTICS



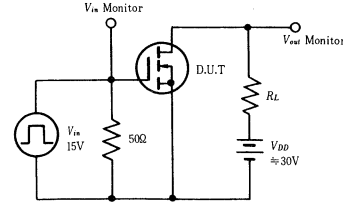
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



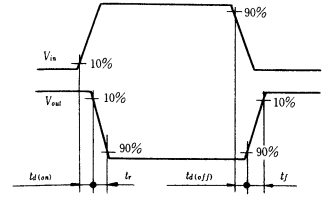
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



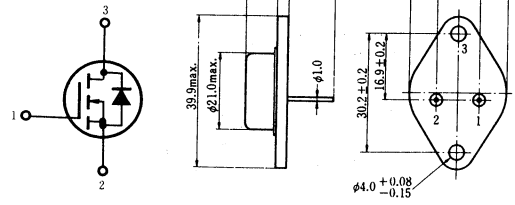
2SK401

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Control, and Ultrasonic Power Oscillators.



1. Gate
2. Source
3. Drain (Case)

(Dimensions in mm)

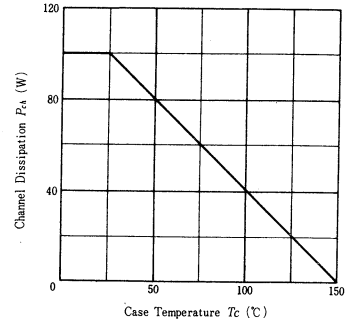
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	250	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	10	A
Drain Peak Current	$I_{D(peak)}$	15	A
Body-Drain Diode Reverse Drain Current	I_{DR}	10	A
Channel Dissipation	P_{ch}*	100	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

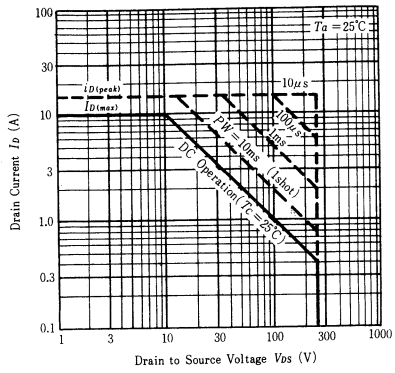


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

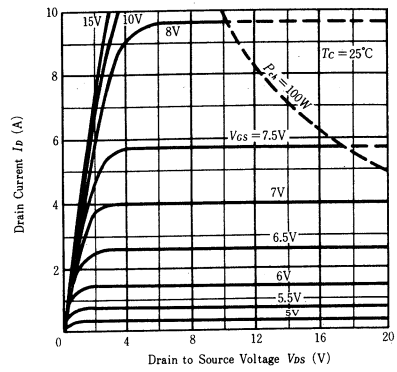
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	250	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=200V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	0.3	0.4	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	1.5	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=5A, V_{DS}=10V*	1.6	2.5	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	1400	—	pF
Output Capacitance	C_{oss}		—	500	—	pF
Reverse Transfer Capacitance	C_{rss}		—	35	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	13	—	ns
Rise Time	t_r		—	52	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	120	—	ns
Fall Time	t_f		—	60	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=5A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=5A, V_{GS}=0 di_F/dt=100A/μs	—	400	—	ns

*Pulse Test

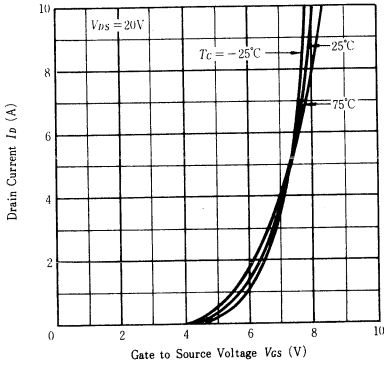
MAXIMUM SAFE OPERATION AREA



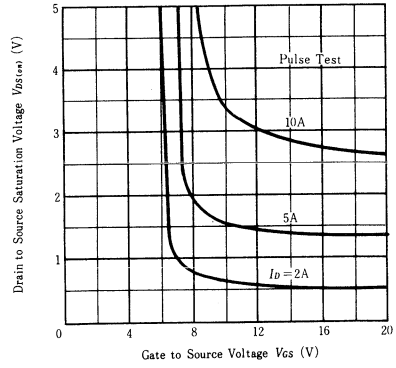
TYPICAL OUTPUT CHARACTERISTICS



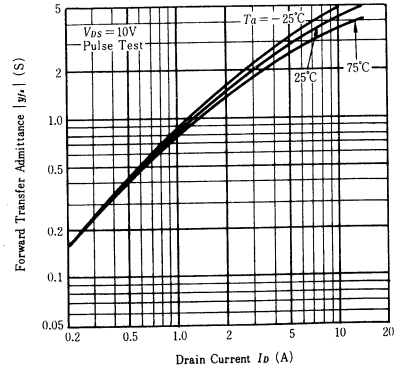
TYPICAL TRANSFER CHARACTERISTICS



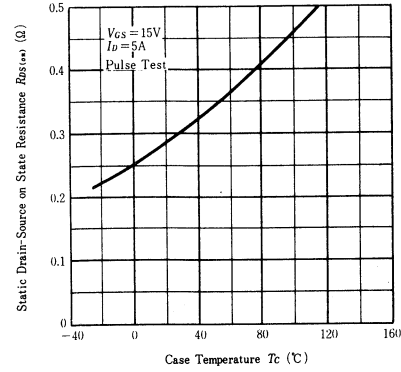
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



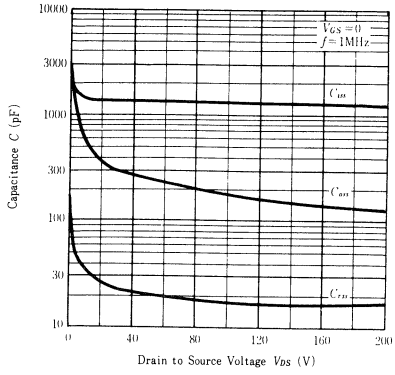
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



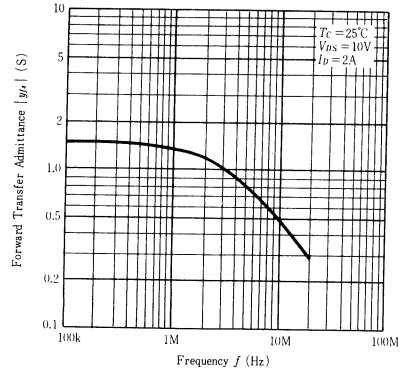
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



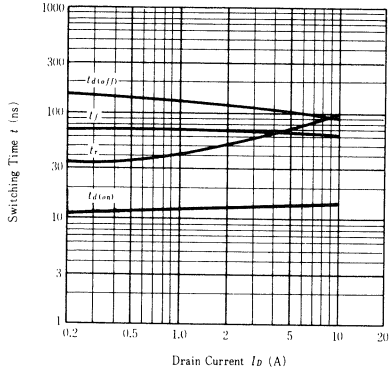
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



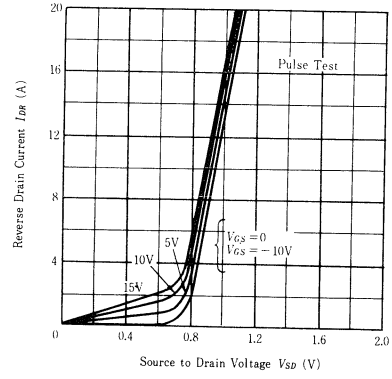
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



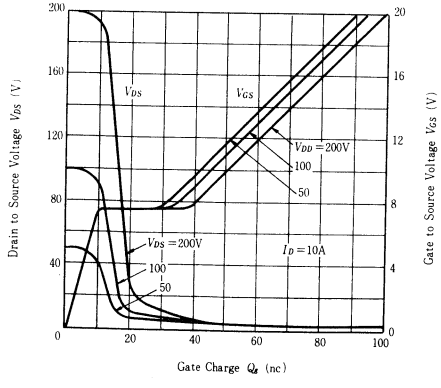
SWITCHING CHARACTERISTICS



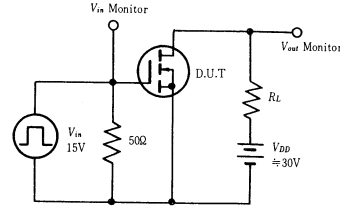
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



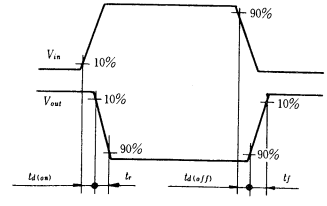
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



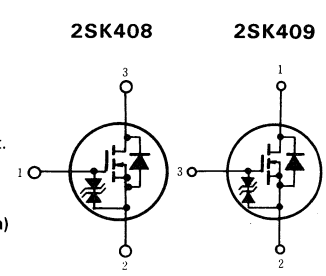
2SK408, 2SK409

SILICON N-CHANNEL MOS FET

HF/VHF POWER AMPLIFIER

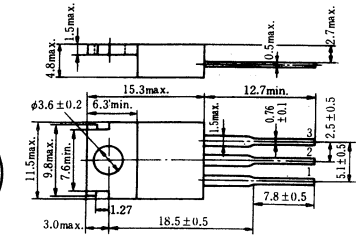
■ FEATURES

- High Breakdown Voltage.
- You Can Decrease Handling Current.
- Included Gate Protection Diode.
- No Secondary-Breakdown.
- Wide A.S.O. (Area of Safe Operation)
- Simple Bias Circuitry
- No Thermal Runaway.



2SK408
1. Gate
2. Source
3. Drain

2SK409
1. Drain
2. Source
3. Gate



(Dimensions in mm)

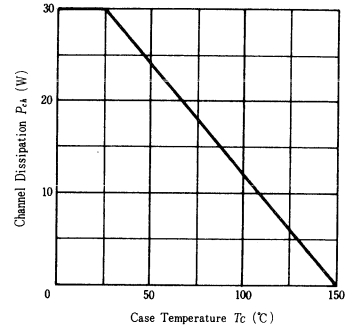
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	180	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	2	A
Channel Dissipation	P_{ch}*	30	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

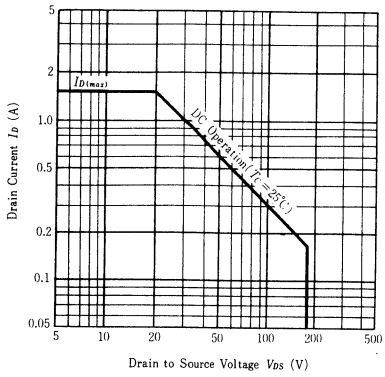


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

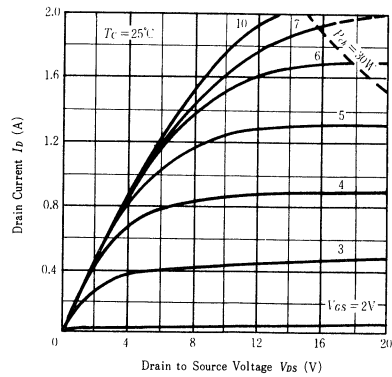
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Power Output	P_O	V_{DS}=80V, f=28MHz	5	10	—	W
Drain Efficiency	η	I_{DQ}=50mA, P_{in}=150mW	—	80	—	%
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	180	—	—	V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	0.5	—	3.0	V
Drain Current	I_{DSS}	V_{DS}=140V, V_{GS}=0	—	—	1.0	mA
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=1.0A, V_{GS}=10V*	—	6.5	8.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=1.0A, V_{DS}=20V*	0.2	0.3	—	S
Input Capacitance	C_{iss}	V_{GS}=5V, V_{DS}=0, f=1MHz	—	100	—	pF
Output Capacitance	C_{oss}	V_{GS}=−5V, V_{DS}=50V, f=1MHz	—	20	—	pF
Reverse Transfer Capacitance	C_{rss}	V_{GD}=−50V, f=1MHz	—	0.2	—	pF
Power Output	P_O	V_{DS}=80V, f=28MHz	—	10	—	W_{PEP}
Power Gain	P.G	Δf=20kHz, IMD≦−30dB	—	20	—	dB

*Pulse Test

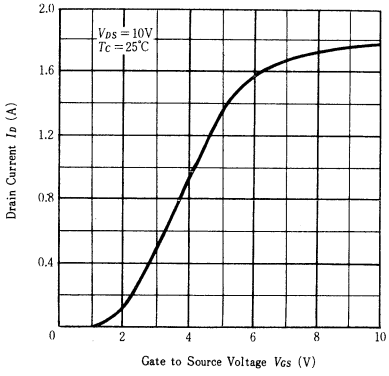
MAXIMUM SAFE OPERATION AREA



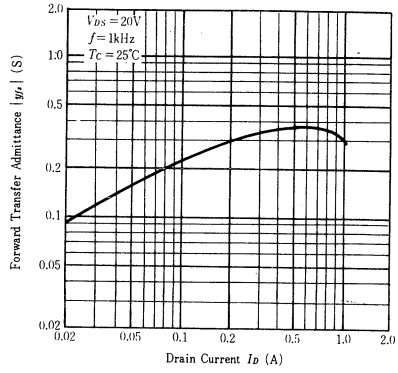
TYPICAL OUTPUT CHARACTERISTICS



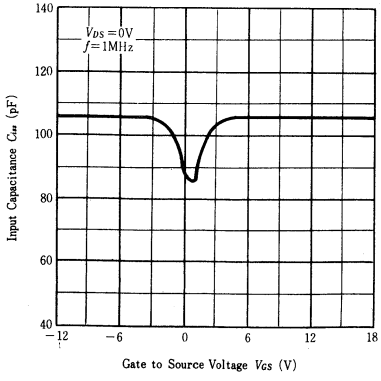
TYPICAL TRANSFER CHARACTERISTICS



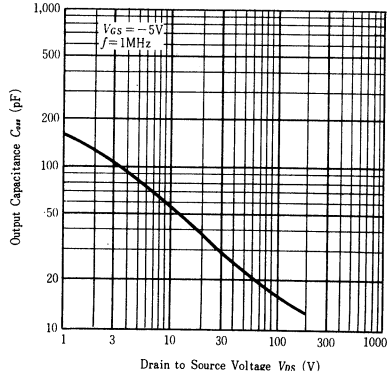
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



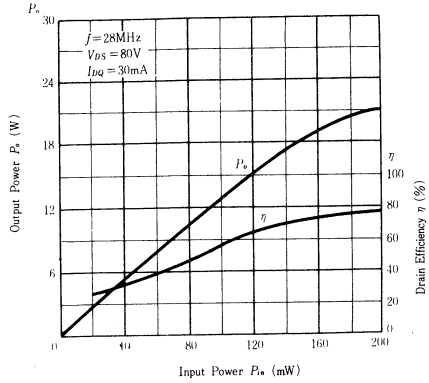
INPUT CAPACITANCE VS. GATE-SOURCE VOLTAGE



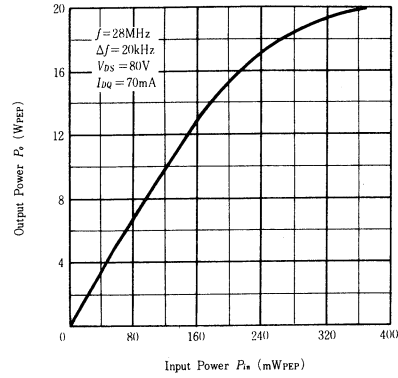
OUTPUT CAPACITANCE VS. GATE-SOURCE VOLTAGE



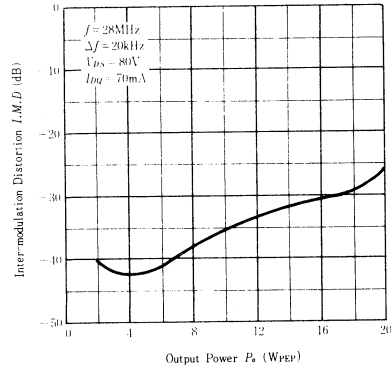
OUTPUT POWER, DRAIN EFFICIENCY VS. INPUT POWER



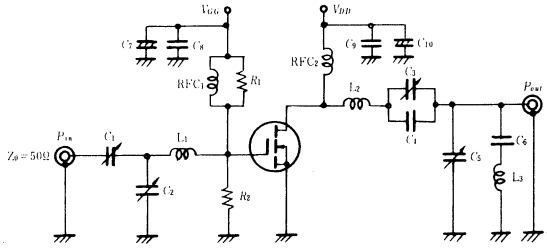
OUTPUT POWER VS. INPUT POWER (2 TONES)



INTER-MODULATION DISTORTION VS. OUTPUT POWER



28MHz Pout TEST CIRCUIT



C_1, C_2, C_3 = ~50pF
C_4 = 68pF
C_5 = ~20pF
C_6 = 1.5pF
C_7, C_9 = 0.1μF
C_8 = 4.7μF
C_{10} = 22μF
L_1 : ID=12mm, d=1.5mm, T=6T
L_2 : ID=12mm, d=1.5mm, T=9T
L_3 : ID=12mm, d=1.5mm, T=5T

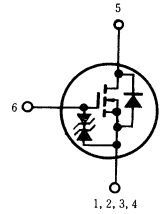
2SK410

SILICON N-CHANNEL MOS FET

HF/VHF POWER AMPLIFIER

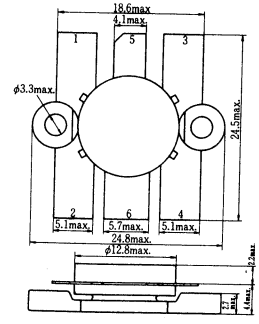
■ FEATURES

- High Breakdown Voltage.
- You Can Decrease Handling Current.
- Included Gate Protection Diode.
- No Secondary-Breakdown.
- Wide Area of Safe Operation.
- Simple Bias Circuitry.
- No Thermal Runaway.



1. Source
2. Source
3. Source
4. Source
5. Drain
6. Gate

(Dimensions in mm)



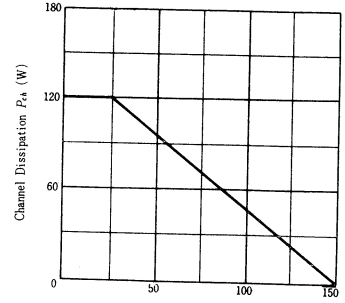
(RF-PAK)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	180	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Channel Dissipation	P_{ch}*	120	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Power Output	P_O	V_{DS}=80V, f=28MHz	140	180	—	W
Drain Efficiency	η	I_{DQ}=0.1A, P_{in}=5W	—	80	—	%
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	180	—	—	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	0.5	—	3.0	V
Drain Current	I_{DSS}	V_{DS}=140V, V_{GS}=0	—	—	1.0	mA
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=4A, V_{GS}=10V*	—	3.8	6.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=3A, V_{DS}=20V*	0.9	1.25	—	S
Input Capacitance	C_{iss}	V_{GS}=5V, V_{DS}=0, f=1MHz	—	440	—	pF
Output Capacitance	C_{oss}	V_{GS}=−5V, V_{DS}=50V, f=1MHz	—	75	—	pF
Reverse Transfer Capacitance	C_{rss}	V_{GD}=−50V, f=1MHz	—	0.5	—	pF
Power Output	P_O	V_{DS}=80V, f=28MHz	—	100	—	W_{PEP}
Power Gain	P.G	Δf=20kHz, IMD≦−30dB	—	17	—	dB

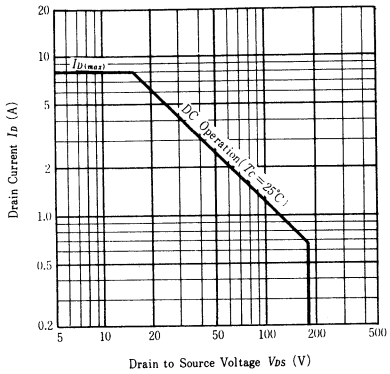
*Pulse Test

■ CAUTION: OPERATING HAZARDS

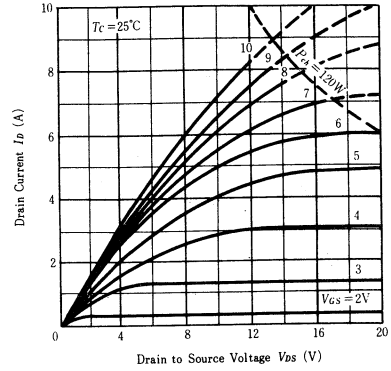
Beryllium Oxide Ceramics have been employed in these products.
Since dust or fume of the material is highly poison to the human body, please do not treat them mechanically or chemically in the manner which might expose them to the air. And it should never be thrown out with general industrial or domestic waste.

HITACHI

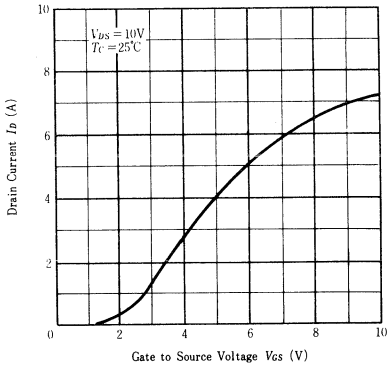
MAXIMUM SAFE OPERATION AREA



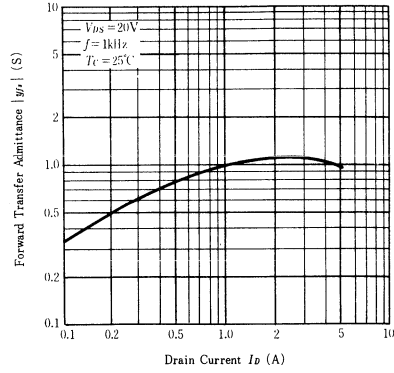
TYPICAL OUTPUT CHARACTERISTICS



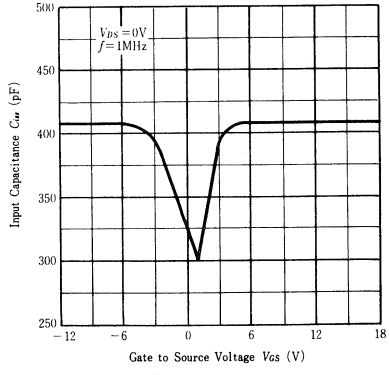
TYPICAL TRANSFER CHARACTERISTICS



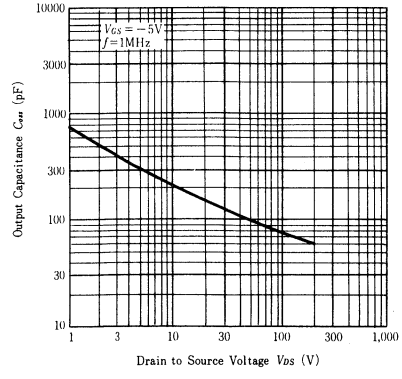
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



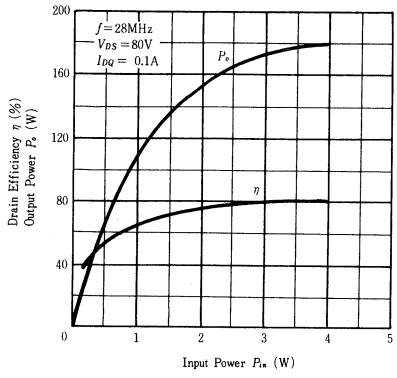
INPUT CAPACITANCE VS. GATE-SOURCE VOLTAGE



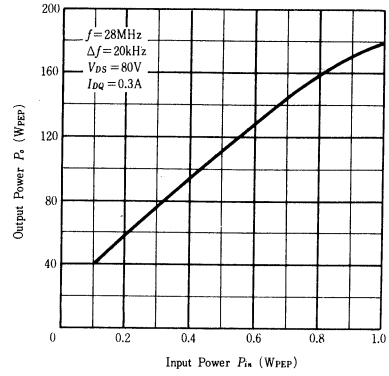
OUTPUT CAPACITANCE VS. GATE-SOURCE VOLTAGE



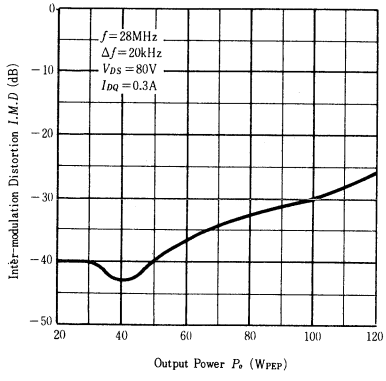
OUTPUT POWER, DRAIN EFFICIENCY VS. INPUT POWER



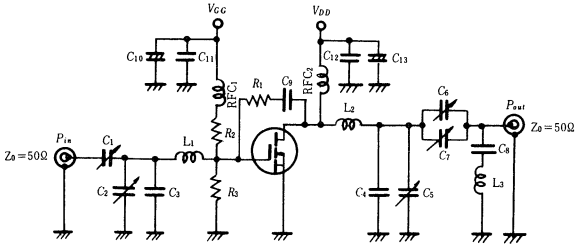
OUTPUT POWER VS. INPUT POWER (2 TONES)



INTER-MODULATION DISTORTION VS. OUTPUT POWER



28MHz Pout TEST CIRCUIT

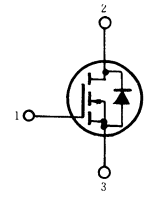


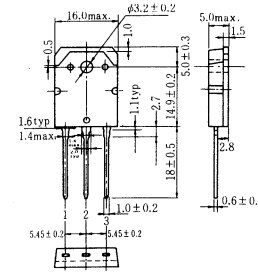
C_1, C_6	= ~50pF	L_1	: ID=12mm, d=1.5mm, T=7T
C_2, C_5	= ~20pF	L_2	: ID=12mm, d=1.5mm, T=5T
C_3, C_4	= 10pF	L_3	: ID=12mm, d=1.5mm, T=5T
C_7	= 32pF	R_1	= 1kΩ
C_8	= 15pF	R_2, R_3	= 100Ω
C_9, C_{11}, C_{12}	= 0.1μF	RFC_1	= FC 15φ, d=1mm, T=3T
C_{10}	= 4.7μF	RFC_2	= FC 6φ, d=1mm, T=4T
C_{13}	= 22μF		

2SK412

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

(TO-3P)

■ FEATURES

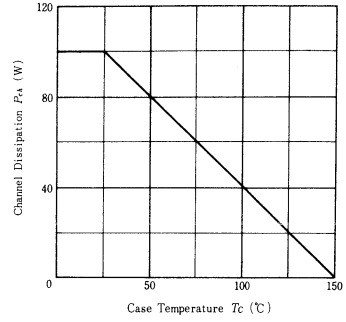
- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Control, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	250	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	10	A
Drain Peak Current	$I_{D(peak)}$	15	A
Body-Drain Diode Reverse Drain Current	I_{DR}	10	A
Channel Dissipation	P_{ch}*	100	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

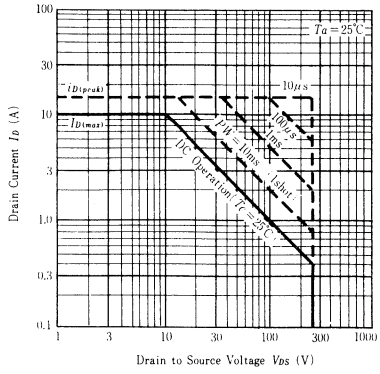


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

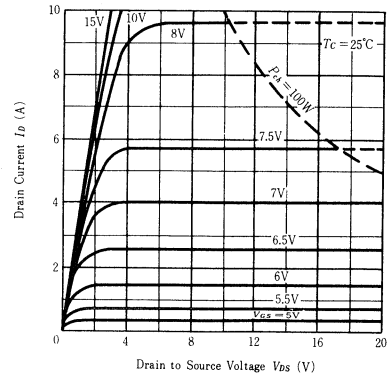
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	250	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=200V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	0.3	0.4	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	1.5	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=5A, V_{DS}=10V*	1.6	2.5	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	1400	—	pF
Output Capacitance	C_{oss}		—	500	—	pF
Reverse Transfer Capacitance	C_{rss}		—	35	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	13	—	ns
Rise Time	t_r		—	52	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	120	—	ns
Fall Time	t_f		—	60	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=5A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=5A, V_{GS}=0 di_F/dt=100A/μs	—	400	—	ns

*Pulse Test

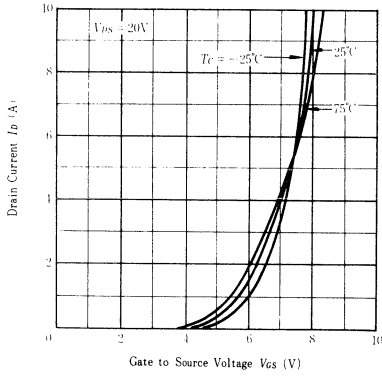
MAXIMUM SAFE OPERATION AREA



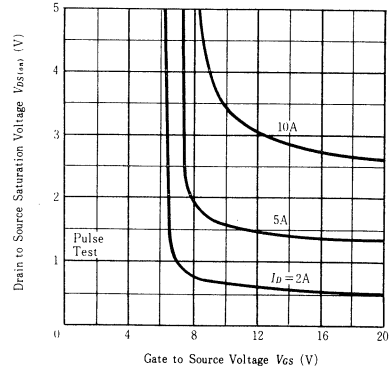
TYPICAL OUTPUT CHARACTERISTICS



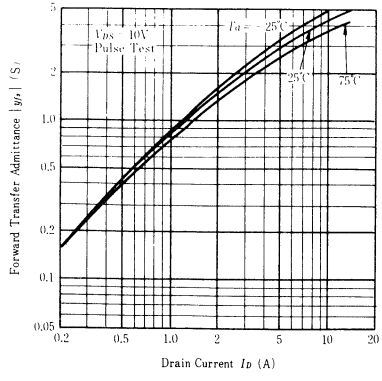
TYPICAL TRANSFER CHARACTERISTICS



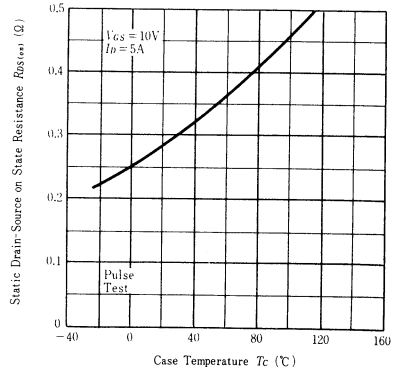
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



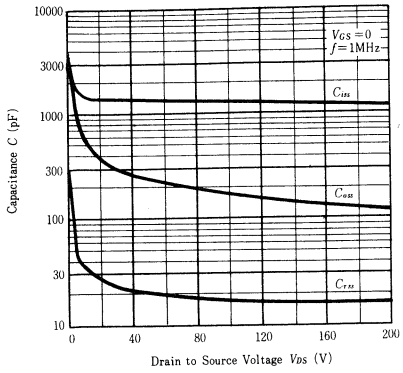
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



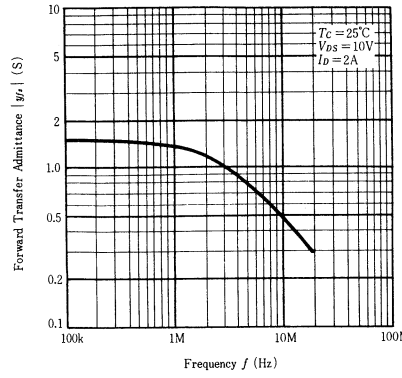
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



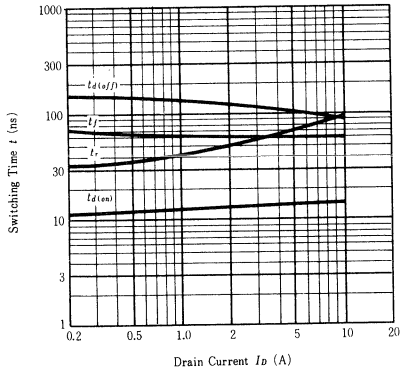
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



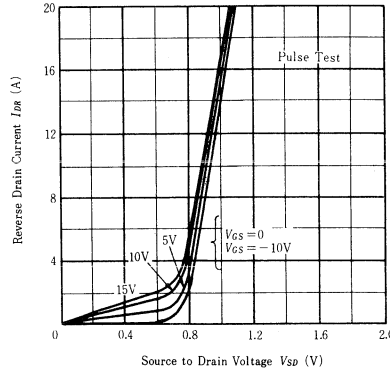
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



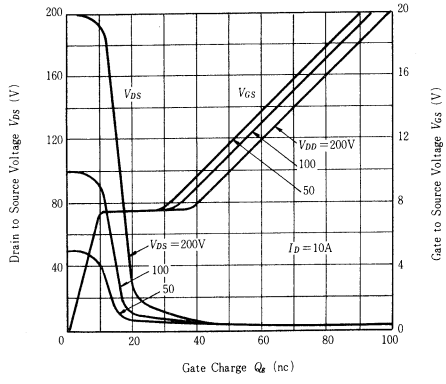
SWITCHING CHARACTERISTICS



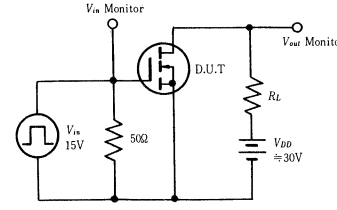
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



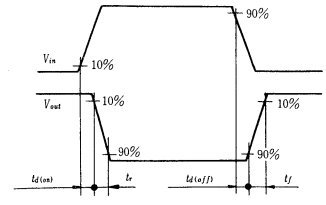
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



2SK413, 2SK414

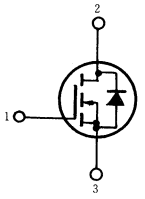
SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

Complementary pair with 2SJ118, 119

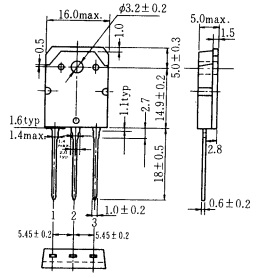
■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, PWM Amplifiers, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)



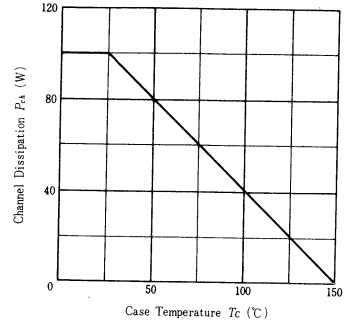
(TO-3P)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SK413	2SK414	
Drain-Source Voltage	V_{DSS}	140	160	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	8		A
Drain Peak Current	$I_{D(peak)}$	12		A
Body-Drain Diode Reverse Drain Current	I_{DR}	8		A
Channel Dissipation	P_{ch}*	100		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



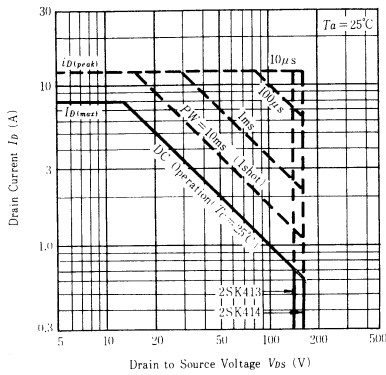
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK413	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	140	—	—	V
	2SK414			160	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	2SK413	I_{DSS}	V_{DS}=120V, V_{GS}=0	—	—	1	mA
	2SK414		V_{DS}=140V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	5.0	V
Static Drain-Source On State Resistance		$R_{DS(on)}$	I_D=4A, V_{GS}=15V*	—	0.4	0.5	Ω
Drain-Source Saturation Voltage		$V_{DS(on)}$	I_D=4A, V_{GS}=15V*	—	1.6	2.0	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=4A, V_{DS}=10V*	1.0	2.0	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	800	—	pF
Output Capacitance		C_{oss}		—	330	—	pF
Reverse Transfer Capacitance		C_{rss}		—	60	—	pF
Turn-on Delay Time		$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=2Ω	—	15	—	ns
Rise Time		t_r		—	35	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	60	—	ns
Fall Time		t_f		—	50	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=4A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=4A, V_{GS}=0 di_F/dt=50A/μs	—	250	—	ns

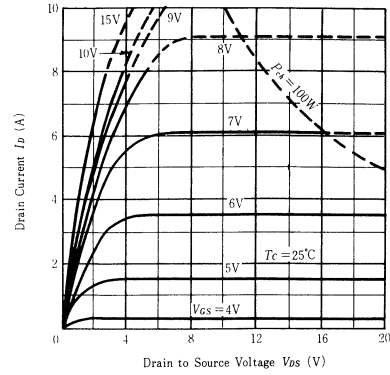
*Pulse Test

HITACHI

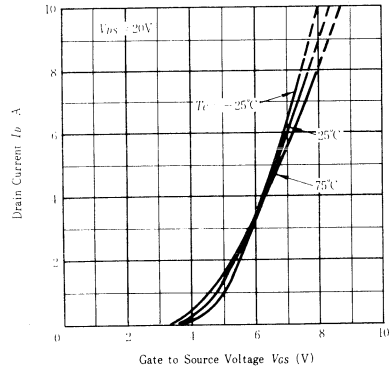
MAXIMUM SAFE OPERATION AREA



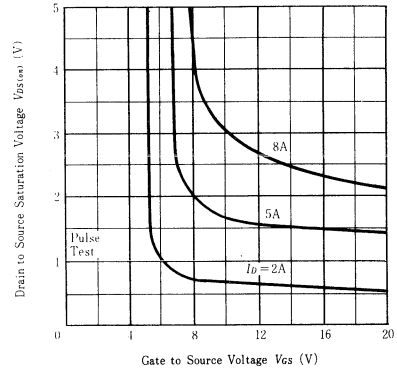
TYPICAL OUTPUT CHARACTERISTICS



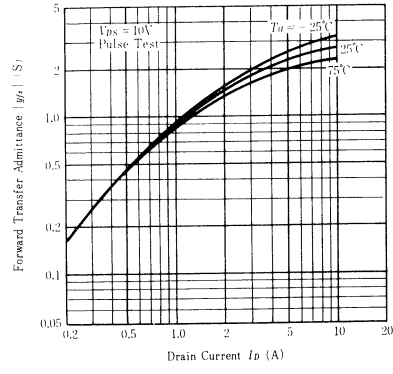
TYPICAL TRANSFER CHARACTERISTICS



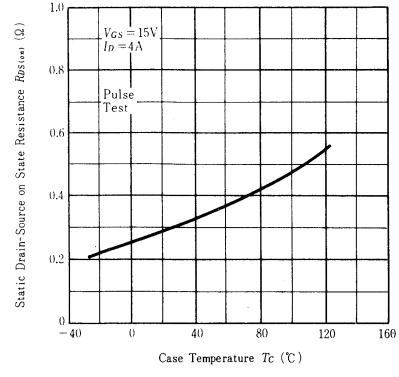
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



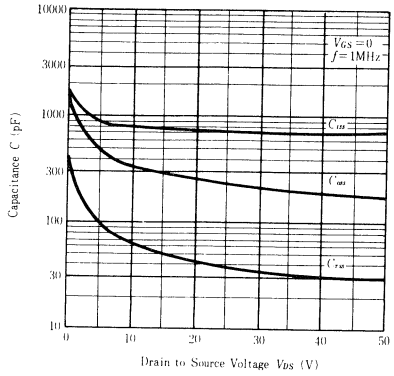
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



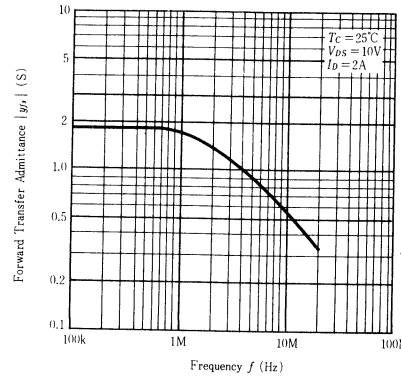
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



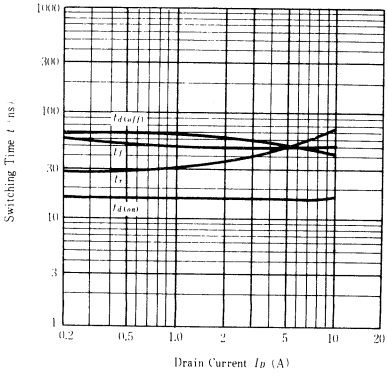
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



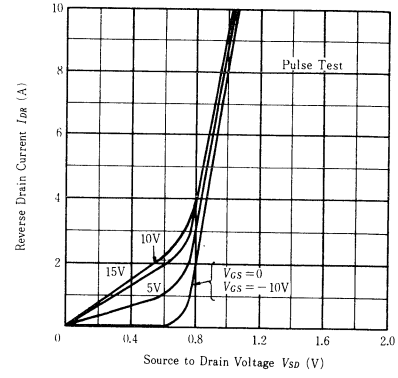
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



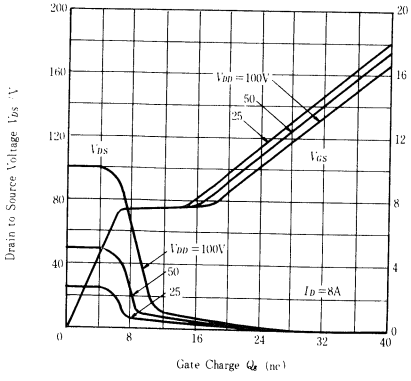
SWITCHING CHARACTERISTICS



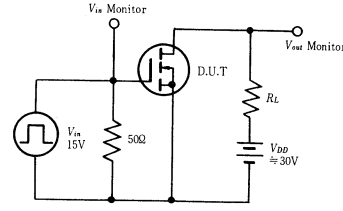
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



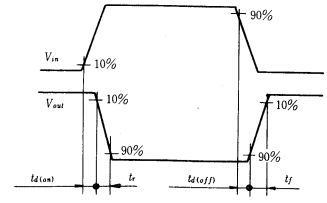
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



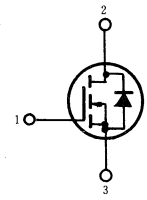
2SK415

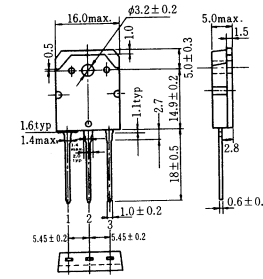
SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- High Breakdown Voltage.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, and Ultrasonic Power Oscillators.





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

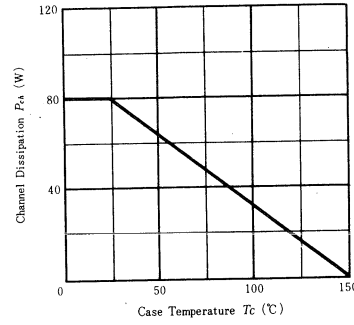
(TO-3P)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	800	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	3	A
Drain Peak Current	$I_{D(peak)}$	6	A
Body-Drain Diode Reverse Drain Current	I_{DR}	3	A
Channel Dissipation	P_{ch}*	80	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

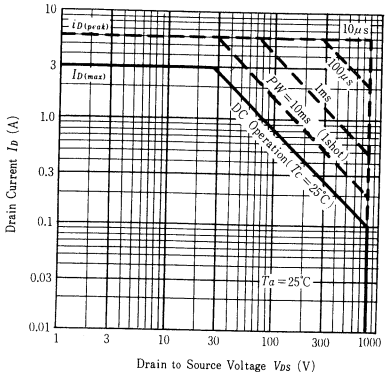


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

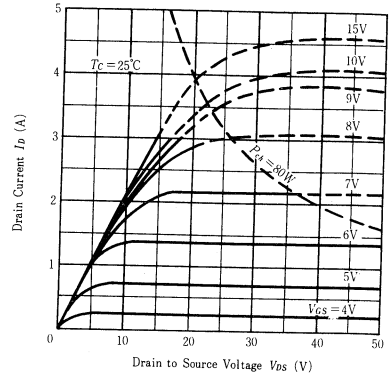
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	800	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=640V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=2A, V_{GS}=15V*	—	5.0	6.0	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=2A, V_{GS}=15V*	—	10.0	12.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=2A, V_{DS}=20V*	0.4	0.7	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	470	—	pF
Output Capacitance	C_{oss}		—	120	—	pF
Reverse Transfer Capacitance	C_{rss}		—	22	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	15	—	ns
Rise Time	t_r		—	35	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	85	—	ns
Fall Time	t_f		—	35	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=2A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=2A, V_{GS}=0 di_F/dt=100A/μs	—	700	—	ns

*Pulse Test

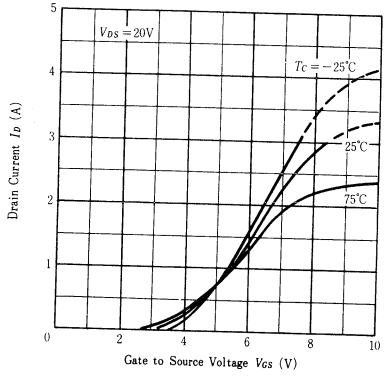
MAXIMUM SAFE OPERATION AREA



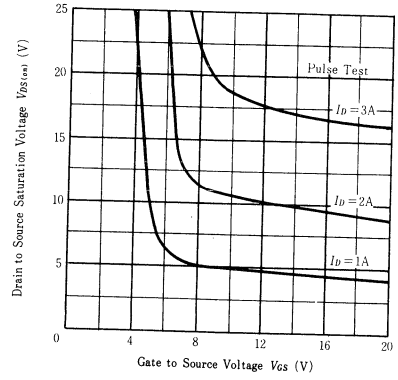
TYPICAL OUTPUT CHARACTERISTICS



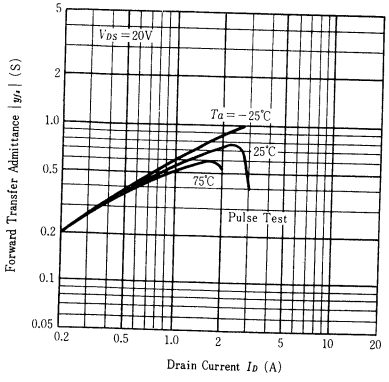
TYPICAL TRANSFER CHARACTERISTICS



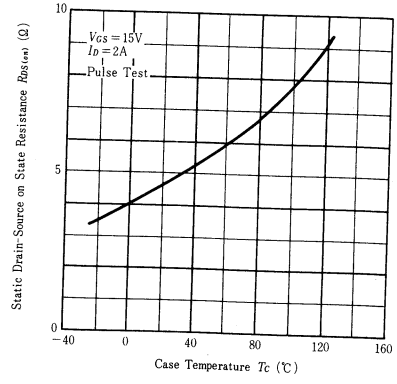
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



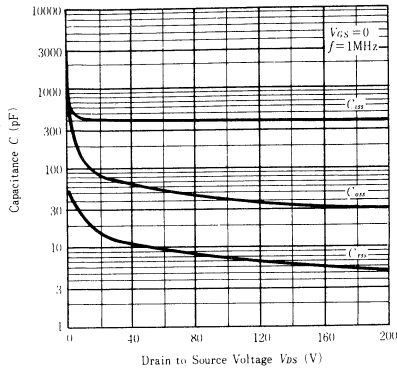
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



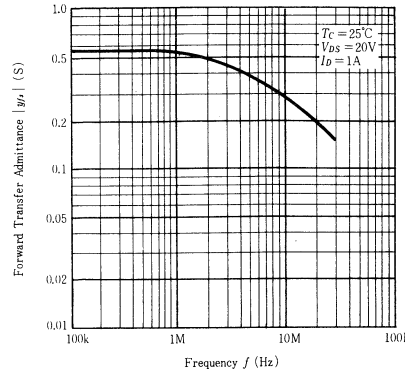
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



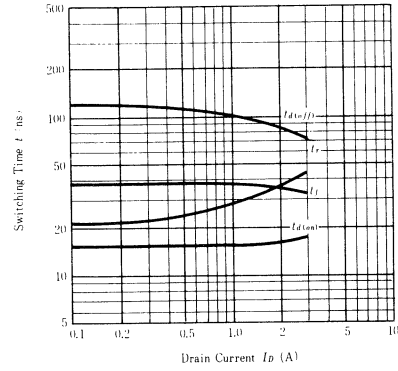
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



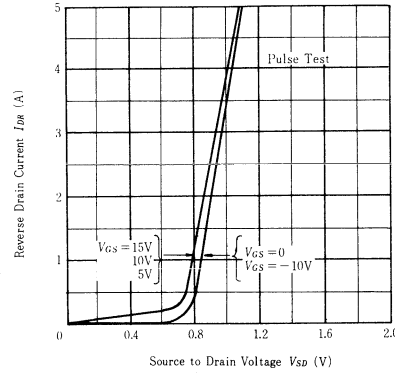
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



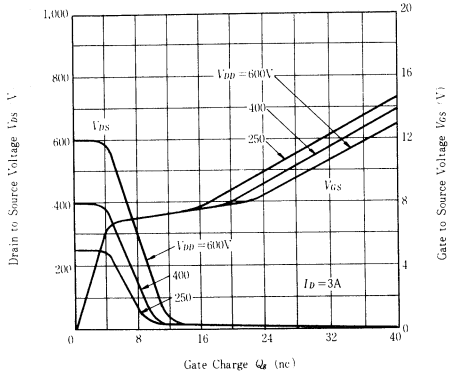
SWITCHING CHARACTERISTICS



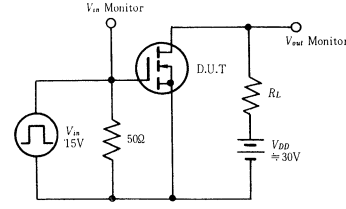
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



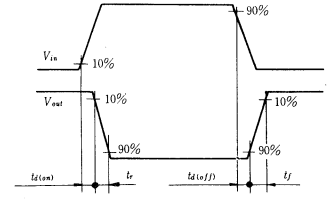
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



2SK416Ⓛ,2SK416Ⓢ

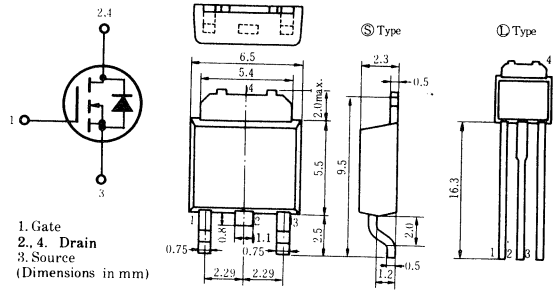
SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

Complementary pair with 2SJ120

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, and Bubble Memory Driver.



1. Gate
2., 4. Drain
3. Source
(Dimensions in mm)

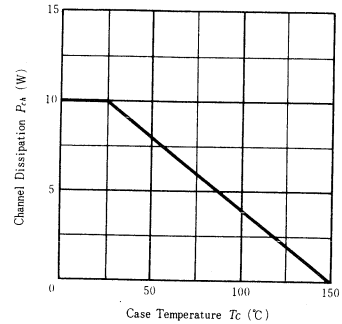
(DPAK)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	40	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	2	A
Drain Peak Current	$I_{D(peak)}$	4	A
Body-Drain Diode Reverse Drain Current	I_{DR}	2	A
Channel Dissipation	P_{ch}*	10	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



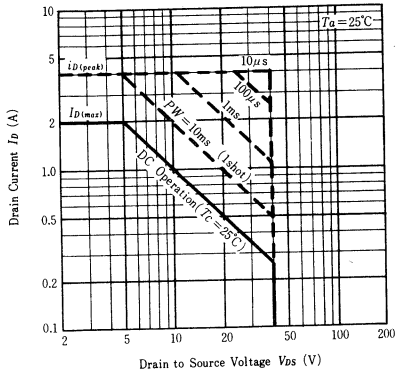
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	40	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=35V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	4.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=1A, V_{GS}=15V*	—	0.5	0.8	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=1A, V_{GS}=15V*	—	0.5	0.8	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=1A, V_{DS}=10V*	0.2	0.4	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	170	—	pF
Output Capacitance	C_{oss}		—	160	—	pF
Reverse Transfer Capacitance	C_{rss}		—	30	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=1A, V_{GS}=15V R_L=30Ω	—	7	—	ns
Rise Time	t_r		—	18	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	14	—	ns
Fall Time	t_f		—	21	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=1A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=1A, V_{GS}=0 di_F/dt=50A/μs	—	90	—	ns

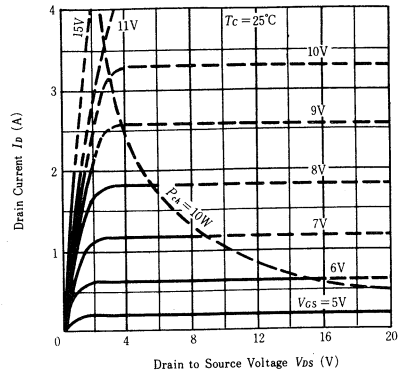
*Pulse Test

HITACHI

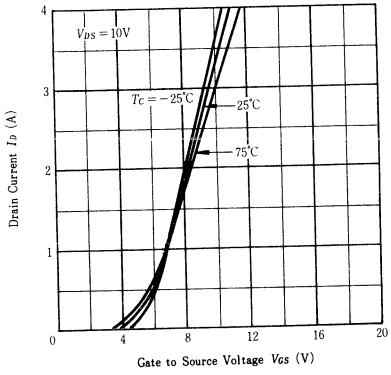
MAXIMUM SAFE OPERATION AREA



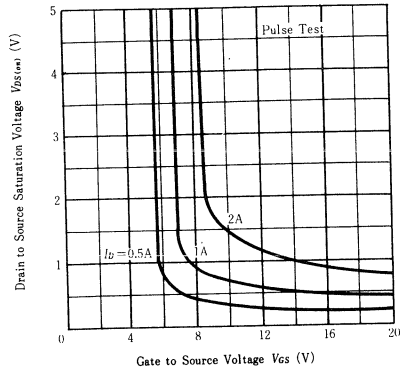
TYPICAL OUTPUT CHARACTERISTICS



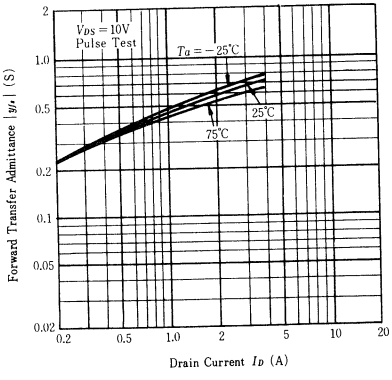
TYPICAL TRANSFER CHARACTERISTICS



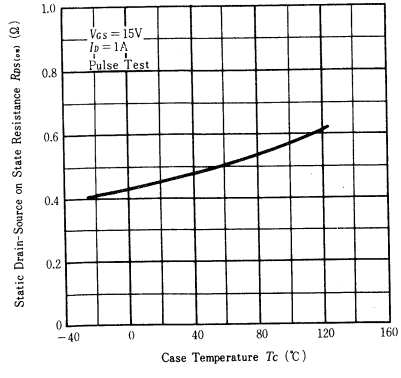
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



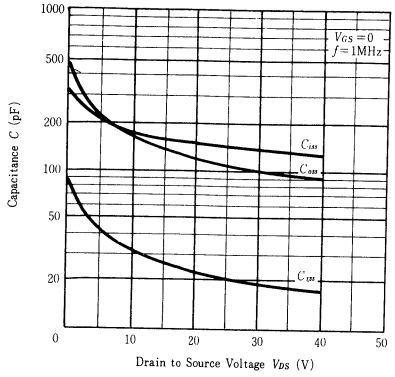
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



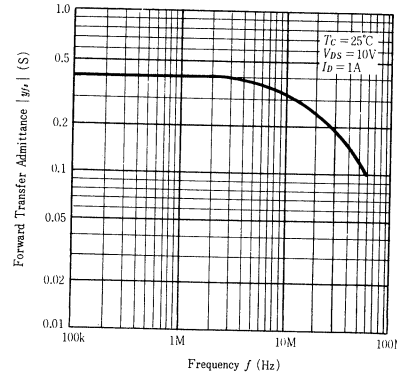
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



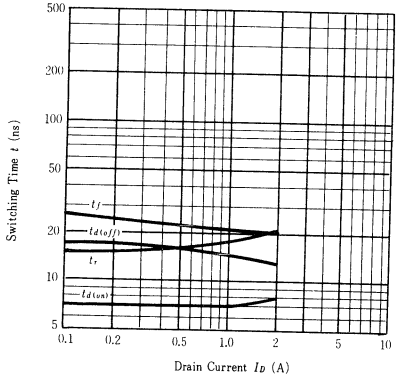
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



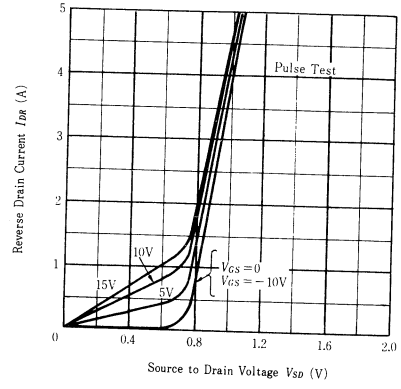
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



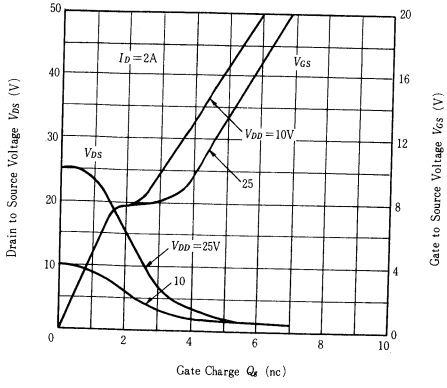
SWITCHING CHARACTERISTICS



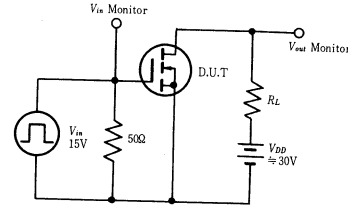
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



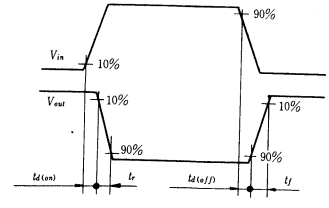
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS

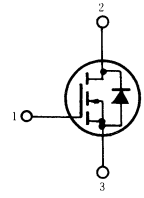


2SK428

SILICON N-CHANNEL MOS FET

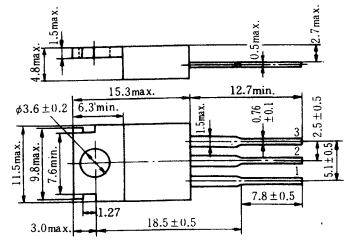
HIGH SPEED POWER SWITCHING, HIGH FREQUENCY POWER AMPLIFIER

Complementary pair with 2SJ122



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)



(JEDEC TO-220AB)

■ FEATURES

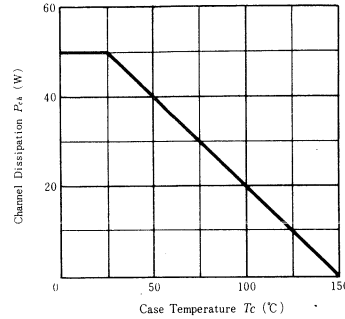
- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, PWM Amplifiers, and Ultrasonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	10	A
Drain Peak Current	$I_{D(peak)}$	15	A
Body-Drain Diode Reverse Drain Current	I_{DR}	10	A
Channel Dissipation	P_{ch}*	50	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

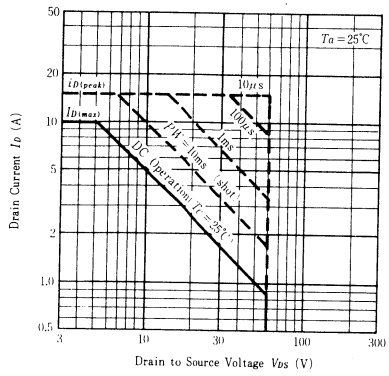


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

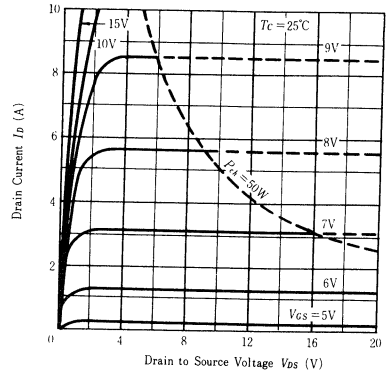
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	60	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	0.1	0.15	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=5A, V_{GS}=15V*	—	0.5	0.75	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=5A, V_{DS}=10V*	1.5	2.2	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	900	—	pF
Output Capacitance	C_{oss}		—	700	—	pF
Reverse Transfer Capacitance	C_{rss}		—	120	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V, R_L=15Ω	—	15	—	ns
Rise Time	t_r		—	45	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	55	—	ns
Fall Time	t_f		—	65	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=5A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=5A, V_{GS}=0, di_F/dt=50A/μs	—	300	—	ns

*Pulse Test

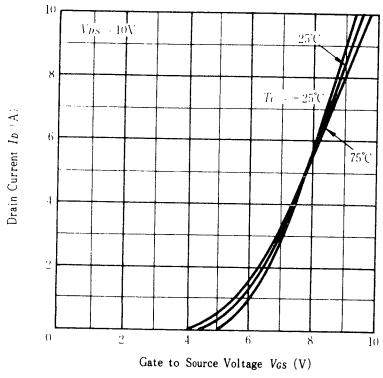
MAXIMUM SAFE OPERATION AREA



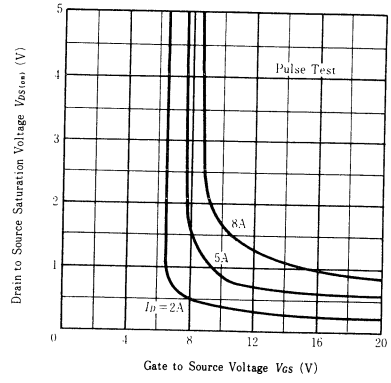
TYPICAL OUTPUT CHARACTERISTICS



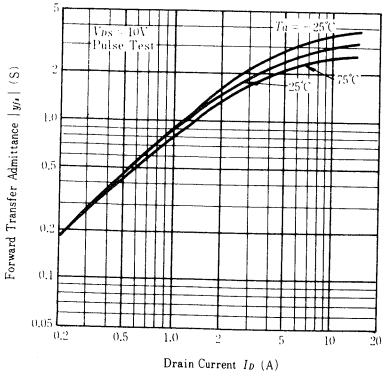
TYPICAL TRANSFER CHARACTERISTICS



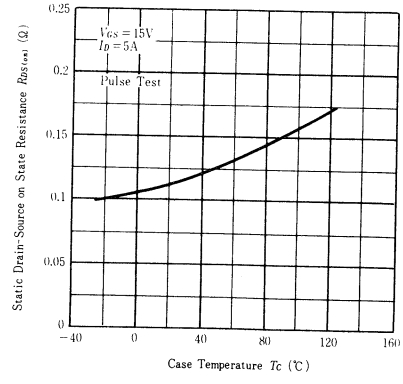
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



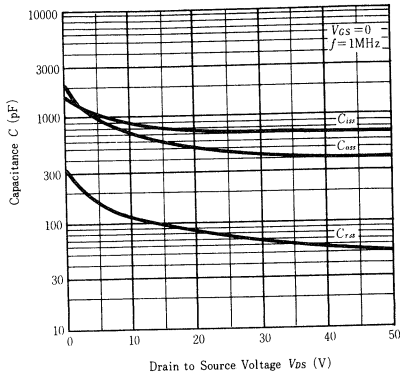
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



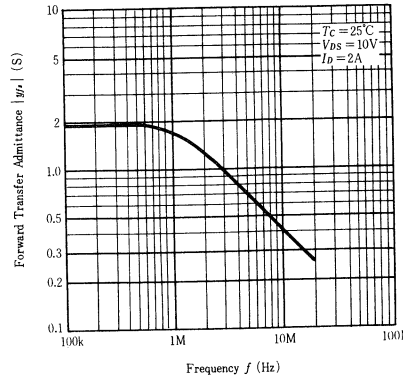
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



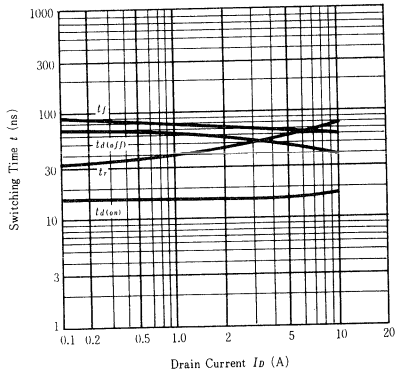
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



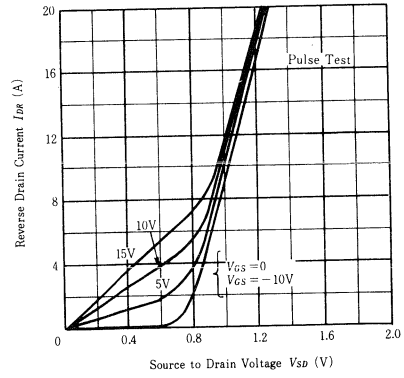
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



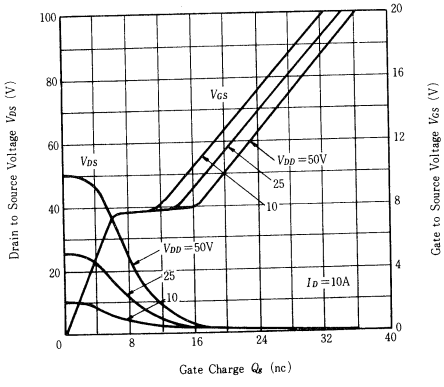
SWITCHING CHARACTERISTICS



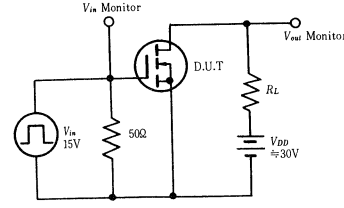
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



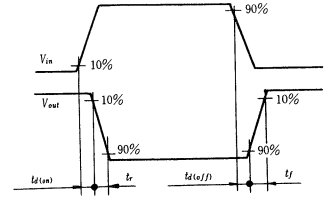
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



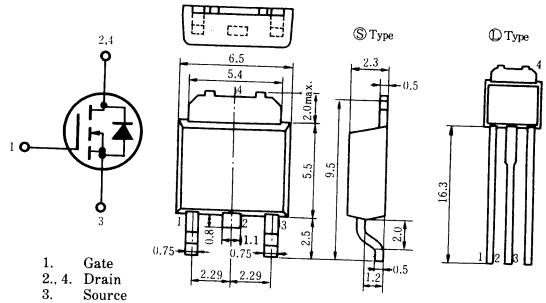
2SK429Ⓛ, 2SK429Ⓢ

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING
HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator and DC-DC Converter.



1. Gate
2., 4. Drain
3. Source

(Dimensions in mm)

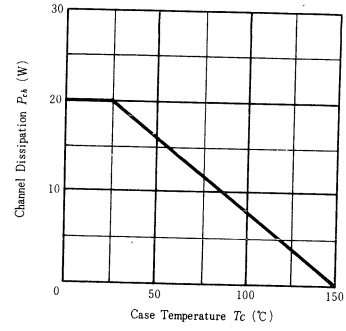
(DPAK)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	3	A
Drain Peak Current	$I_{D(peak)}$	6	A
Body-Drain Diode Reverse Drain Current	I_{DR}	3	A
Channel Dissipation	P_{ch}*	20	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING



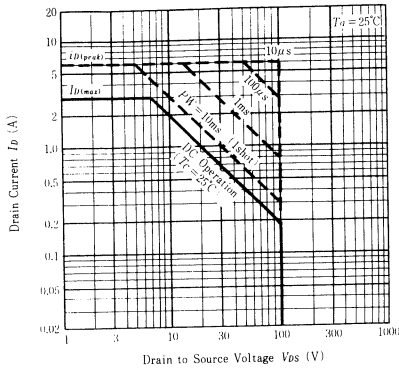
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	100	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	4.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=2A, V_{GS}=15V*	—	0.5	0.7	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=2A, V_{GS}=15V*	—	1.0	1.4	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=2A, V_{DS}=10V*	0.5	0.9	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	280	—	pF
Output Capacitance	C_{oss}		—	150	—	pF
Reverse Transfer Capacitance	C_{rss}		—	24	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V, R_L=15Ω	—	10	—	ns
Rise Time	t_r		—	25	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	30	—	ns
Fall Time	t_f		—	20	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=2A, V_{GS}=0	—	0.8	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=2A, V_{GS}=0, di_F/dt=50A/μs	—	200	—	ns

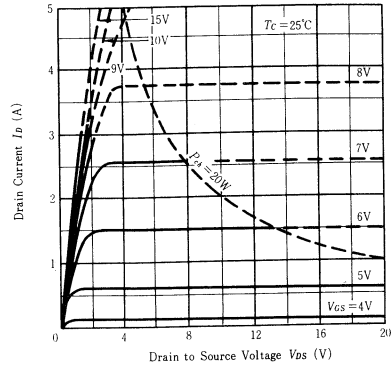
*Pulse Test

HITACHI

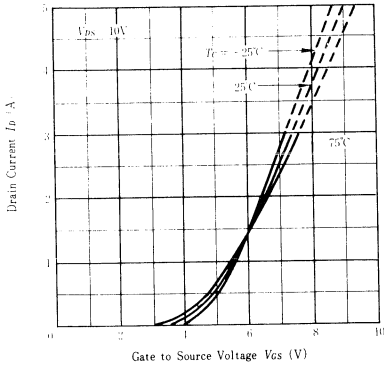
MAXIMUM SAFE OPERATION AREA



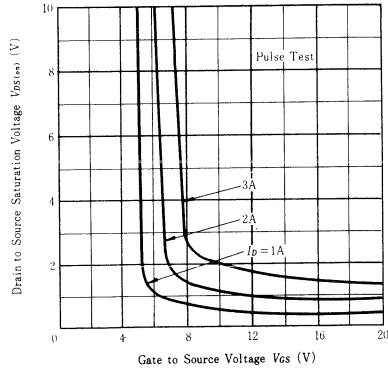
TYPICAL OUTPUT CHARACTERISTICS



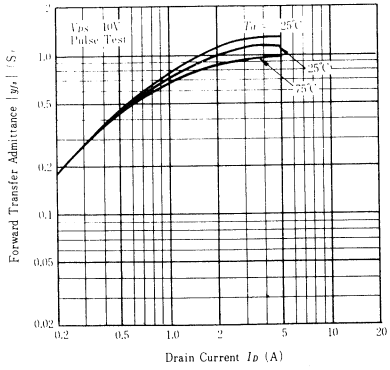
TYPICAL TRANSFER CHARACTERISTICS



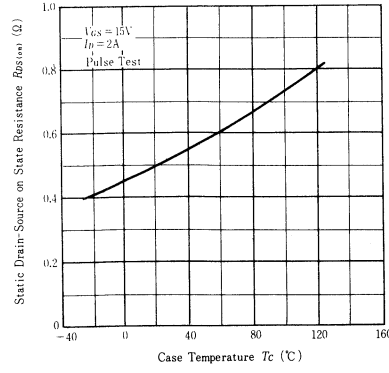
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



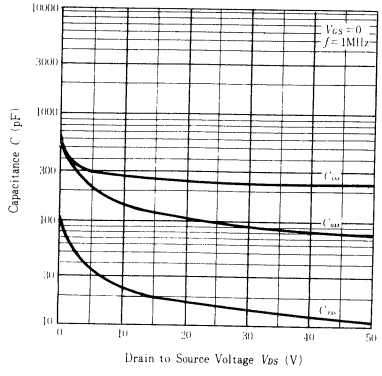
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



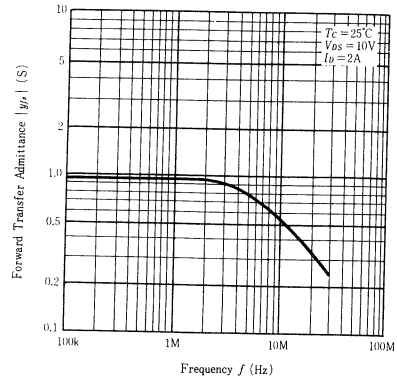
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



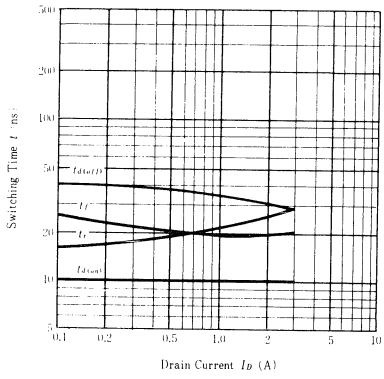
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



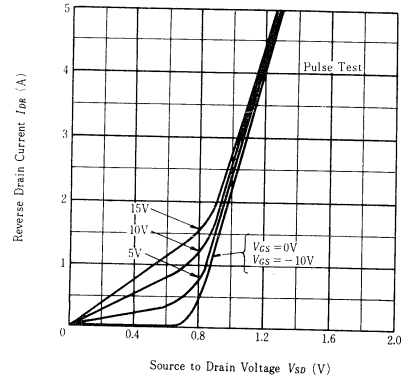
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



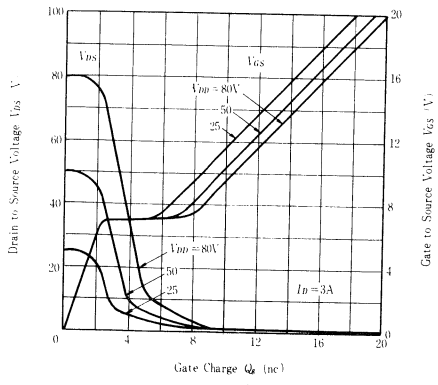
SWITCHING CHARACTERISTICS



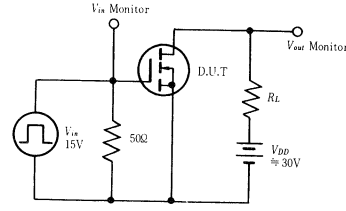
MAXIMUM BODY-DRAIN DIODE



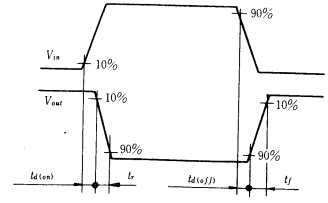
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



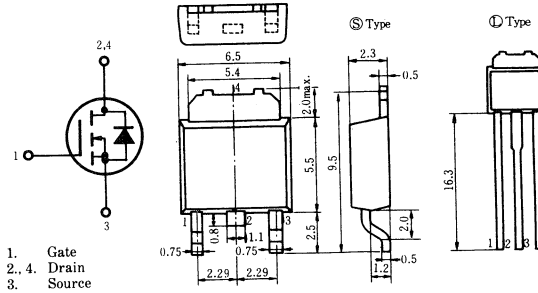
2SK430Ⓛ, 2SK430Ⓢ

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING
HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator and DC-DC Converter.



1. Gate
2., 4. Drain
3. Source

(Dimensions in mm)

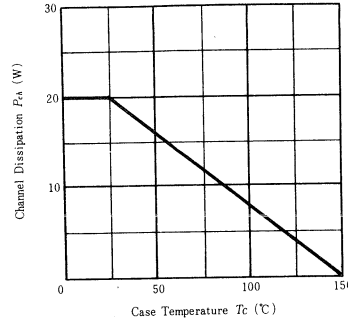
(DPAK)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	150	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	3	A
Drain Peak Current	$I_{D(peak)}$	6	A
Body-Drain Diode Reverse Drain Current	I_{DR}	3	A
Channel Dissipation	P_{ch}*	20	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

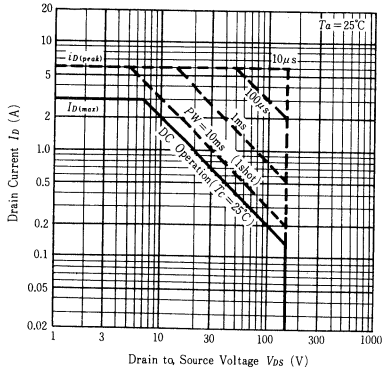


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

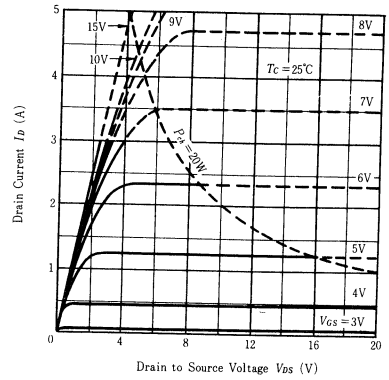
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	150	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=120V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	4.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=2A, V_{GS}=15V*	—	0.8	1.0	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=2A, V_{GS}=15V*	—	1.6	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=2A, V_{DS}=10V*	0.5	0.9	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	260	—	pF
Output Capacitance	C_{oss}		—	100	—	pF
Reverse Transfer Capacitance	C_{rss}		—	14	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V, R_L=15Ω	—	10	—	ns
Rise Time	t_r		—	25	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	30	—	ns
Fall Time	t_f		—	20	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=2A, V_{GS}=0	—	0.8	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=2A, V_{GS}=0, di_F/dt=50A/μs	—	200	—	ns

*Pulse Test

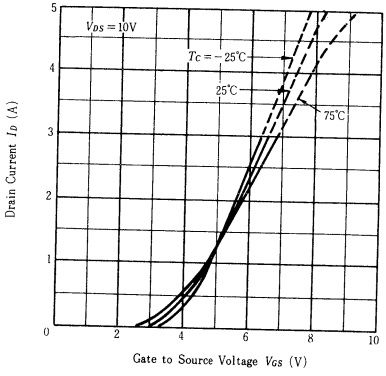
MAXIMUM SAFE OPERATION AREA



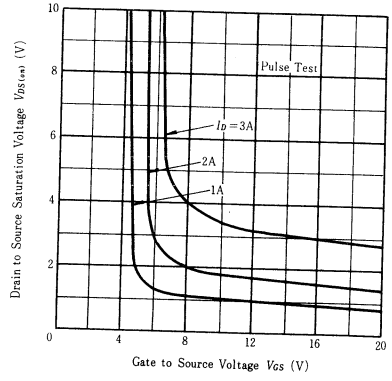
TYPICAL OUTPUT CHARACTERISTICS



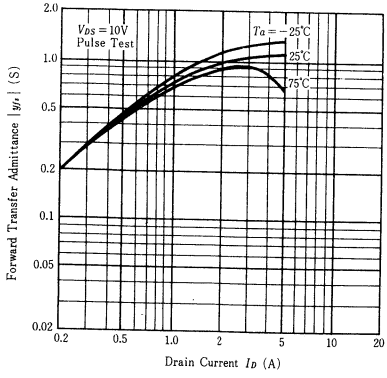
TYPICAL TRANSFER CHARACTERISTICS



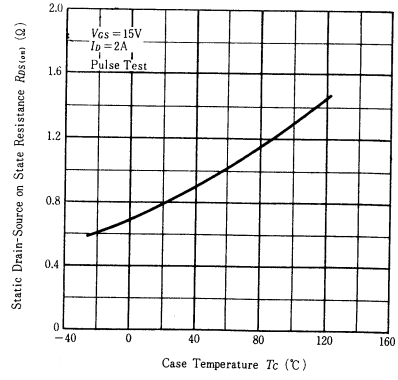
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



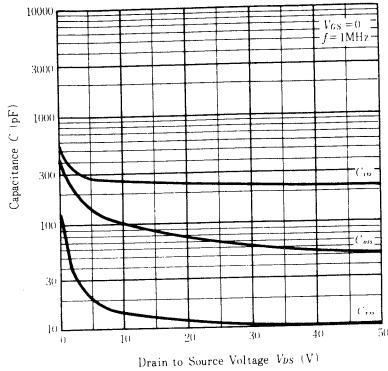
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



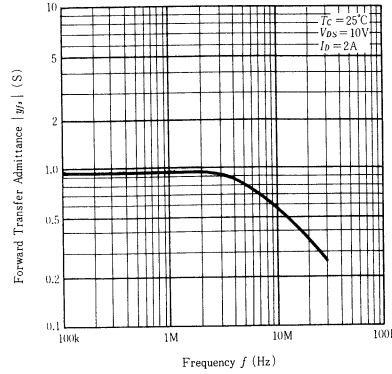
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



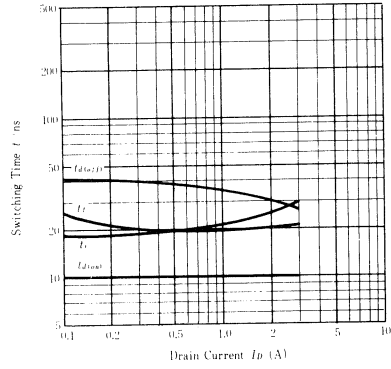
INPUT, OUTPUT CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



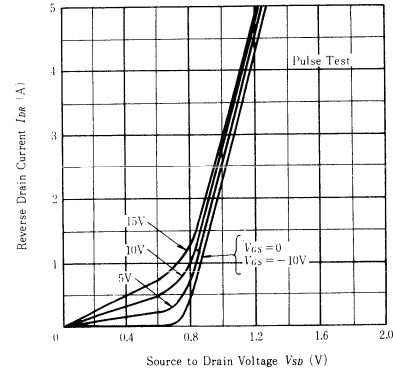
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



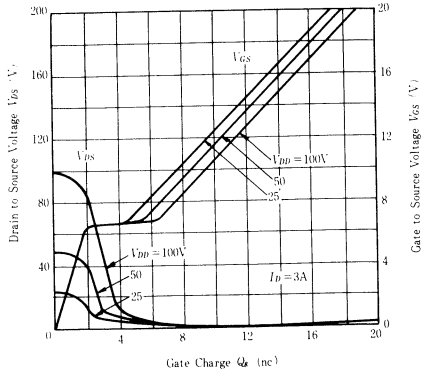
REVERSE TRANSFER CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



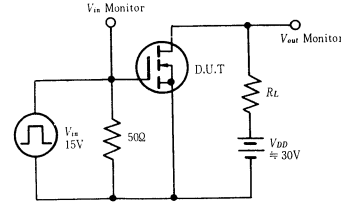
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



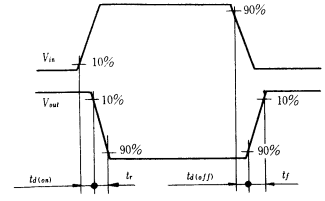
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



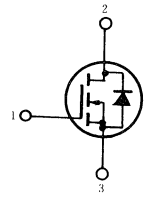
2SK440

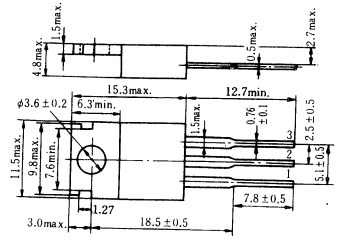
SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING
HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator and DC-DC Converter.





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

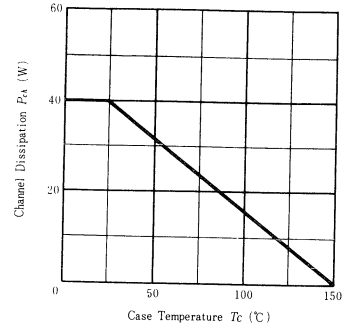
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	200	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	6	A
Drain Peak Current	$I_{D(peak)}$	12	A
Body-Drain Diode Reverse Drain Current	I_{DR}	6	A
Channel Dissipation	P_{ch}*	40	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

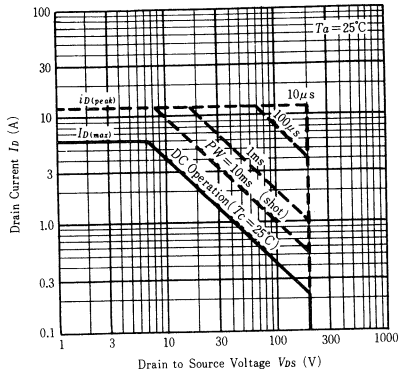


■ ELECTRICAL CHARACTERISTICS (T_a=25°C)

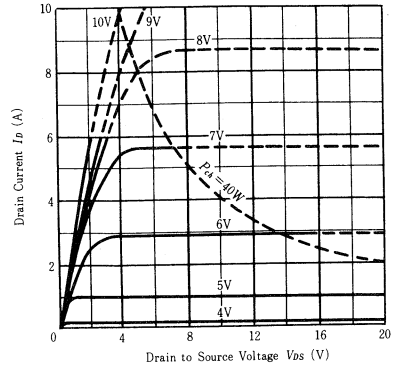
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	200	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=160V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=3A, V_{GS}=15V*	—	0.4	0.5	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=3A, V_{GS}=15V*	—	1.2	1.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	1.0	1.8	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	750	—	pF
Output Capacitance	C_{oss}		—	300	—	pF
Reverse Transfer Capacitance	C_{rss}		—	60	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V, R_L=15Ω	—	15	—	ns
Rise Time	t_r		—	25	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	70	—	ns
Fall Time	t_f		—	40	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=3A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=3A, V_{GS}=0, di_F/dt=50A/μs	—	300	—	ns

*Pulse Test

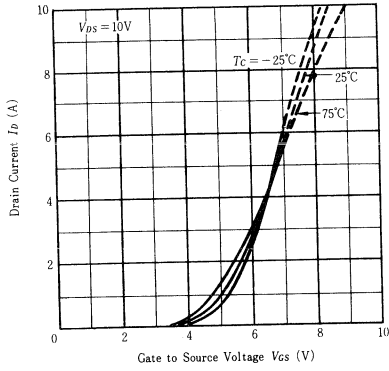
MAXIMUM SAFE OPERATION AREA



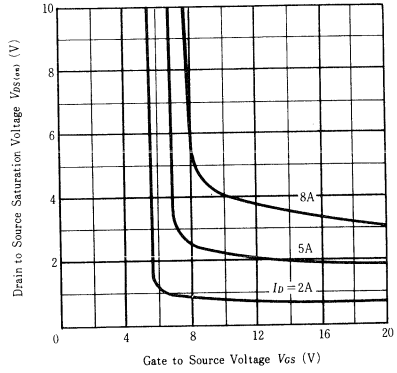
TYPICAL OUTPUT CHARACTERISTICS



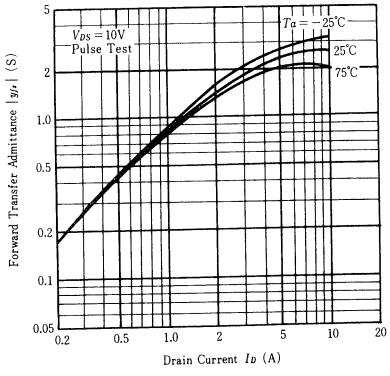
TYPICAL TRANSFER CHARACTERISTICS



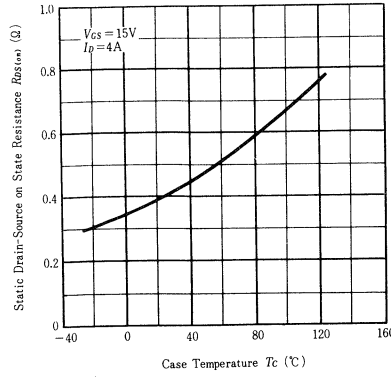
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



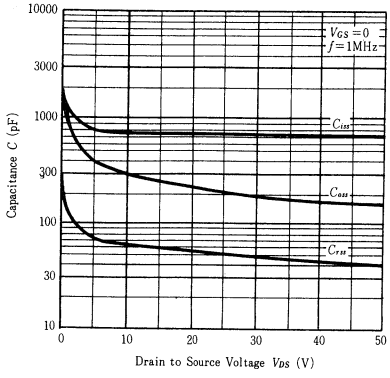
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



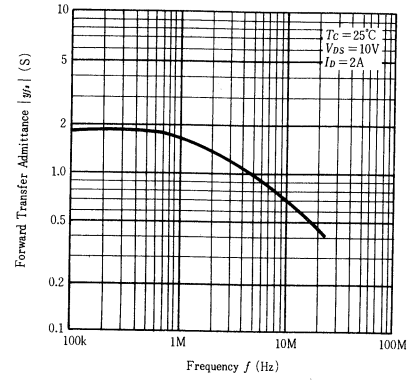
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



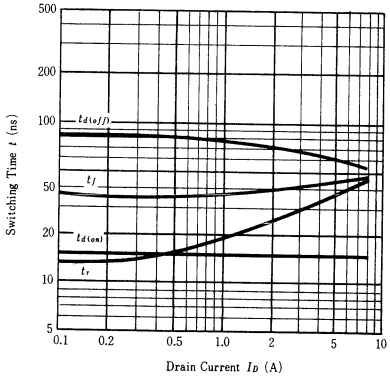
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



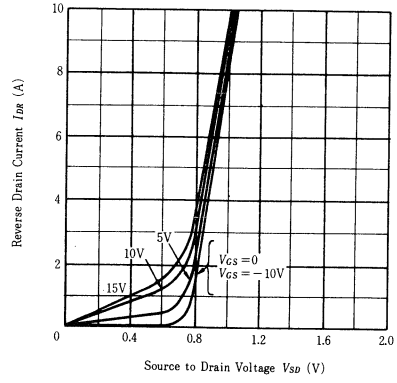
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



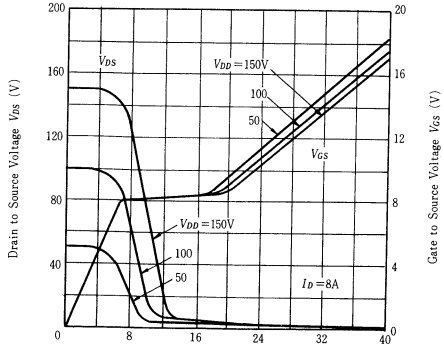
SWITCHING CHARACTERISTICS



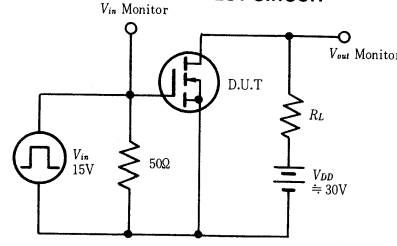
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



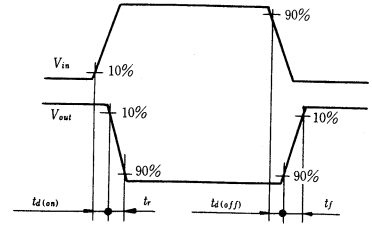
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



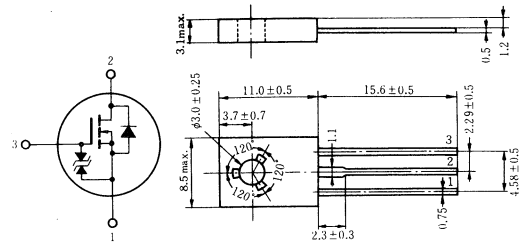
2SK511

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING
HIGH FREQUENCY POWER AMPLIFIER

■ FEATURES

- Superior High Frequency Characteristics.
- Low Input and Output Capacitance.
- Suitable for Video Output Stages of Very High Resolution Display.



1. Source
2. Drain
3. Gate

(Dimensions in mm)

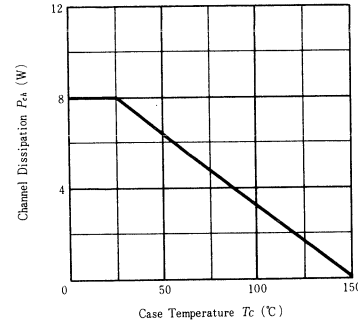
(JEDEC TO-126 MOD.)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	250	V
Gate-Source Voltage	V_{GSS}	±9	V
Drain Current	I_D	0.3	A
Drain Peak Current	$I_{D(peak)}$	0.5	A
Body-Drain Diode Reverse Drain Current	I_{DR}	0.3	A
Channel Dissipation	P_{ch}*	8	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

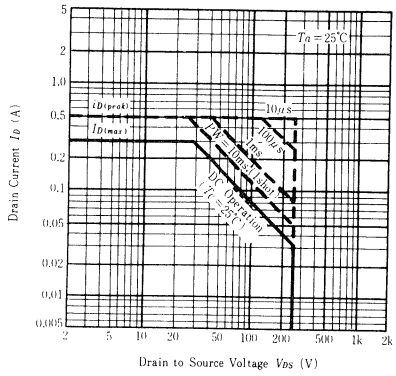


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

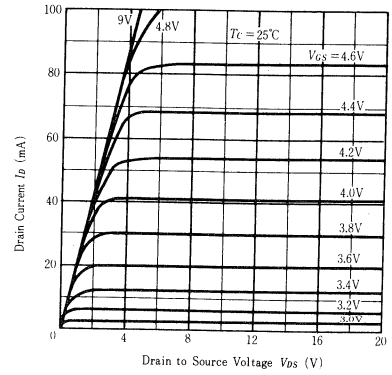
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0	250	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±9V, V_{DS}=0	—	—	±1	mA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=200V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	5.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=0.1A, V_{GS}=9V*	—	30	50	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=0.1A, V_{GS}=9V*	—	3.0	5.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=0.15A, V_{DS}=20V*	50	80	—	mS
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	20	—	pF
Output Capacitance	C_{oss}		—	10	—	pF
Reverse Transfer Capacitance	C_{rss}		—	2.5	—	pF

*Pulse Test

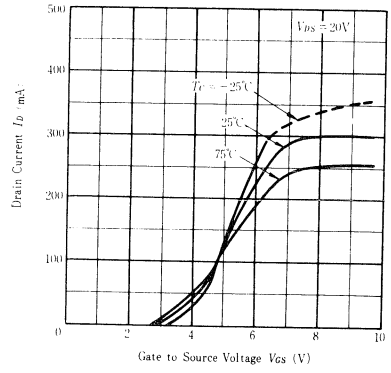
MAXIMUM SAFE OPERATION AREA



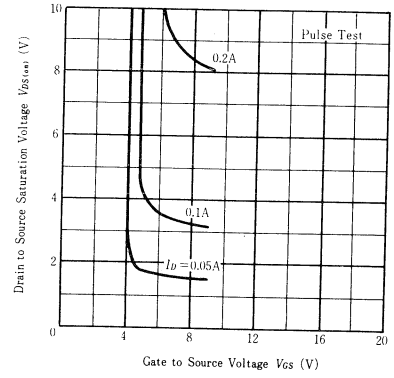
TYPICAL OUTPUT CHARACTERISTICS



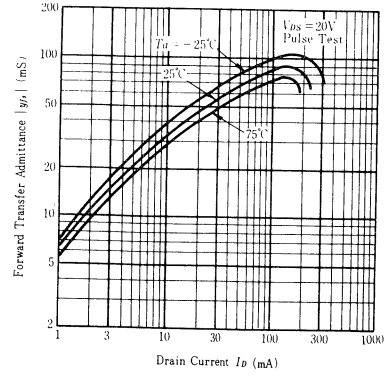
TYPICAL TRANSFER CHARACTERISTICS



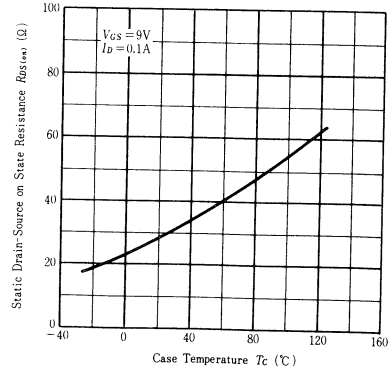
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



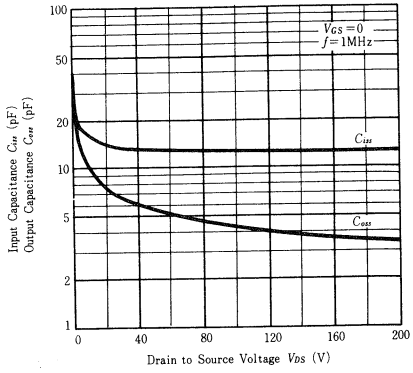
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



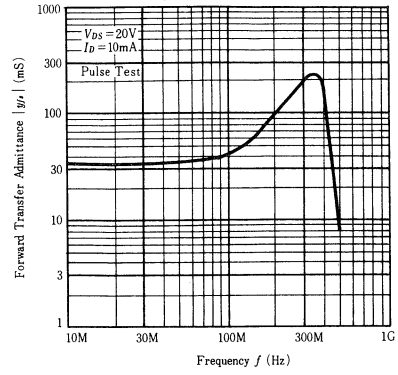
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



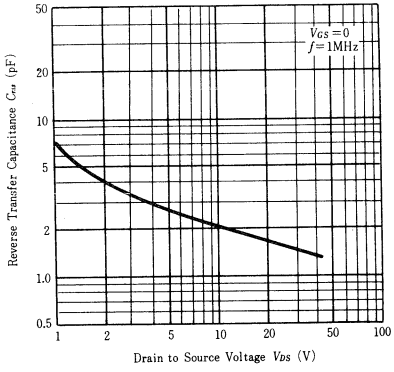
INPUT, OUTPUT CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



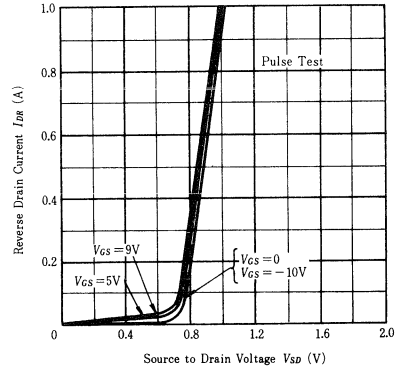
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



REVERSE TRANSFER CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



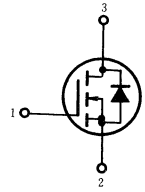
2SK512

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING

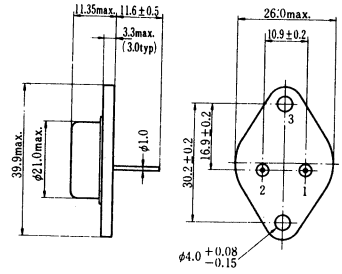
■ FEATURES

- Low On-Resistance. (R_{on}=0.55Ω)
- High Speed Switching.
- High Voltage (V_{DSS}=500V)
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, and Motor Control.



1. Gate
2. Source
3. Drain (Case)

(Dimensions in mm)



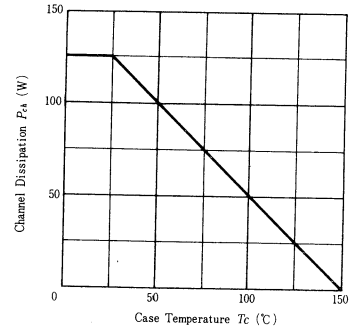
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	500	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	12	A
Drain Peak Current	$I_{D(peak)}$	20	A
Body-Drain Diode Reverse Drain Current	I_{DR}	12	A
Channel Dissipation	P_{ch}*	125	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



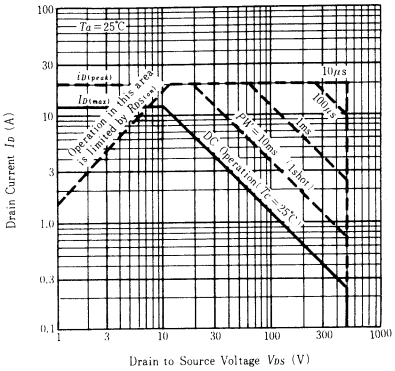
■ ELECTRICAL CHARACTERISTICS (T_a=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	500	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=400V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	4.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=6A, V_{GS}=15V*	—	0.55	0.65	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=6A, V_{GS}=15V*	—	3.3	3.9	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=6A, V_{DS}=10V*	2.5	3.5	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	1800	—	pF
Output Capacitance	C_{oss}		—	400	—	pF
Reverse Transfer Capacitance	C_{rss}		—	50	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V, R_L=15Ω	—	20	—	ns
Rise Time	t_r		—	45	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	230	—	ns
Fall Time	t_f		—	70	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=6A, V_{GS}=0	—	1.0	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=6A, V_{GS}=0, di_F/dt=100A/μs	—	400	—	ns

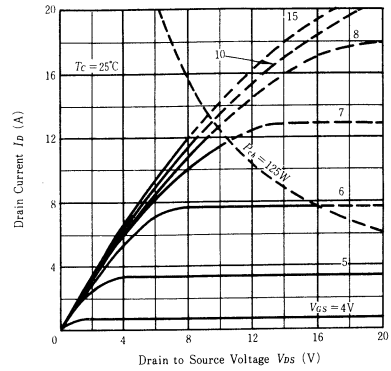
*Pulse Test

HITACHI

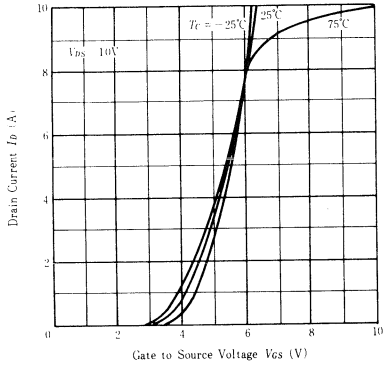
MAXIMUM SAFE OPERATION AREA



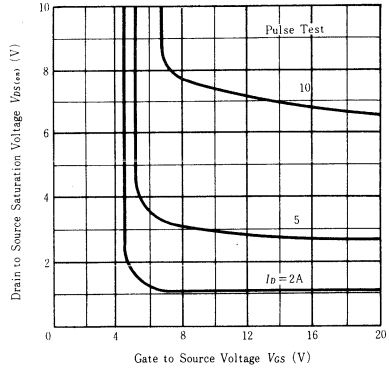
TYPICAL OUTPUT CHARACTERISTICS



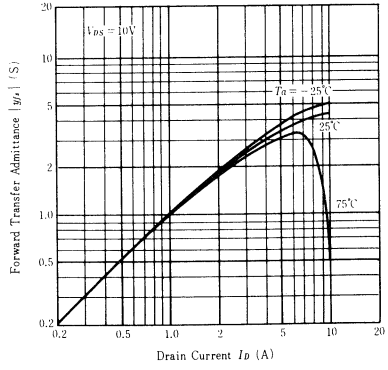
TYPICAL TRANSFER CHARACTERISTICS



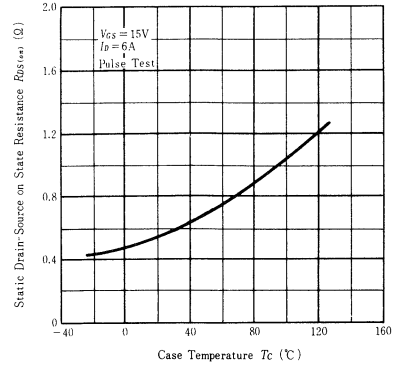
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



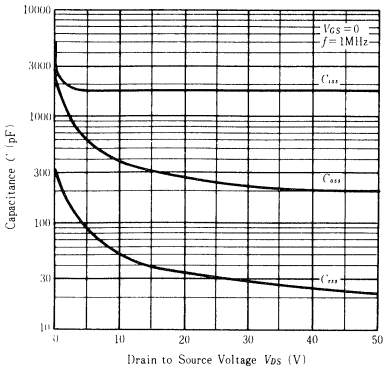
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



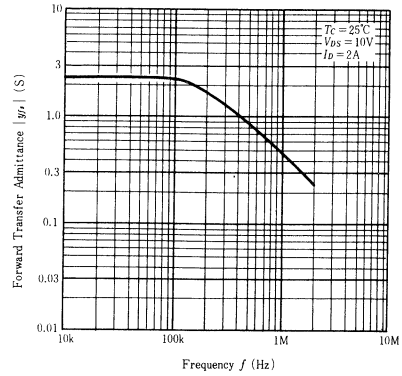
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



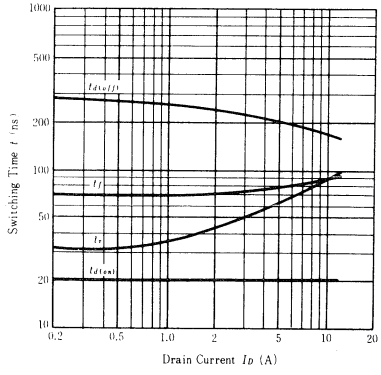
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



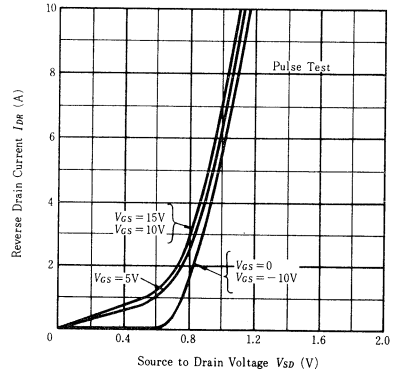
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



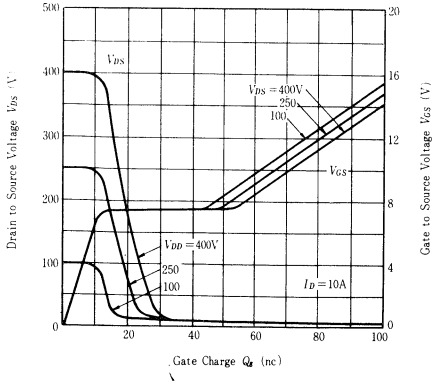
SWITCHING CHARACTERISTICS



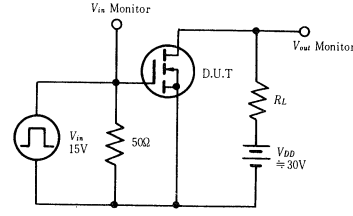
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



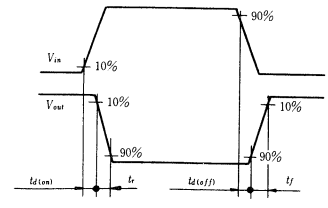
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



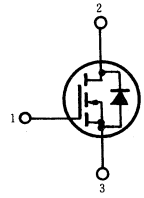
2SK513

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING

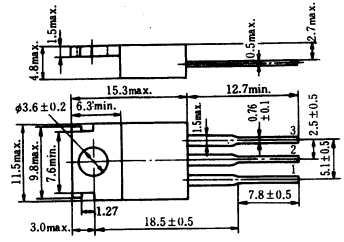
■ FEATURES

- High Breakdown Voltage.
- High Speed Switching.
- High Cutoff Frequency.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)



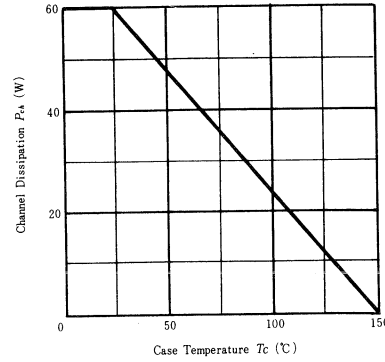
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	800	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	3	A
Drain Peak Current	$I_{D(peak)}$	6	A
Body-Drain Diode Reverse Drain Current	I_{DR}	3	A
Channel Dissipation	P_{ch}*	60	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

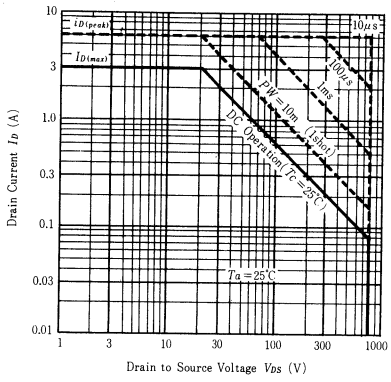


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

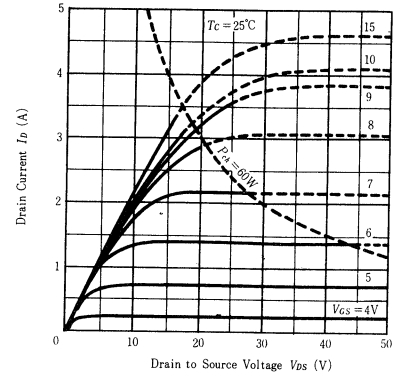
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	800	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=640V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	4.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=2A, V_{GS}=15V*	—	5.0	6.0	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=2A, V_{GS}=15V*	—	10.0	12.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=2A, V_{DS}=20V*	0.4	0.7	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	470	—	pF
Output Capacitance	C_{oss}		—	120	—	pF
Reverse Transfer Capacitance	C_{rss}		—	22	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V, R_L=15Ω	—	15	—	ns
Rise Time	t_r		—	35	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	85	—	ns
Fall Time	t_f		—	35	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=2A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=2A, V_{GS}=0, di_F/dt=100A/μs	—	700	—	ns

*Pulse Test

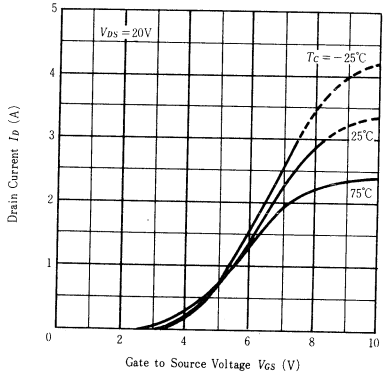
MAXIMUM SAFE OPERATION AREA



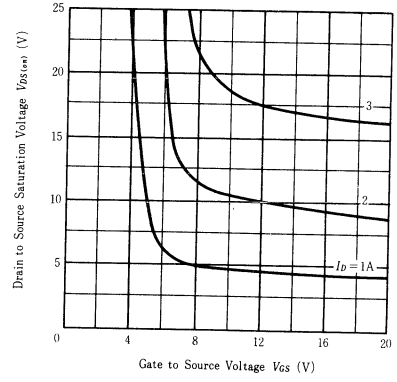
TYPICAL OUTPUT CHARACTERISTICS



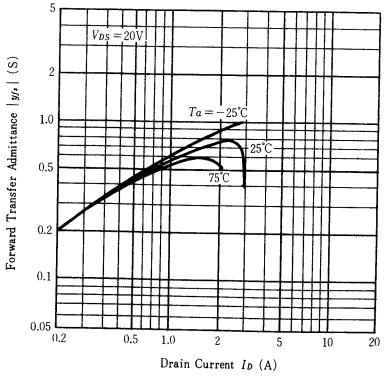
TYPICAL TRANSFER CHARACTERISTICS



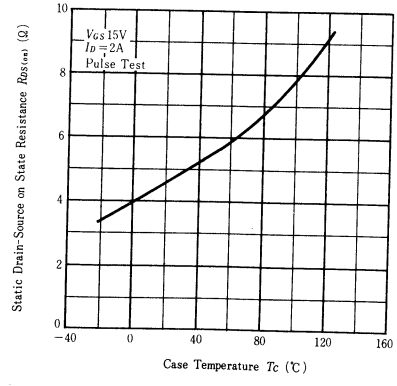
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



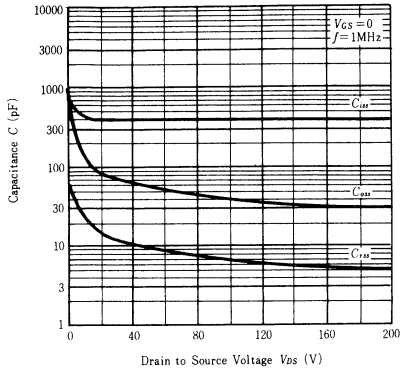
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



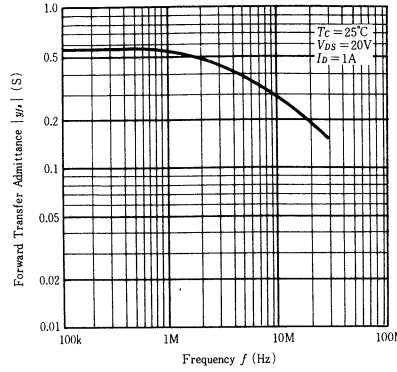
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



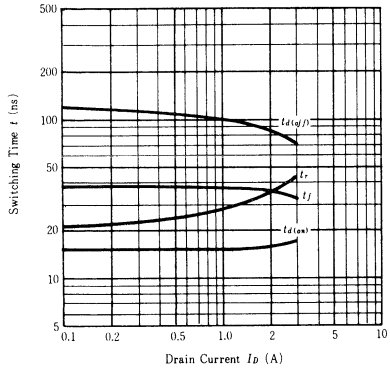
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



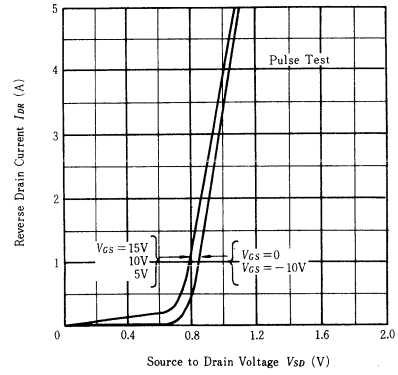
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



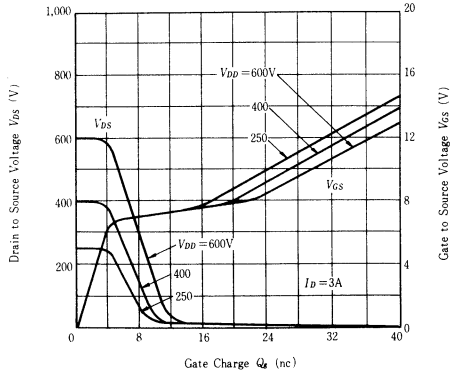
SWITCHING CHARACTERISTICS



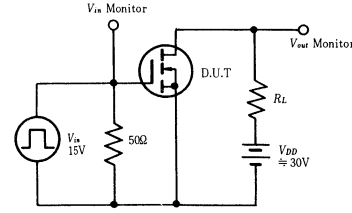
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



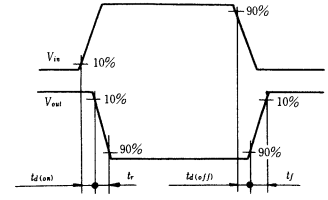
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



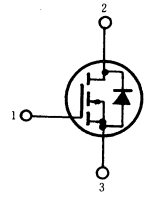
2SK534

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING

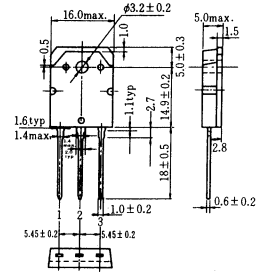
■ FEATURES

- High Speed Switching. (t_f=65ns)
- High Voltage (V_{DSS}=800V)
- No Secondary Breakdown.
- Suitable for Switching Regulator and DC-DC Converter.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)



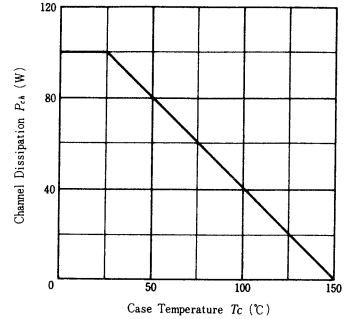
(TO-3P)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	800	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	5	A
Drain Peak Current	$I_{D(peak)}$	10	A
Body-Drain Diode Reverse Drain Current	I_{DR}	5	A
Channel Dissipation	P_{ch}*	100	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



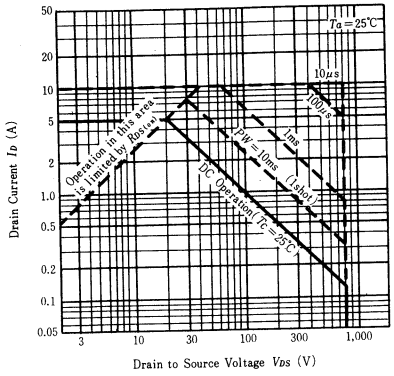
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	800	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	—	—	±1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=640V, V_{GS}=0	—	—	1	mA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	4.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=3A, V_{GS}=10V*	—	3	4	Ω
Drain-Source Saturation Voltage	$V_{DS(on)}$	I_D=3A, V_{GS}=10V*	—	9	12	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=3A, V_{DS}=20V*	0.8	1.2	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	850	—	pF
Output Capacitance	C_{oss}		—	250	—	pF
Reverse Transfer Capacitance	C_{rss}		—	40	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=15V R_L=15Ω	—	15	—	ns
Rise Time	t_r		—	60	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	155	—	ns
Fall Time	t_f		—	65	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=3A, V_{GS}=0	—	0.9	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=3A, V_{GS}=0 di_F/dt=100A/μs	—	850	—	ns

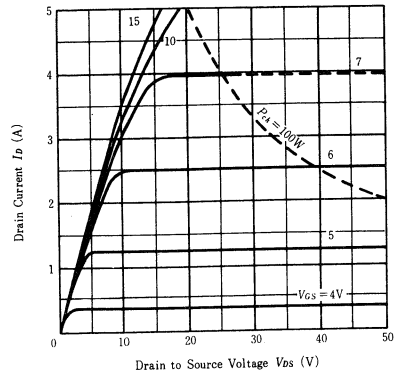
*Pulse Test

HITACHI

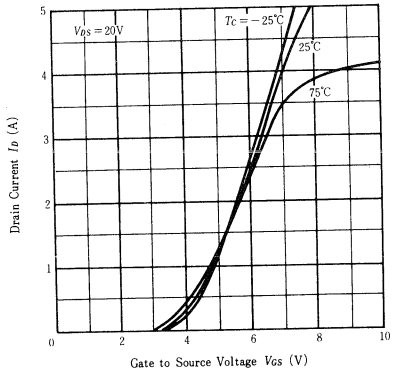
MAXIMUM SAFE OPERATION AREA



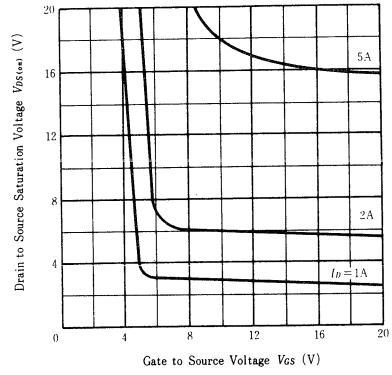
TYPICAL OUTPUT CHARACTERISTICS



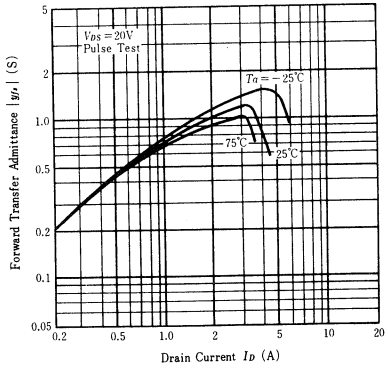
TYPICAL TRANSFER CHARACTERISTICS



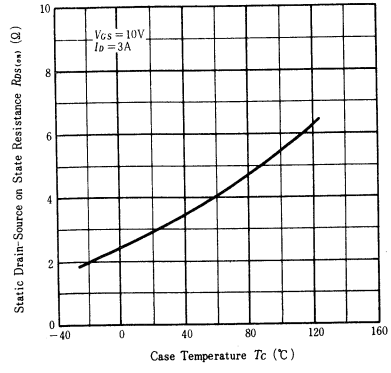
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



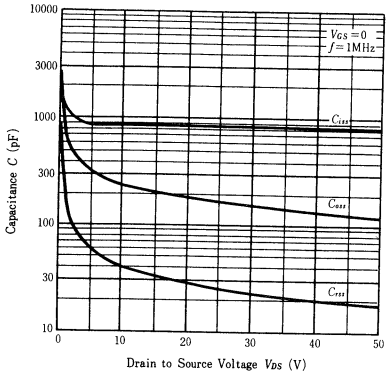
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



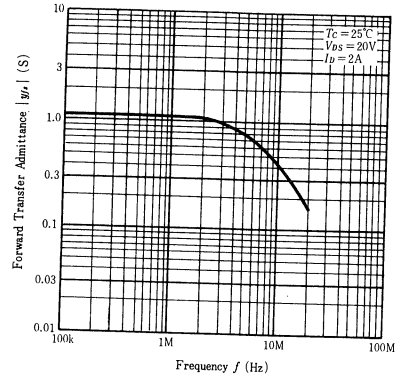
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



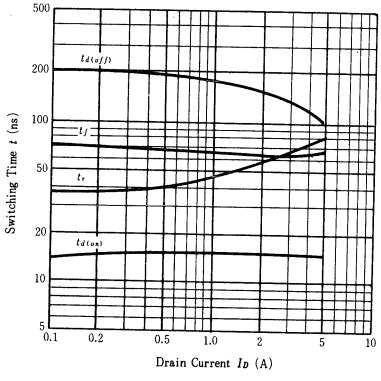
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



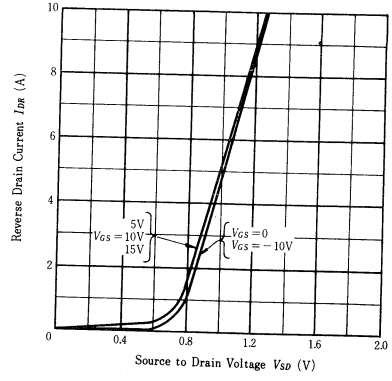
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



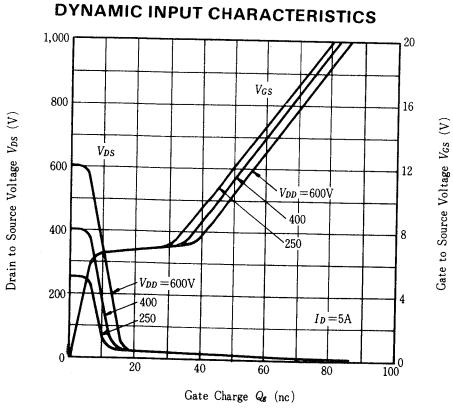
SWITCHING CHARACTERISTICS



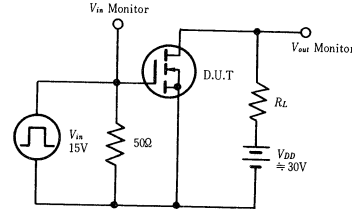
MAXIMUM BODY-DRAIN DIODE FORWARD VOLTAGE



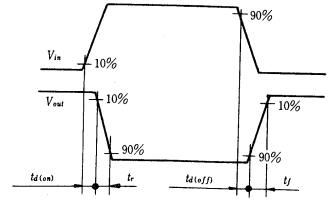
DYNAMIC INPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



Super High Resolution CRT
Video Amplifier Output

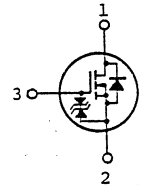
2SK619

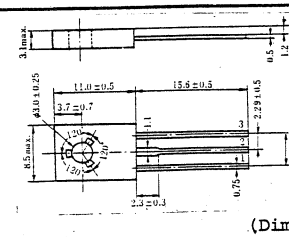
SILICON N-CHANNEL ENHANCEMENT MOS FET

HIGH FREQUENCY HIGH IMPEDANCE AMPLIFIER

Features

1. High Voltage. (V_{DSS}=70V)
2. Effective to suppress signal radiation.
   Connected source to heatsink.
3. High Gain Low capacitance.
4. Bultin protective diode gate to source.





1. Drain
2. Source
3. Gate

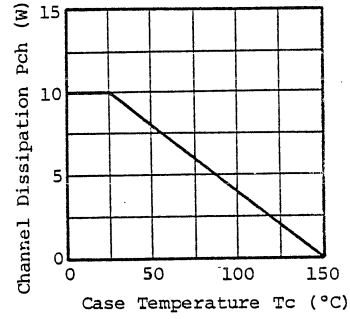
(JEDEC TO-126 MOD.) (Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	70	V
Gate to Source Voltage	V_{GSS}	$^{+9}_{-6}$	V
Drain Current	I_D	0.3	A
Drain Peak Current	$i_{D(peak)}$	0.5	A
Channel Dissipation	P_{ch}	1.0	W
Channel Dissipation	P_{ch}*	10	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 ~ +150	°C

*Value at Tc=25°C

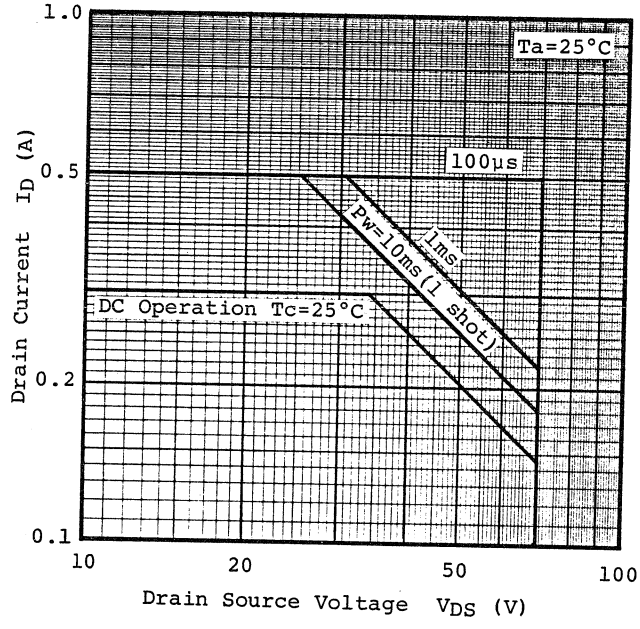
MAXIMUM COLLECTOR DISSIPATION CURVE



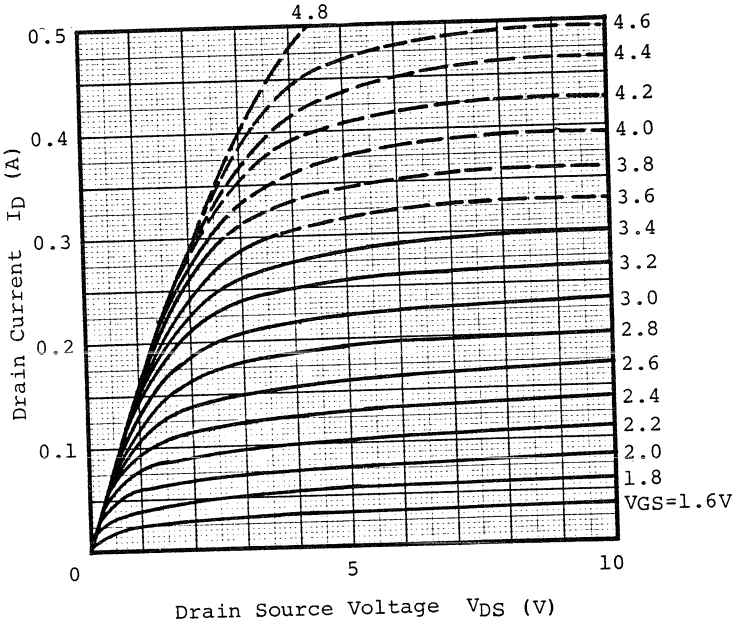
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA , V_{GS}=0	70	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±1mA , V_{DS}=0	$^{+9}_{-6}$	-	-	V
Drain Cutoff Current	I_{DSS}	V_{DS}=50V , V_{GS}=0	-	-	1	mA
Gate Soff Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=20V	0.3	-	1.8	V
Drain to Source on Voltage	$V_{DS(on)}$	I_D=0.1A , V_{GS}=9V	-	-	5.0	V
Forward Transfer Ratio	$\|yfs\|$	I_D=0.2A , V_{DS}=10V	90	130	-	ms
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	10	-	pF
Output Capacitance	Coss		-	6	10	pF

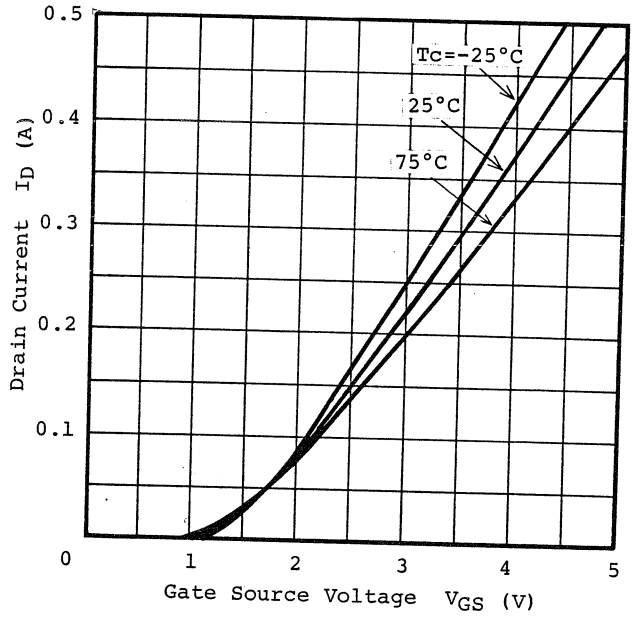
MAXIMUM SAFE OPERATION AREA



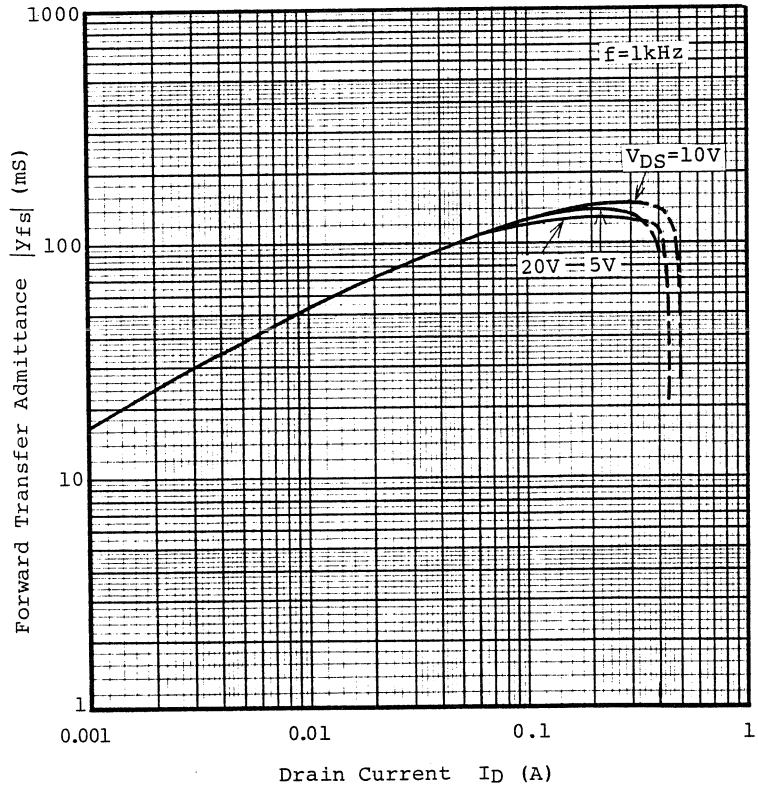
TYPICAL OUTPUT CHARACTERISTICS



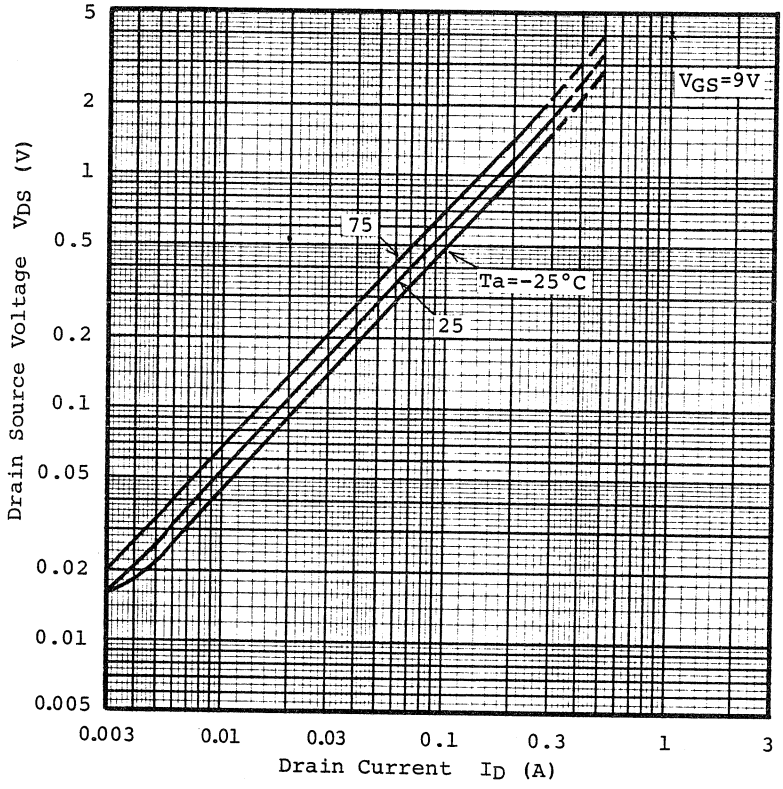
TYPICAL TRANSFER CHARACTERISTICS



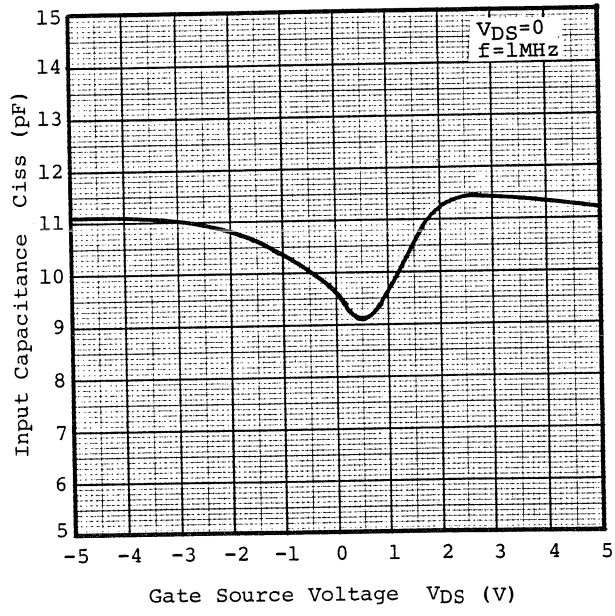
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



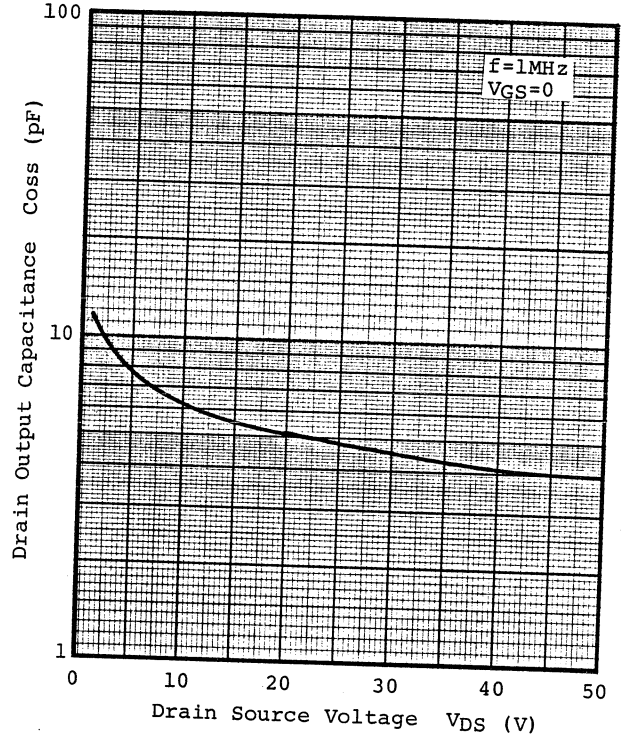
DRAIN SOURCE VOLTAGE VS. DRAIN CURRENT



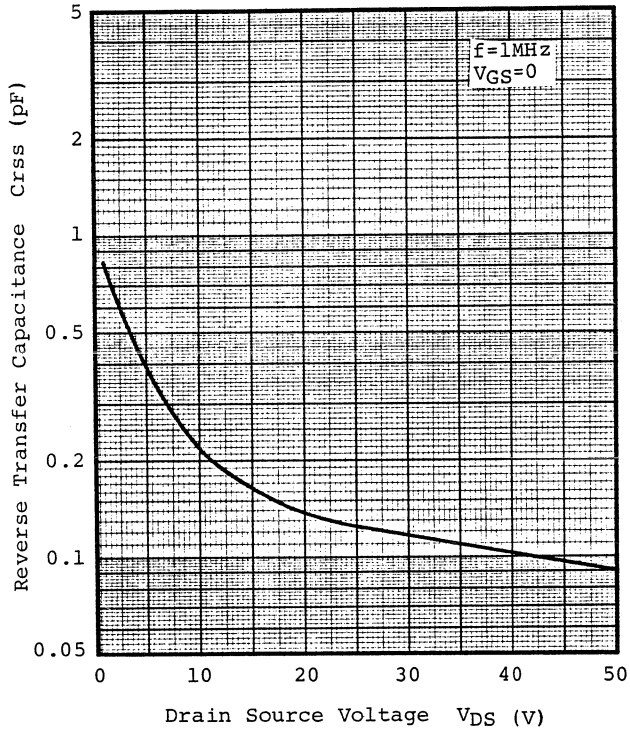
INPUT CAPACITANCE VS. GATE SOURCE VOLTAGE



DRAIN OUTPUT CAPACITANCE VS.
DRAIN SOURCE VOLTAGE



REVERSE TRANSFER CAPACITANCE VS.
DRAIN SOURCE VOLTAGE



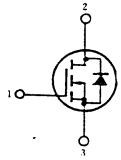
2SK646

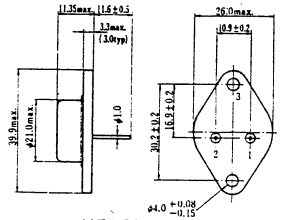
—Preliminary—

SILICON Nch TRIPLE DIFFUSED
HIGH SPEED POWER SWITCHING
HIGH SPEED SCANNING HORIZONTAL DEFLECTION OUTPUT

Features

1. High Voltage. V_{DSS}=1200V
2. High Speed. Enable to Operate High Speed Horizontal Deflection Output. (f_H=130KHz)
3. Wide Safe Operating Area.





(JEDEC TO-3)

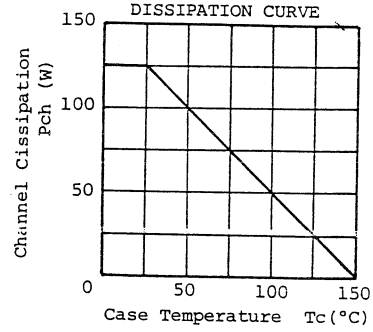
1. Gate
2. Source
3. Drain

■ ABSOLUTE MAXIMUM RATINGS. (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	1200	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	4	A
Drain Peak Current	$I_{D(peak)}$	8	A
Channel Dissipation	Pch*	125	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55~+150	°C

* Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATION CURVE



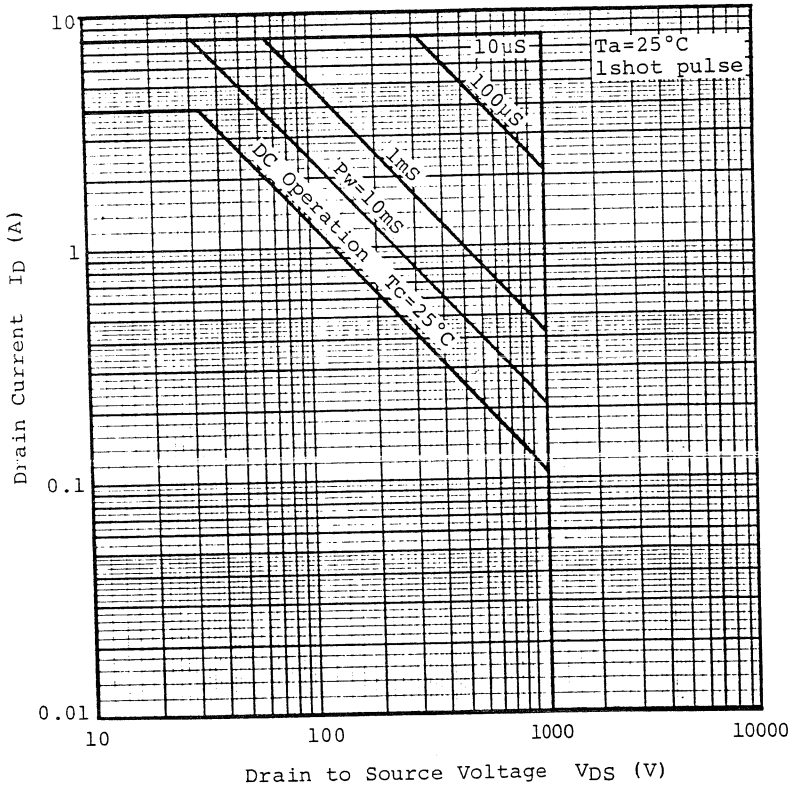
■ ELECTRICAL CHARACTERISTICS.

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	1200	-	-	V
Gate Cutoff Current	I_{GSS}	V_{GS}=±20V , V_{DS}=0	-	-	±1.0	μA
Drain Cutoff Current	I_{DSS}	V_{DS}=960V , V_{GS}=0	-	-	1.0	mA
Gate to Source Voltage	$V_{GS(off)}$	V_{DS}=10V , I_D=1mA	1.0	-	5.0	V
Forward Transfer Admittance	Y_{fs}	V_{DS}=20V , I_D=2A	0.7	1.3	-	S
Drain to Source on Resistance	$R_{DS(on)}$	I_D=2A , V_{GS}=15V	-	6.0	8.0	Ω
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	2000	-	pF
Output Capacitance	Coss		-	400	-	pF
Reverse Transfer Capacitance	Crss		-	1300	-	pF
Turn-on Time	ton	I_D=2A , V_{GS}=15V	-	80	-	ns
Turn-off Time	toff	R_L=15Ω , R_G=50Ω	-	350	-	ns

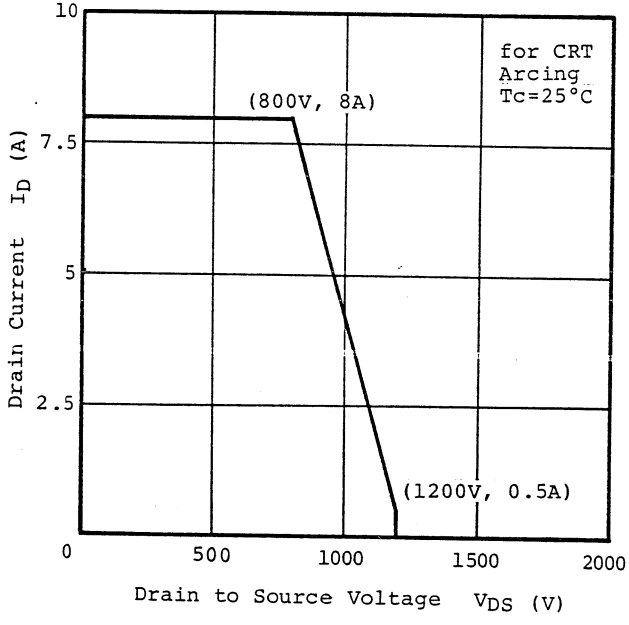
Product Preview : This document contains information on a product under development. Hitachi reserves the right to change or discontinue the product without notice.

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

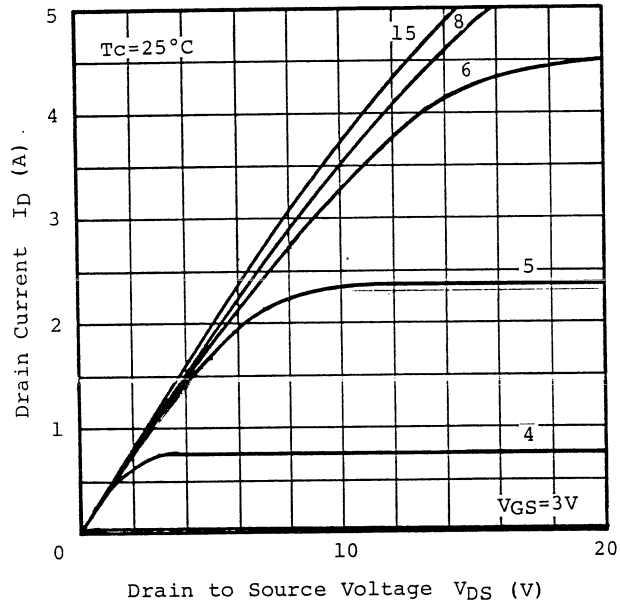
AREA OF SAFE OPERATION



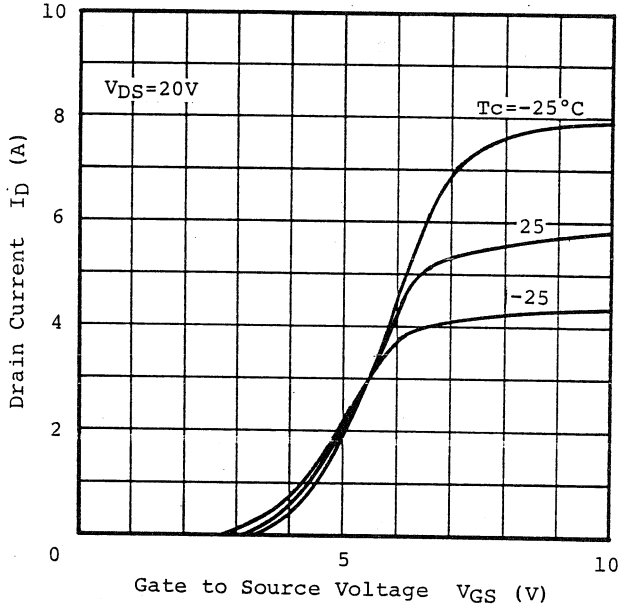
AREA OF SAFE OPERATION



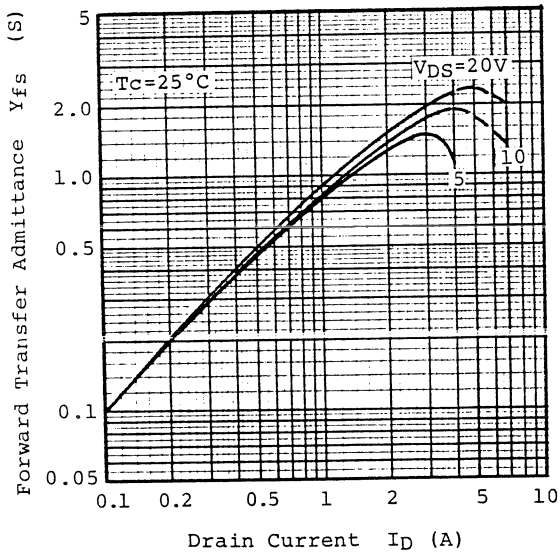
TYPICAL OUTPUT CHARACTERISTICS



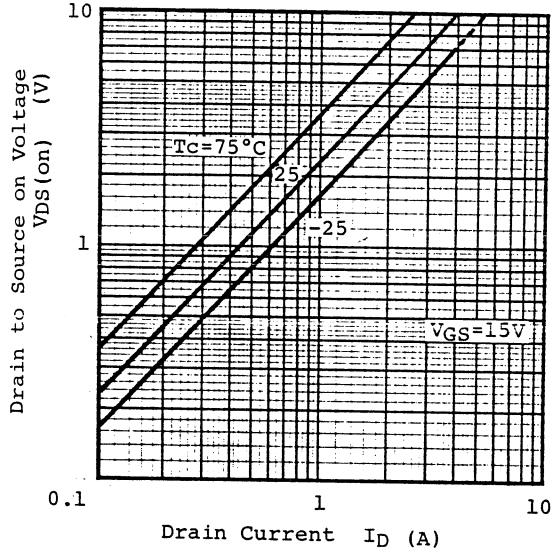
TYPICAL TRANSFER CHARACTERISTICS



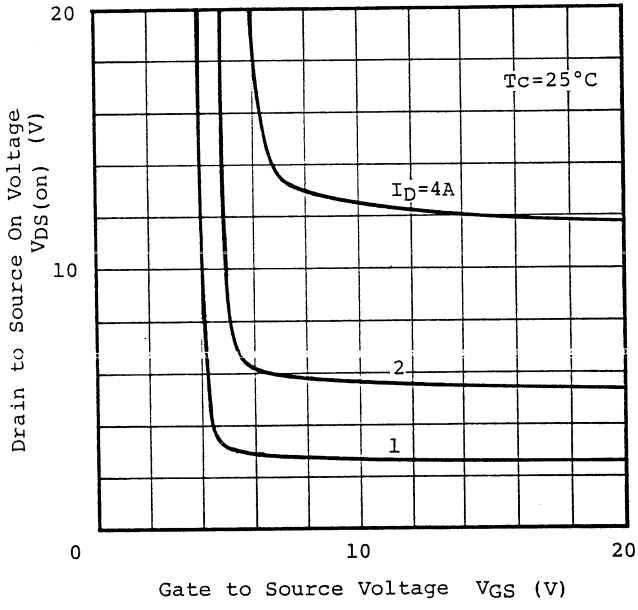
FORWARD TRANSFER ADMITTANCE VS.
DRAIN CURRENT



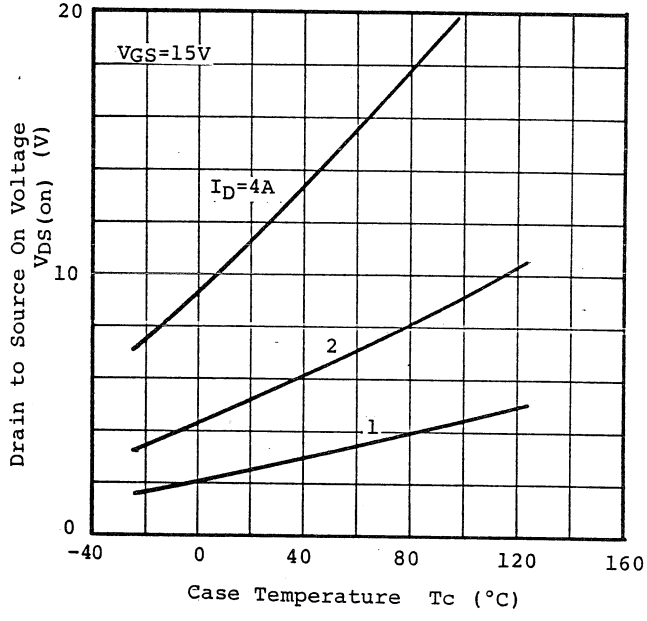
DRAIN TO SOURCE ON VOLTAGE VS.
DRAIN CURRENT



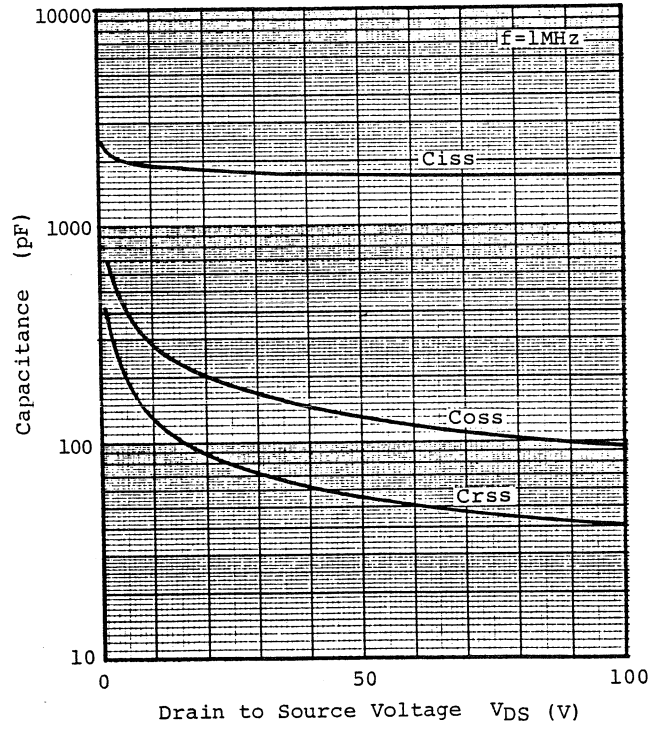
DRAIN TO SOURCE ON VOLTAGE VS.
GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON VOLTAGE VS.
CASE TEMPERATURE



CAPACITANCE DRAIN TO SOURCE VOLTAGE



2SK1056, 2SK1057, 2SK1058

SILICON N-CHANNEL MOS FET

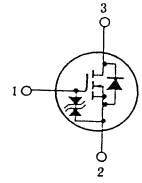
—Preliminary—

LOW FREQUENCY POWER AMPLIFIER

Complementary pair with 2SJ160, 2SJ161, 2SJ162

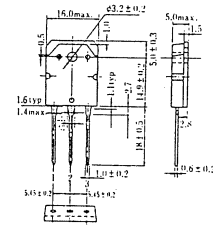
■ FEATURES

- High Power Gain.
- Excellent Frequency Response.
- High Speed Switching.
- Wide Area of Safe Operation.
- Enhancement-Mode.
- Good Complementary Characteristics.
- Equipped with Gate Protection Diodes.



1. Gate
2. Source (Flange)
3. Drain

(Dimensions in mm)



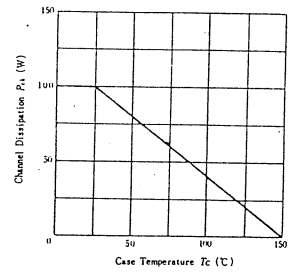
(TO-3P)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Rating			Unit
		2SK1056	2SK1057	2SK1058	
Drain-Source Voltage	V_{DSX}	120	140	160	V
Gate-Source Voltage	V_{GSS}	±15			V
Drain Current	I_D	7			A
Body-Drain Diode Reverse Drain Current	I_{DR}	7			A
Channel Dissipation	P_{ch}*	100			W
Channel Temperature	T_{ch}	150			°C
Storage Temperature	T_{stg}	−55 ~ +150			°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

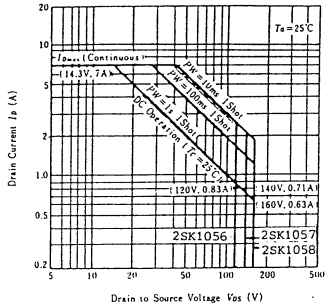
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK1056	$V_{(BR)DSX}$	I_D=10mA, V_{GS}=−10V	120	—	—	V
	2SK1057			140	—	—	V
	2SK1058			160	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	—	—	V
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=100mA, V_{DS}=10V	0.15	—	1.45	V
Drain-Source Saturation Voltage		$V_{DS(sat)}$	I_D=7A, V_{GD}=0*	—	—	12	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	0.7	1.0	1.4	S
Input Capacitance		C_{iss}	V_{GS}=−5V, V_{DS}=10V, f=1MHz	—	600	—	pF
Output Capacitance		C_{oss}		—	350	—	pF
Reverse Transfer Capacitance		C_{rss}		—	10	—	pF
Turn-on Time		t_{on}	V_{DD}=20V, I_D=4A	—	180	—	ns
Turn-off Time		t_{off}		—	60	—	ns

*Pulse Test

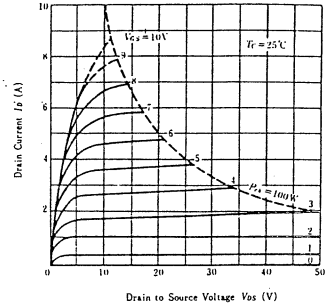
Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

HITACHI

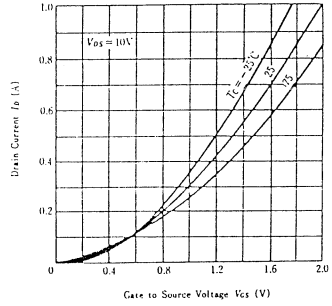
MAXIMUM SAFE OPERATION AREA



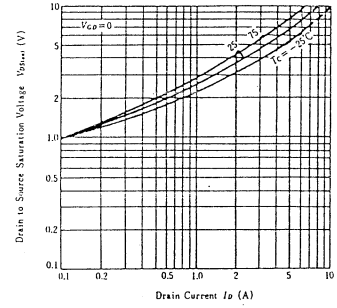
TYPICAL OUTPUT CHARACTERISTICS



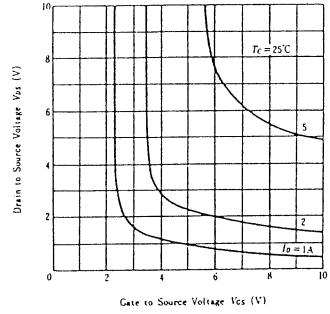
TYPICAL TRANSFER CHARACTERISTICS



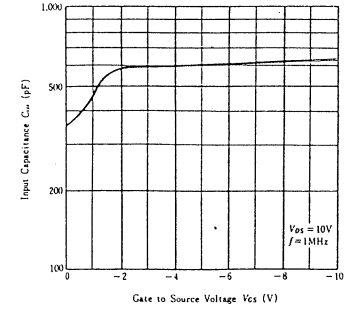
DRAIN - SOURCE SATURATION VOLTAGE VS. DRAIN CURRENT



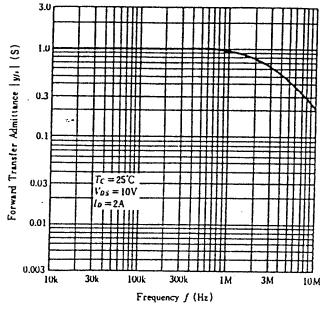
DRAIN - SOURCE VOLTAGE VS. GATE - SOURCE VOLTAGE



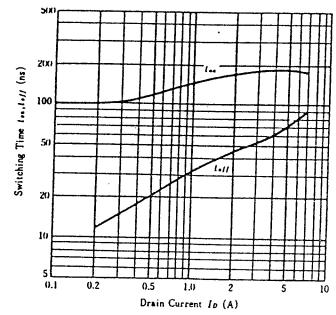
INPUT CAPACITANCE VS. GATE - SOURCE VOLTAGE



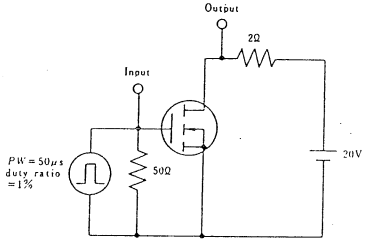
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



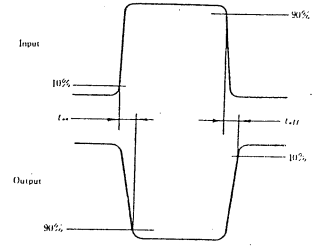
SWITCHING TIME VS. DRAIN CURRENT



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



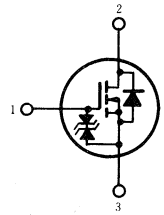
2SK549

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING

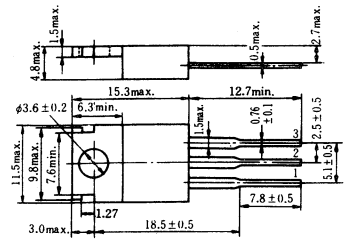
■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)



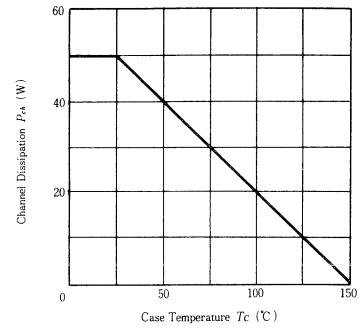
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±15	V
Drain Current	I_D	10	A
Drain Peak Current	$I_{D(pulse)}$*	40	A
Body-Drain Diode Reverse Drain Current	I_{DR}	10	A
Channel Dissipation	P_{ch}**	50	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*PW≤10μs, duty cycle≤1%
**Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

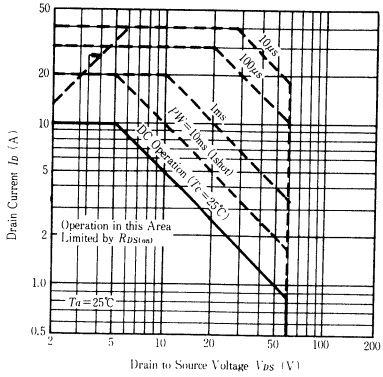


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

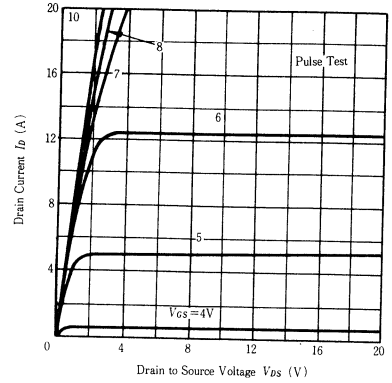
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	60	—	—	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±12V, V_{DS}=0	—	—	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V, V_{GS}=0	—	—	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	4.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	I_D=5A, V_{GS}=10V*	—	0.1	0.15	Ω
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=5A, V_{DS}=10V*	3.0	5.0	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	700	—	pF
Output Capacitance	C_{oss}		—	400	—	pF
Reverse Transfer Capacitance	C_{rss}		—	28	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=5A, V_{GS}=10V R_L=6Ω	—	15	—	ns
Rise Time	t_r		—	40	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	55	—	ns
Fall Time	t_f		—	45	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=10A, V_{GS}=0	—	1.2	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=10A, V_{GS}=0 di_F/dt=50A/μs	—	200	—	ns

*Pulse Test

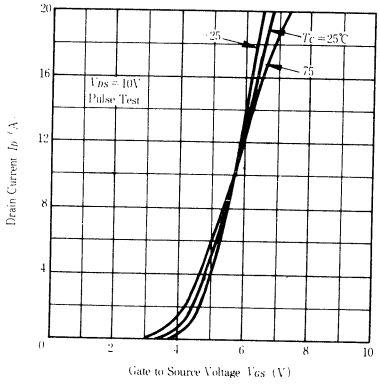
MAXIMUM SAFE OPERATION AREA



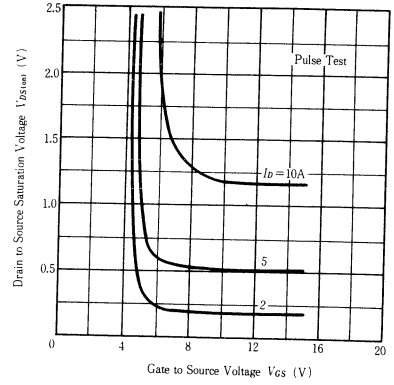
TYPICAL OUTPUT CHARACTERISTICS



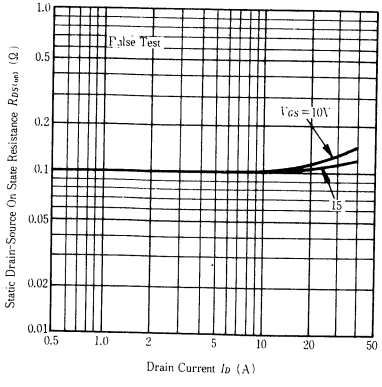
TYPICAL TRANSFER CHARACTERISTICS



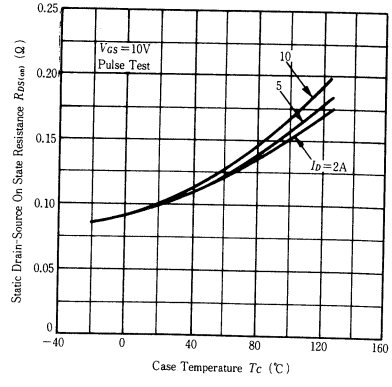
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



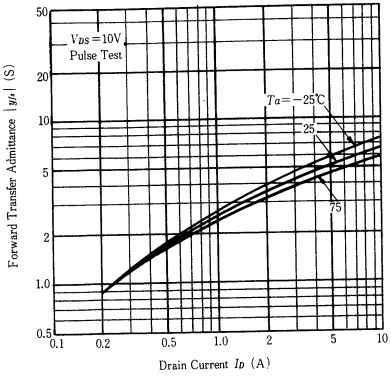
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



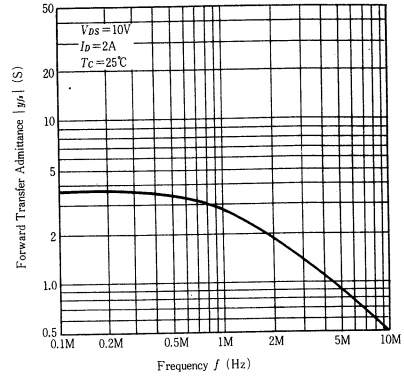
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



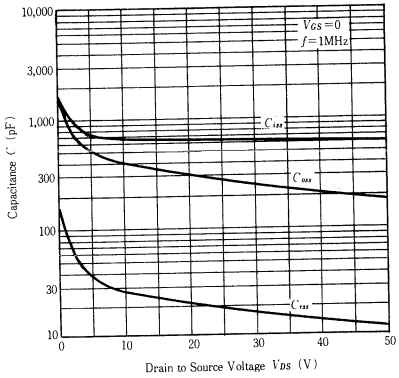
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



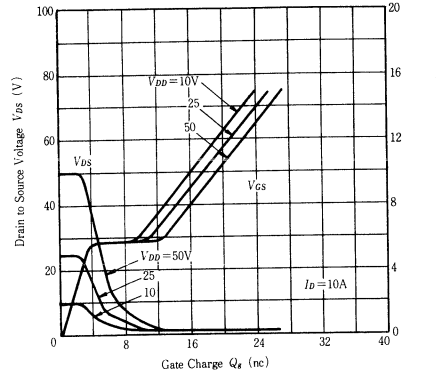
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



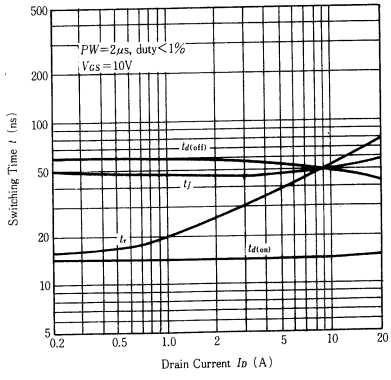
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



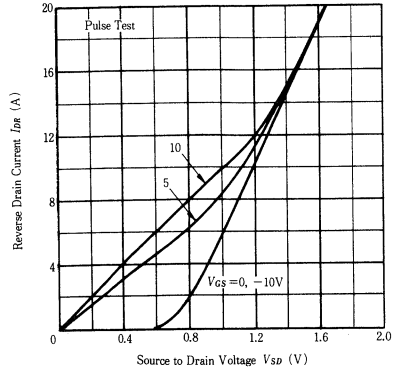
DYNAMIC INPUT CHARACTERISTICS



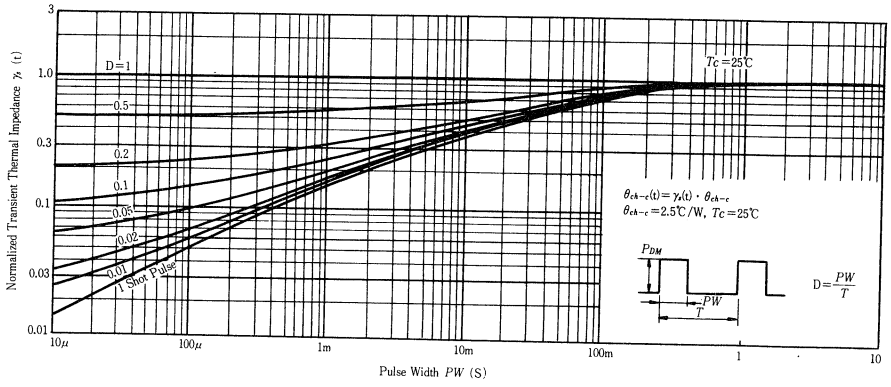
SWITCHING CHARACTERISTICS



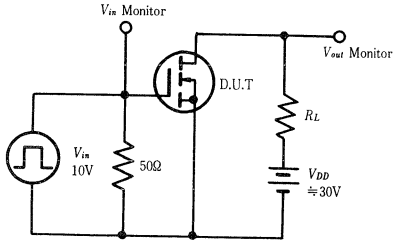
REVERSE DRAIN CURRENT VS. SOURCE - DRAIN VOLTAGE



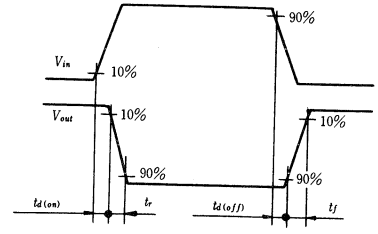
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



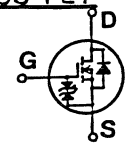
POWER MOS FET DII SERIES

2SK551

SILICON N CHANNEL MOS FET

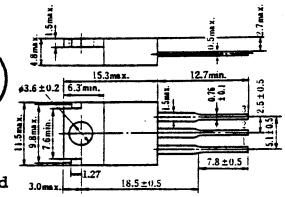
—Preliminary—

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

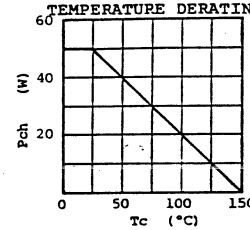
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	120	V
Gate-Source Voltage	V_{GSS}	±15	V
Drain Current	I_D	10	A
Drain Peak Current	$I_{D(pulse)}$*	40	A
Body-Drain Diode Reverse Drain Current	I_{DR}	10	A
Channel Dissipation	Pch**	50	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55 ~ +150	°C

*PW ≤ 10 μs, duty cycle ≤ 1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



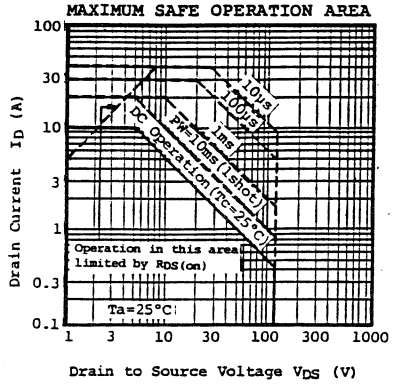
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D= 10mA , V_{GS}=0	120	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=± 12V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V , V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D= 1mA , V_{DS}= 10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D= 5A , V_{GS}=10V *	-	0.15	0.20	Ω
Foward Transfer Admittance	$\|yfs\|$	I_D= 5A , V_{DS}= 10V *	3.0	5.0	-	S
Input Capacitance	Ciss	V_{DS}= 10 V, V_{GS}=0 f=1MHz	-	730	-	pF
Output Capacitance	Coss		-	330	-	pF
Reverse Transfer Capacitance	Crss		-	40	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D= 5A , V_{GS}= 10V R_L= 6Ω	-	15	-	ns
Rise Time	t_r		-	40	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	70	-	ns
Fall Time	t_f		-	45	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F= 10A , V_{GS}=0	-	1.2	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F= 10A , V_{GS}=0 dI_F/dt= 50 A/μs	-	200	-	ns

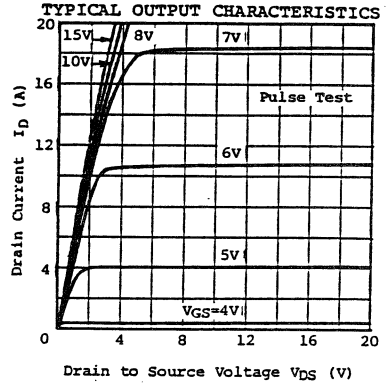
*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.
新製品のデータシートです。掲載内容は、予告なく変更されることがあります。

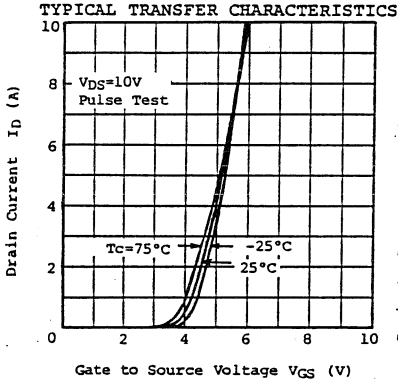
MAXIMUM SAFE OPERATION AREA



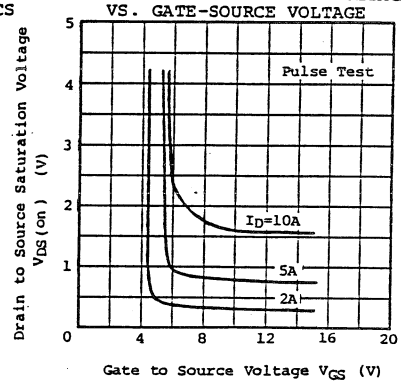
TYPICAL OUTPUT CHARACTERISTICS



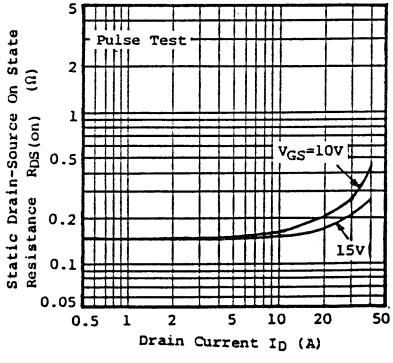
TYPICAL TRANSFER CHARACTERISTICS



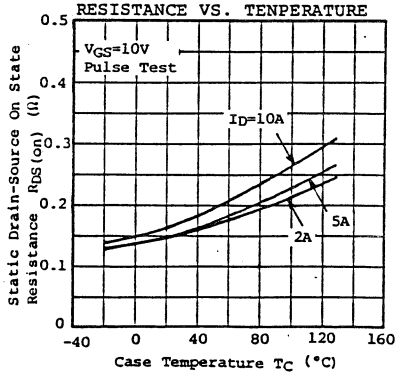
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



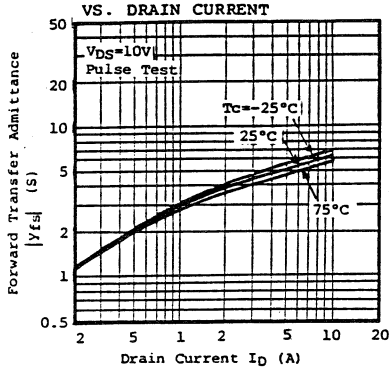
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



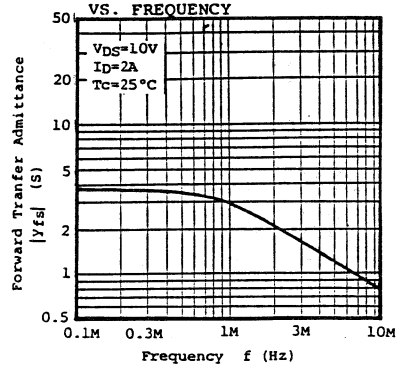
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



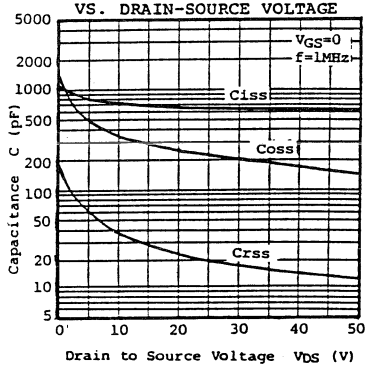
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



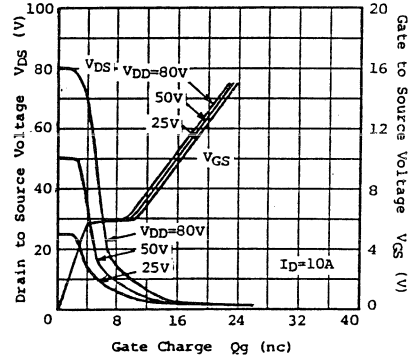
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



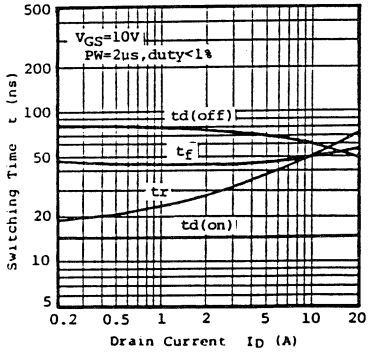
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



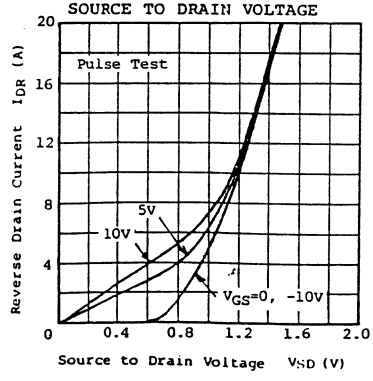
DYNAMIC INPUT CHARACTERISTICS



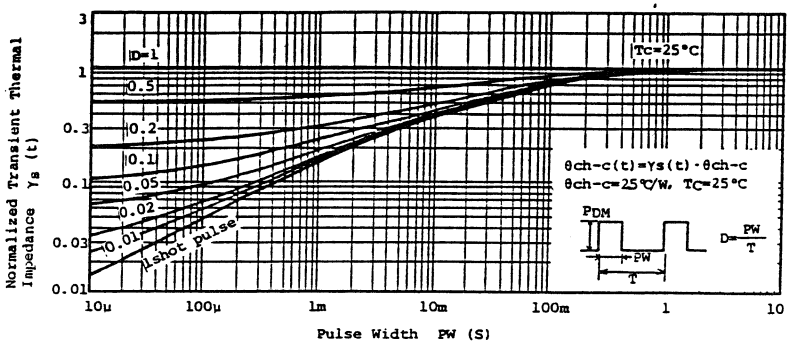
SWITCHING CHARACTERISTICS



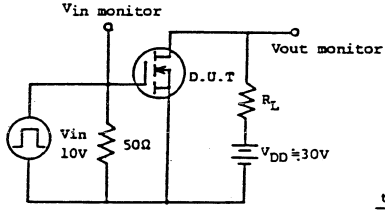
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



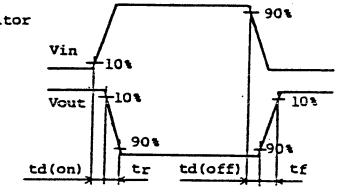
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



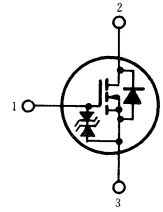
2SK552, 2SK553

SILICON N-CHANNEL MOS FET

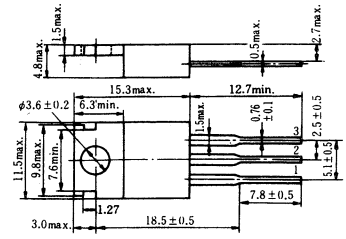
HIGH SPEED POWER SWITCHING

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source



(Dimensions in mm)

(JEDEC TO-220AB)

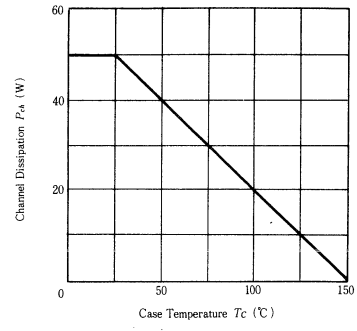
■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	2SK552	2SK553	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±15		V
Drain Current	I_D	5		A
Drain Peak Current	$I_{D(pulse)}$*	20		A
Body-Drain Diode Reverse Drain Current	I_{DR}	5		A
Channel Dissipation	P_{ch}**	50		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*PW≤10μs, duty cycle≤1%

**Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

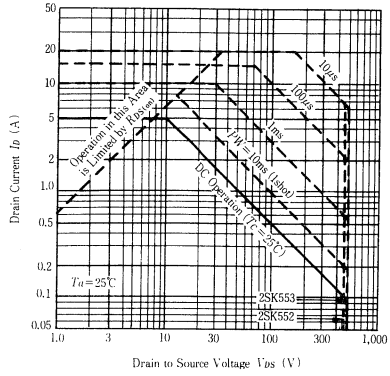


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

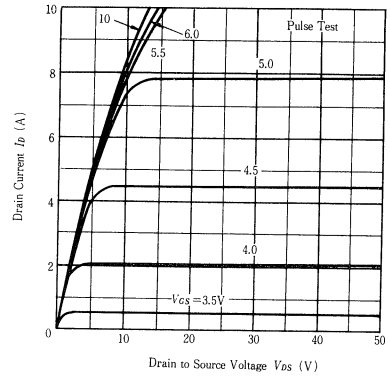
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK552	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	—	—	V
	2SK553			500	—	—	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±12V, V_{DS}=0	—	—	±10	μA
Zero Gate Voltage Drain Current	2SK552	I_{DSS}	V_{DS}=360V, V_{GS}=0	—	—	250	μA
	2SK553		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	4.0	V
Static Drain-Source On State Resistance		$R_{DS(on)}$	I_D=2.5A, V_{GS}=10V*	—	1.2	1.4	Ω
				—	1.2	1.5	
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=2.5A, V_{DS}=10V*	2.5	4.0	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	820	—	pF
Output Capacitance		C_{oss}		—	300	—	pF
Reverse Transfer Capacitance		C_{rss}		—	45	—	pF
Turn-on Delay Time		$t_{d(on)}$	I_D=2.5A, V_{GS}=10V, R_L=12Ω	—	10	—	ns
Rise Time		t_r		—	35	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	70	—	ns
Fall Time		t_f		—	45	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=5A, V_{GS}=0	—	1.0	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=5A, V_{GS}=0, di_F/dt=100A μs	—	300	—	ns

*Pulse Test

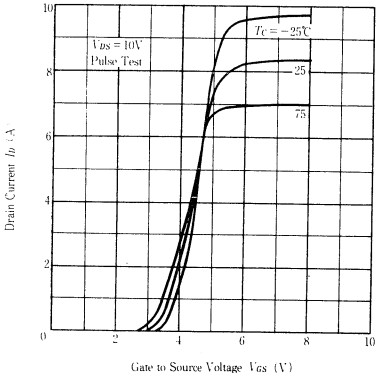
MAXIMUM SAFE OPERATION AREA



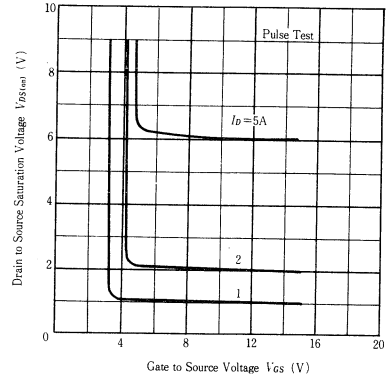
TYPICAL OUTPUT CHARACTERISTICS



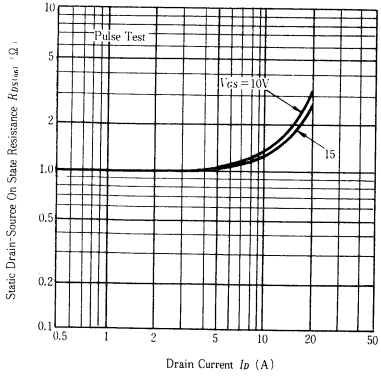
TYPICAL TRANSFER CHARACTERISTICS



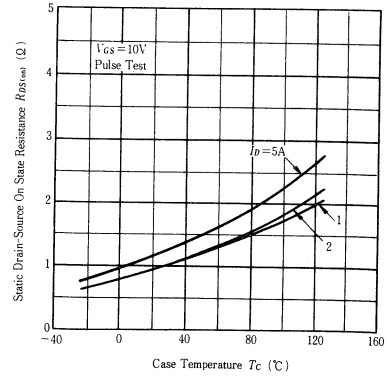
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



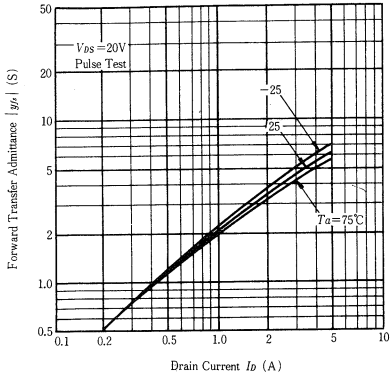
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



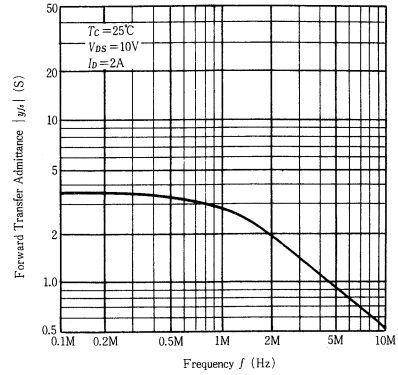
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



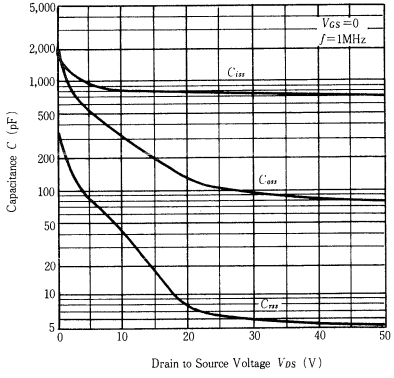
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



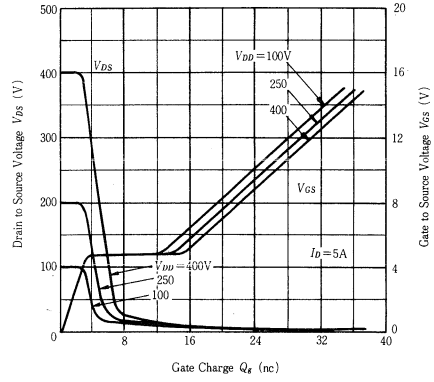
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



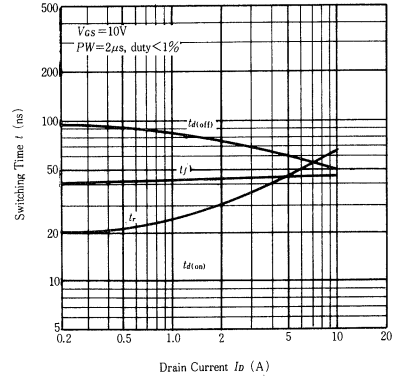
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



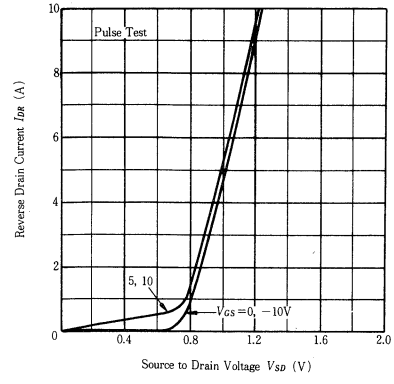
DYNAMIC INPUT CHARACTERISTICS



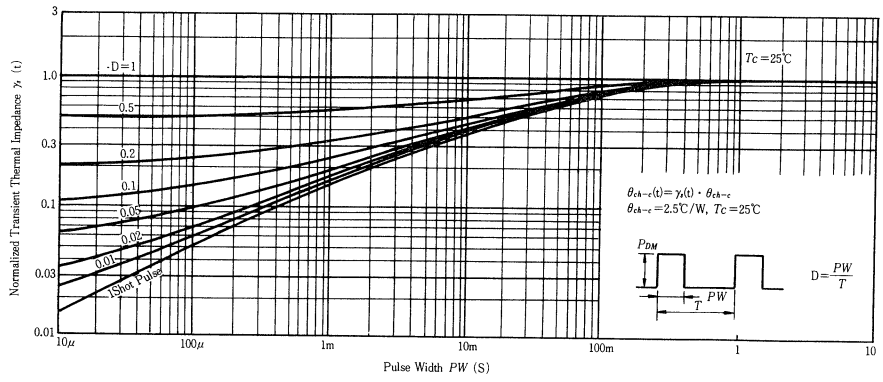
SWITCHING CHARACTERISTICS



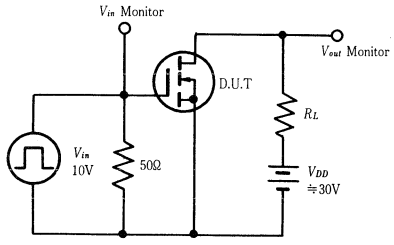
REVERSE DRAIN CURRENT VS. SOURCE - DRAIN VOLTAGE



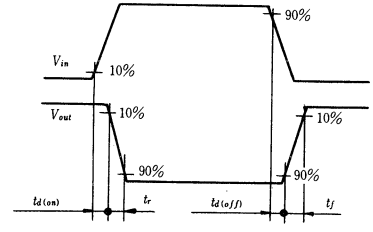
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



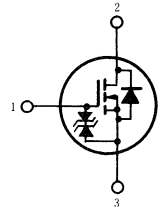
2SK554, 2SK555

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING

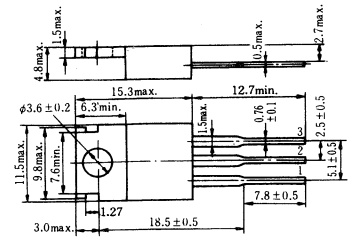
■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)



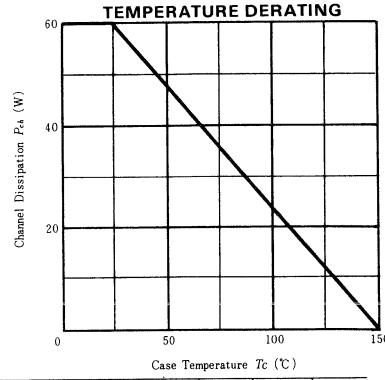
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	2SK554	2SK555	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±15		V
Drain Current	I_D	7		A
Drain Peak Current	$I_{D(pulse)}$*	28		A
Body-Drain Diode Reverse Drain Current	I_{DR}	7		A
Channel Dissipation	P_{ch}*	60		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*PW≤10μs, duty cycle≤1%
**Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

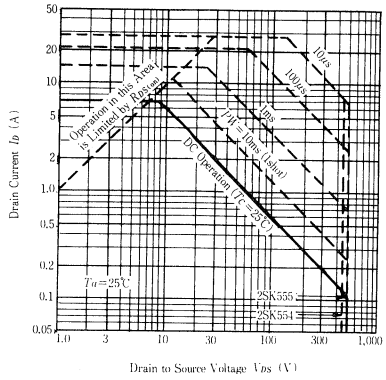


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

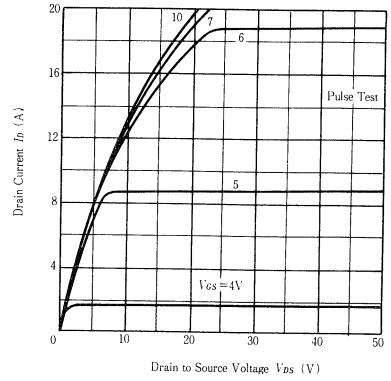
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK554	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	—	—	V
	2SK555			500	—	—	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±12V, V_{DS}=0	—	—	±10	μA
Zero Gate Voltage Drain Current	2SK554	I_{DSS}	V_{DS}=360V, V_{GS}=0	—	—	250	μA
	2SK555		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	4.0	V
Static Drain-Source On State Resistance	2SK554	$R_{DS(on)}$	I_D=4A, V_{GS}=10V*	—	0.6	0.85	Ω
	2SK555			—	0.7	1.0	
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=4A, V_{DS}=10V*	4.0	6.5	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	1300	—	pF
Output Capacitance		C_{oss}		—	470	—	pF
Reverse Transfer Capacitance		C_{rss}		—	65	—	pF
Turn-on Delay Time		$t_{d(on)}$	I_D=4A, V_{GS}=10V, R_L=7.5Ω	—	15	—	ns
Rise Time		t_r		—	50	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	100	—	ns
Fall Time		t_f		—	55	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=7A, V_{GS}=0	—	1.0	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=7A, V_{GS}=0, di_F/dt=100A/μs	—	400	—	ns

*Pulse Test

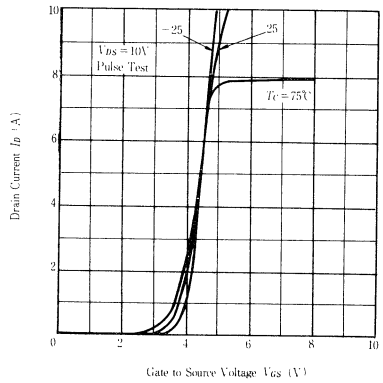
MAXIMUM SAFE OPERATION AREA



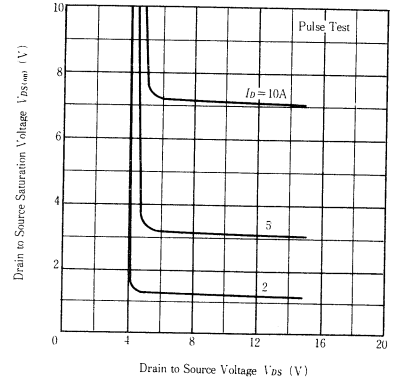
TYPICAL OUTPUT CHARACTERISTICS



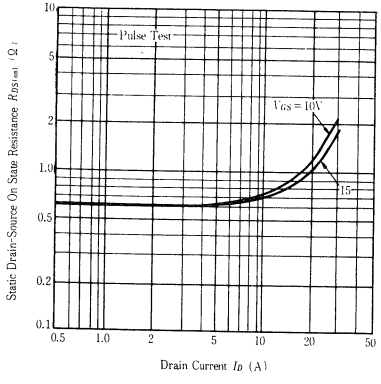
TYPICAL TRANSFER CHARACTERISTICS



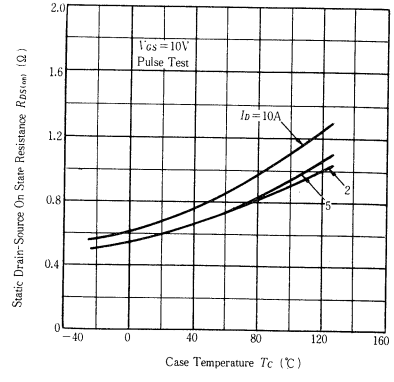
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



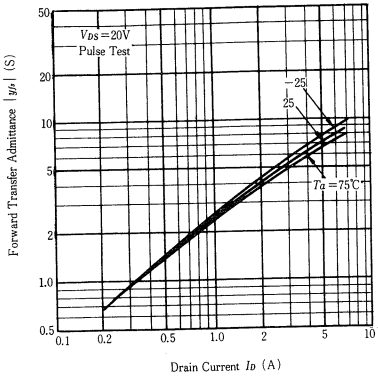
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



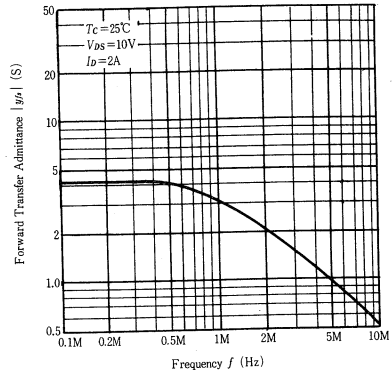
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



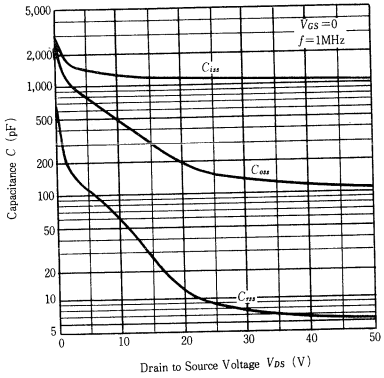
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



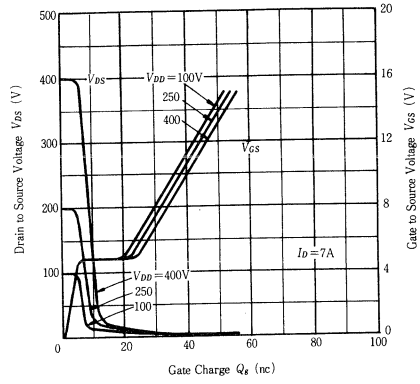
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



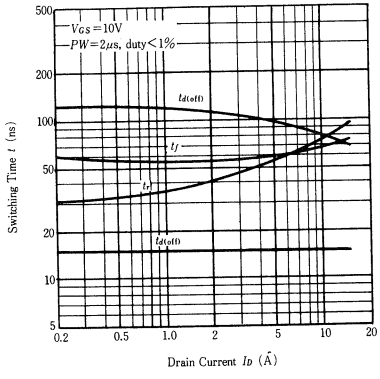
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



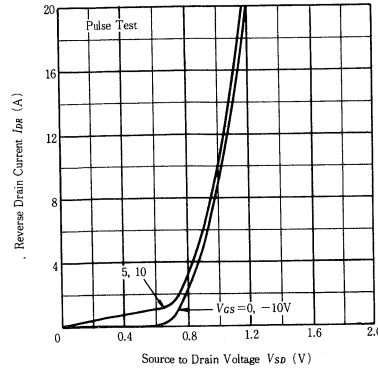
DYNAMIC INPUT CHARACTERISTICS



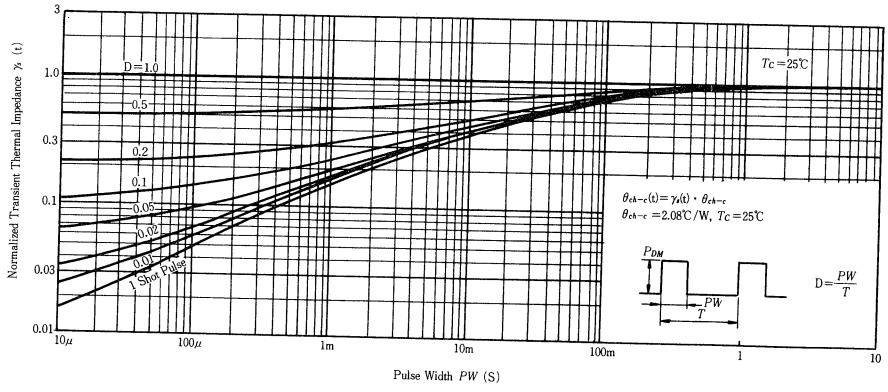
SWITCHING CHARACTERISTICS



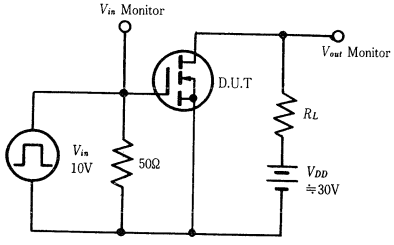
REVERSE DRAIN CURRENT VS. SOURCE - DRAIN VOLTAGE



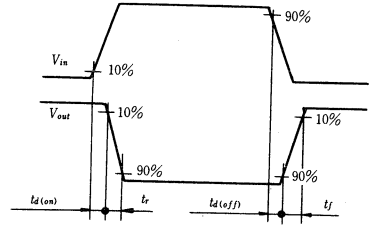
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



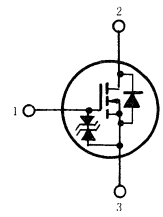
2SK556, 2SK557

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING

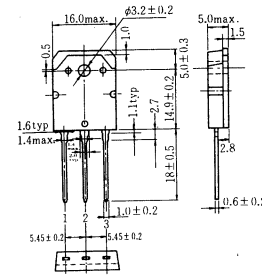
■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)



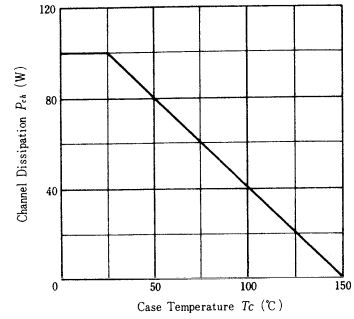
(TO-3P)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	2SK556	2SK557	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±15		V
Drain Current	I_D	12		A
Drain Peak Current	$I_{D(pulse)}$*	48		A
Body-Drain Diode Reverse Drain Current	I_{DR}	12		A
Channel Dissipation	P_{ch}*	100		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*PW≤10μs, duty cycle≤1%
**Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

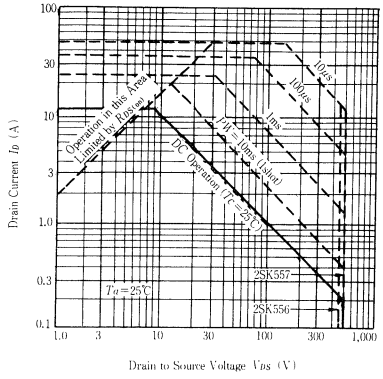


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

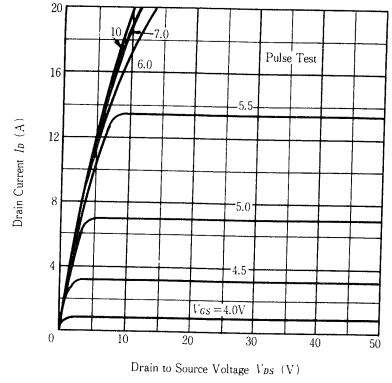
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK556	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	—	—	V
	2SK557			500	—	—	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±12V, V_{DS}=0	—	—	±10	μA
Zero Gate Voltage Drain Current	2SK556	I_{DSS}	V_{DS}=360V, V_{GS}=0	—	—	250	μA
	2SK557		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	4.0	V
Static Drain-Source On State Resistance	2SK556	$R_{DS(on)}$	I_D=6A, V_{GS}=10V*	—	0.4	0.55	Ω
	2SK557			—	0.45	0.60	
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=6A, V_{DS}=10V*	6	10	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	2050	—	pF
Output Capacitance		C_{oss}		—	720	—	pF
Reverse Transfer Capacitance		C_{rss}		—	80	—	pF
Turn-on Delay Time		$t_{d(on)}$	I_D=6A, V_{GS}=10V, R_L=5Ω	—	25	—	ns
Rise Time		t_r		—	85	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	145	—	ns
Fall Time		t_f		—	85	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=12A, V_{GS}=0	—	1.0	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=12A, V_{GS}=0, di_F/dt=100A/μs	—	450	—	ns

*Pulse Test

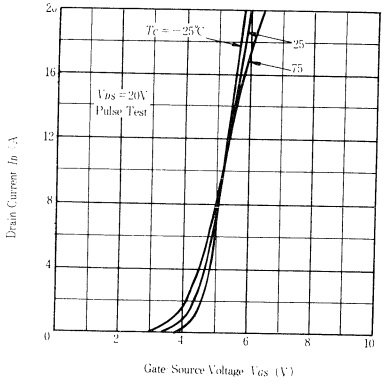
MAXIMUM SAFE OPERATION AREA



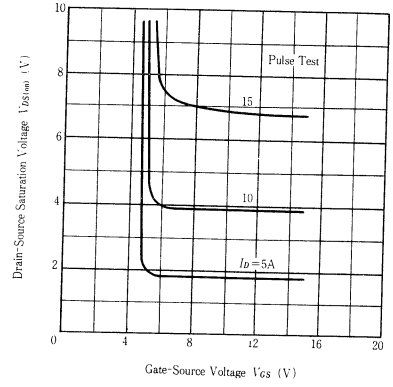
TYPICAL OUTPUT CHARACTERISTICS



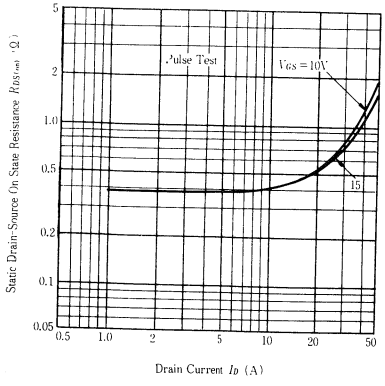
TYPICAL TRANSFER CHARACTERISTICS



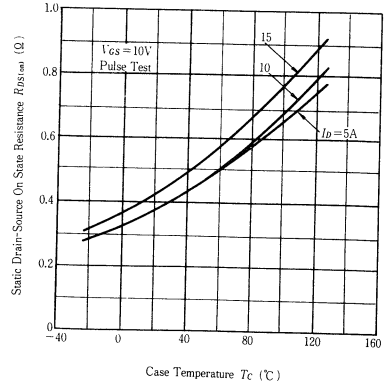
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



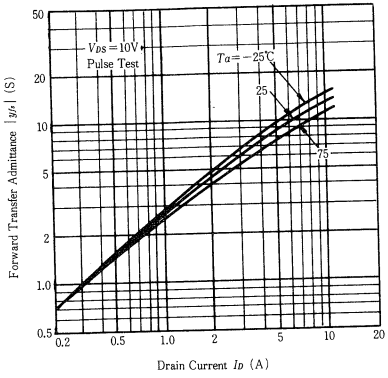
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



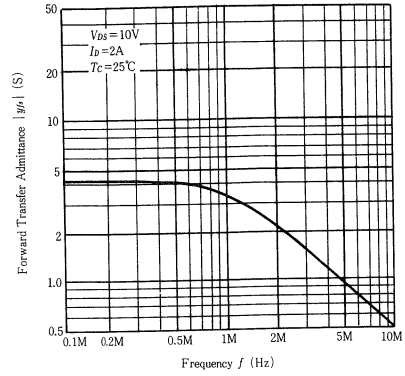
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



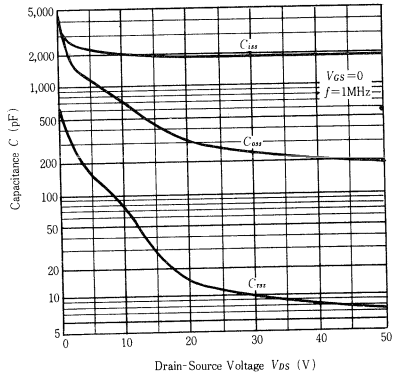
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



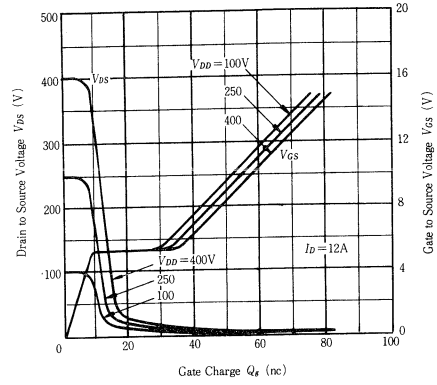
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



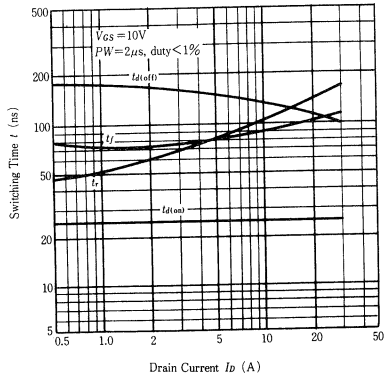
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



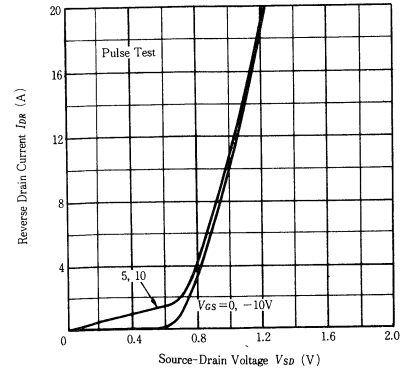
DYNAMIC INPUT CHARACTERISTICS



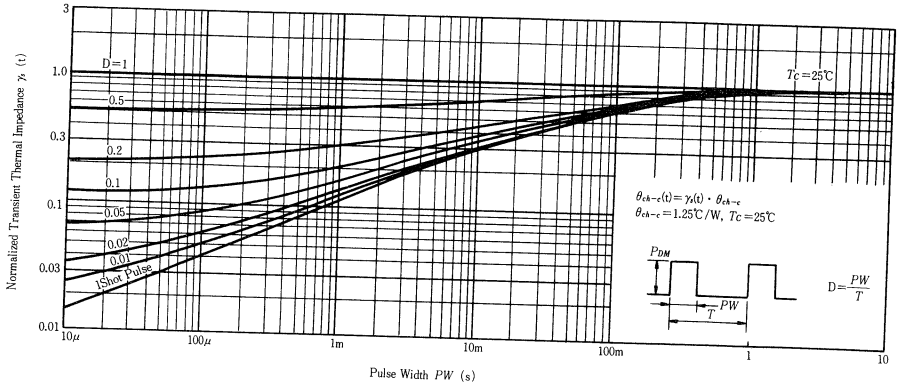
SWITCHING CHARACTERISTICS



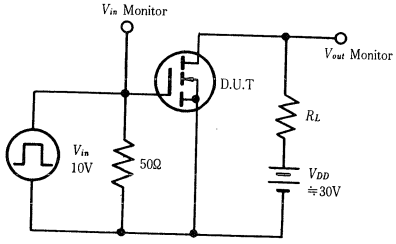
REVERSE DRAIN CURRENT VS. SOURCE - DRAIN VOLTAGE



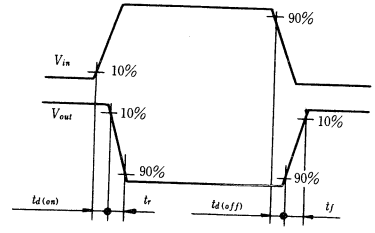
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



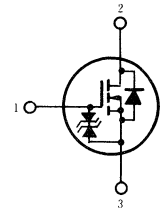
2SK559,2SK560

SILICON N-CHANNEL MOS FET

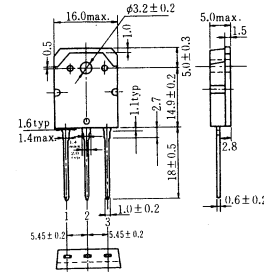
HIGH SPEED POWER SWITCHING

■ FEATURES

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source



(TO-3P)

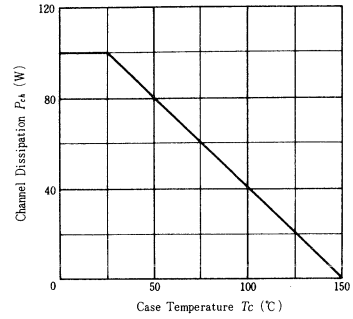
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	2SK559	2SK560	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±15		V
Drain Current	I_D	15		A
Drain Peak Current	$I_{D(pulse)}$*	60		A
Body-Drain Diode Reverse Drain Current	I_{DR}	15		A
Channel Dissipation	P_{ch}*	100		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*PW≤10μs, duty cycle≤1%
**Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

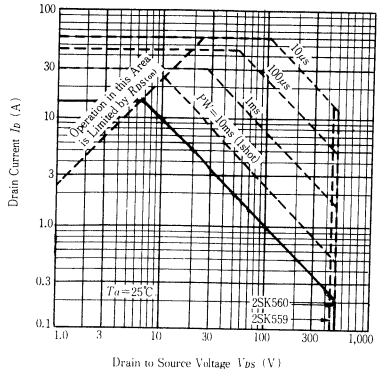


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

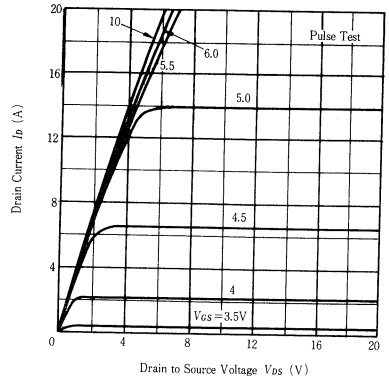
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK559	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	—	—	V
	2SK560			500	—	—	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±12V, V_{DS}=0	—	—	±10	μA
Zero Gate Voltage Drain Current	2SK559	I_{DSS}	V_{DS}=360V, V_{GS}=0	—	—	250	μA
	2SK560		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	4.0	V
Static Drain-Source On State Resistance	2SK559	$R_{DS(on)}$	I_D=8A, V_{GS}=10V*	—	0.25	0.36	Ω
	2SK560			—	0.3	0.4	
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=8A, V_{DS}=10V*	8	13	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	2950	—	pF
Output Capacitance		C_{oss}		—	1100	—	pF
Reverse Transfer Capacitance		C_{rss}		—	140	—	pF
Turn-on Delay Time		$t_{d(on)}$	I_D=8A, V_{GS}=10V, R_L=3.75Ω	—	30	—	ns
Rise Tim		t_r		—	115	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	200	—	ns
Fall Time		t_f		—	120	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=15A, V_{GS}=0	—	1.2	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=15A, V_{GS}=0, di_F/dt=100A/μs	—	500	—	ns

*Pulse Test

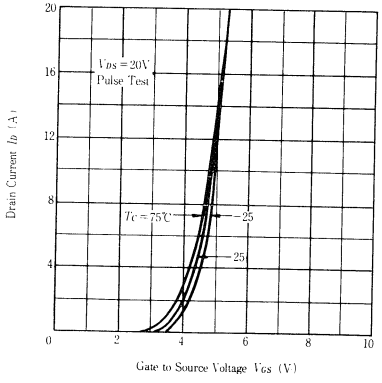
MAXIMUM SAFE OPERATION AREA



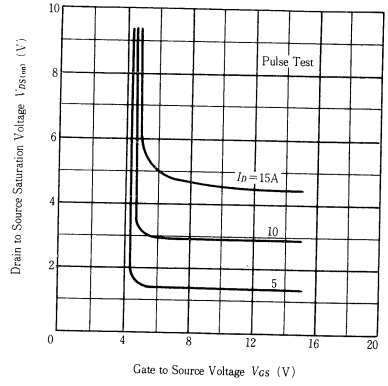
TYPICAL OUTPUT CHARACTERISTICS



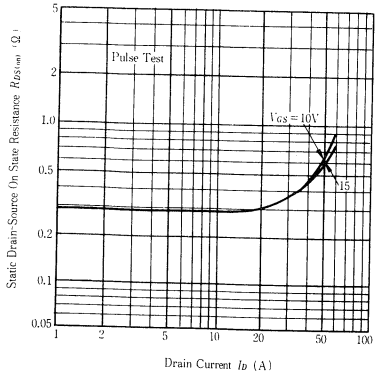
TYPICAL TRANSFER CHARACTERISTICS



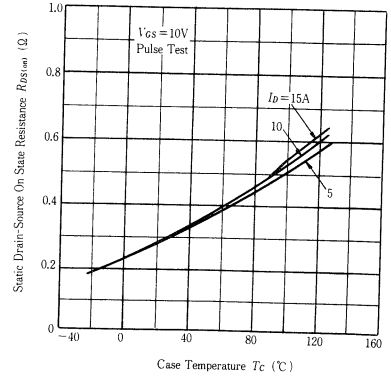
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



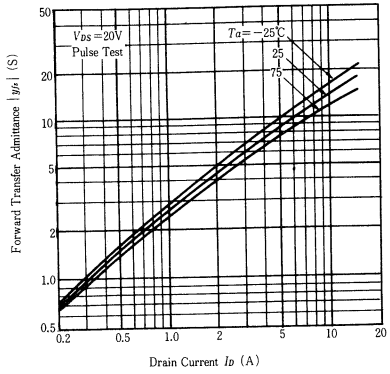
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



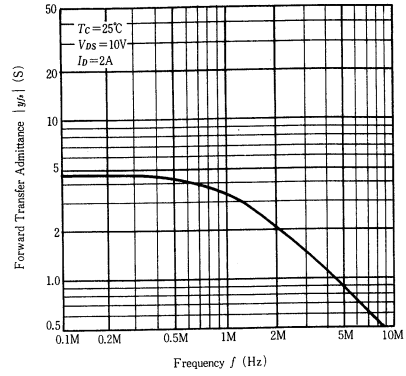
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



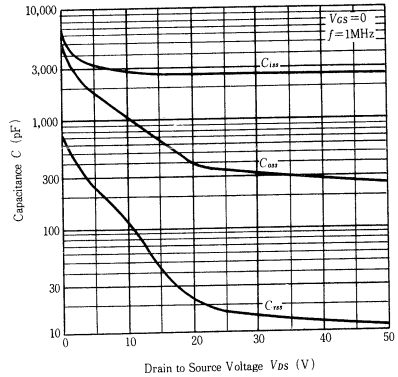
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



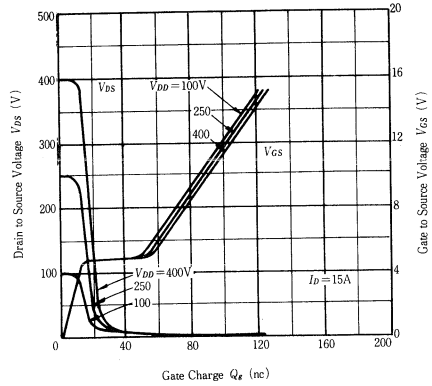
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



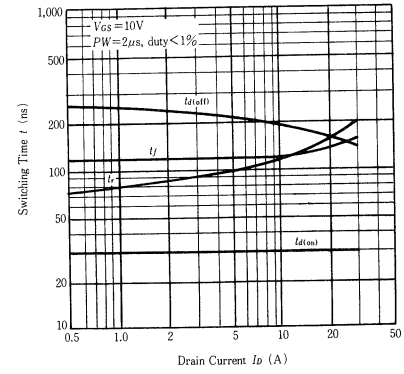
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



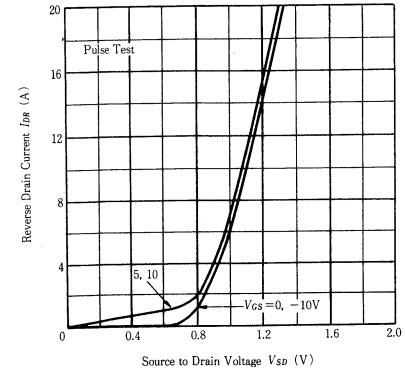
DYNAMIC INPUT CHARACTERISTICS



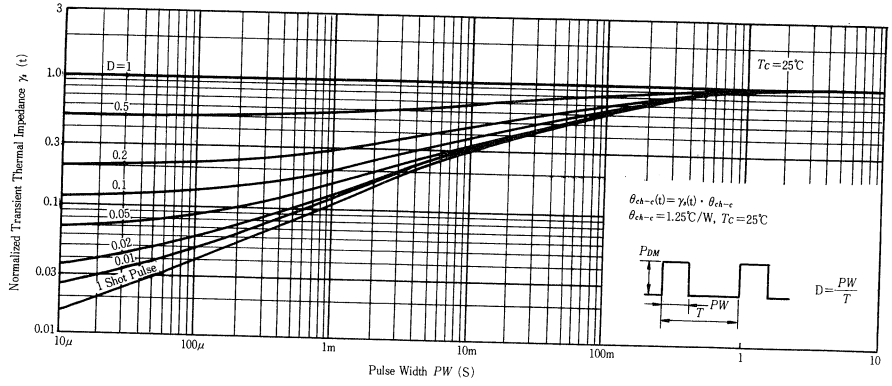
SWITCHING CHARACTERISTICS



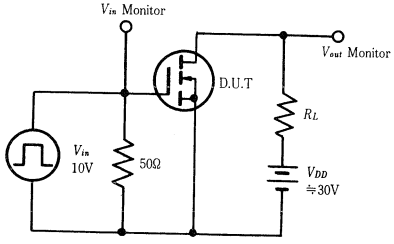
REVERSE DRAIN CURRENT VS. SOURCE - DRAIN VOLTAGE



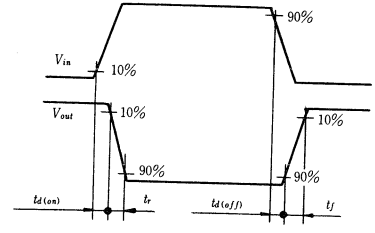
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



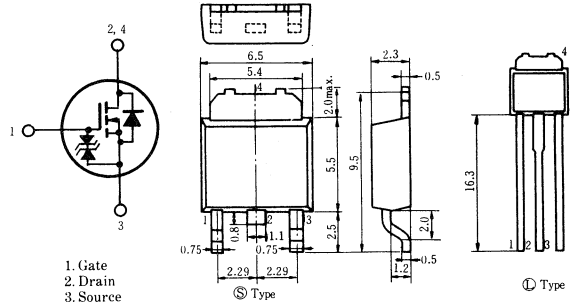
2SK579Ⓛ,2SK580Ⓛ,
2SK579Ⓢ,2SK580Ⓢ

SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING

■ FEATURES

- Small Package.
- High Speed Switching.
- Low Drive Current.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls, and Ultrasonic Power Oscillators.



1. Gate
2. Drain
3. Source
4. Drain

(Dimensions in mm)

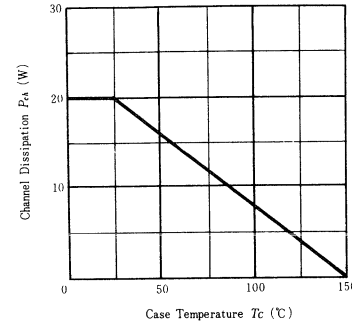
(DPAK)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	2SK579	2SK580	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±15		V
Drain Current	I_D	1.5		A
Drain Peak Current	$I_{D(pulse)}$*	6		A
Body-Drain Diode Reverse Drain Current	I_{DR}	1.5		A
Channel Dissipation	P_{ch}**	20		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−65 ~ +150		°C

*PW≤10μs, duty cycle≤1%
**Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

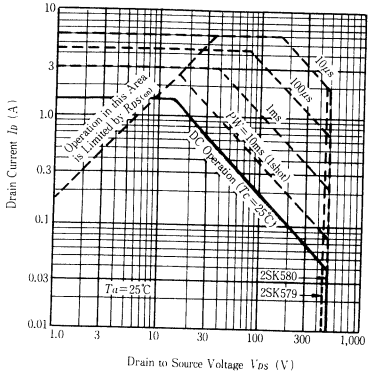


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

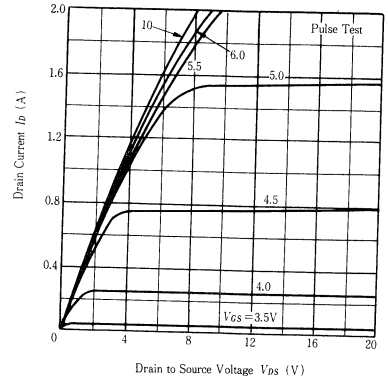
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK579	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	—	—	V
	2SK580			500	—	—	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	—	—	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±12V, V_{DS}=0	—	—	±10	μA
Zero Gate Voltage Drain Current	2SK579	I_{DSS}	V_{DS}=360V, V_{GS}=0	—	—	100	μA
	2SK580		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	—	4.0	V
Static Drain-Source On State Resistance	2SK579	$R_{DS(on)}$	I_D=1A, V_{GS}=10V*	—	3.5	5.5	Ω
	2SK580			—	4.0	6.0	
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=1A, V_{DS}=20V*	0.6	1.0	—	S
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0 f=1MHz	—	260	—	pF
Output Capacitance		C_{oss}		—	95	—	pF
Reverse Transfer Capacitance		C_{rss}		—	12	—	pF
Turn-on Delay Time		$t_{d(on)}$	I_D=1A, V_{GS}=10V R_L=30Ω	—	8	—	ns
Rise Time		t_r		—	20	—	ns
Turn-off Delay Time		$t_{d(off)}$		—	28	—	ns
Fall Time		t_f		—	20	—	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=1.5A, V_{GS}=0	—	1.0	—	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=1.5A, V_{GS}=0 di_F/dt=100A/μs	—	250	—	ns

*Pulse Test

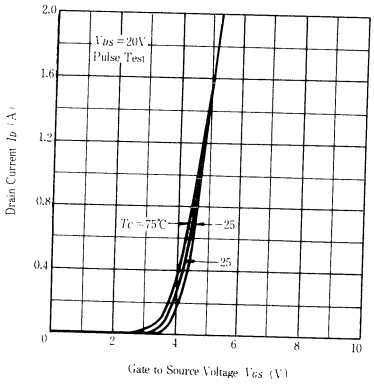
MAXIMUM SAFE OPERATION AREA



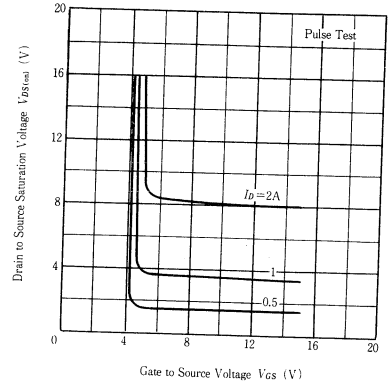
TYPICAL OUTPUT CHARACTERISTICS



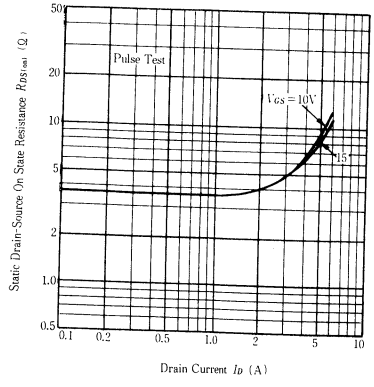
TYPICAL TRANSFER CHARACTERISTICS



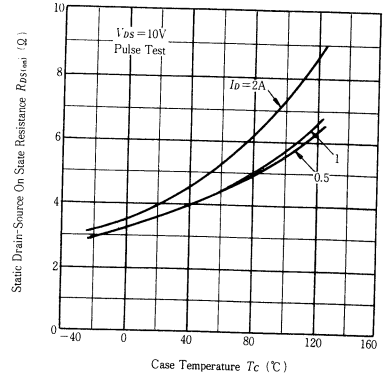
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



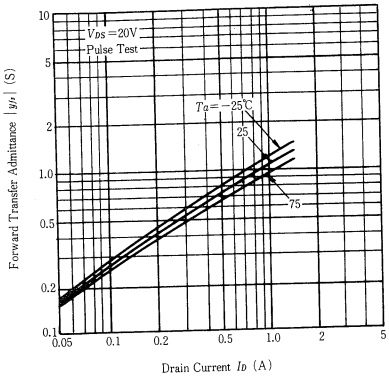
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



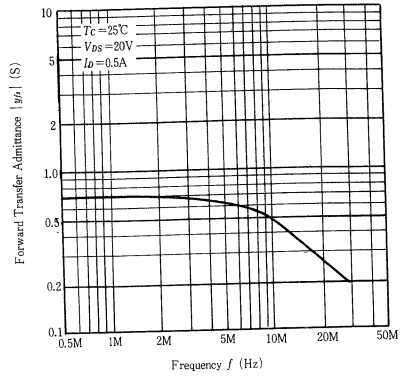
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



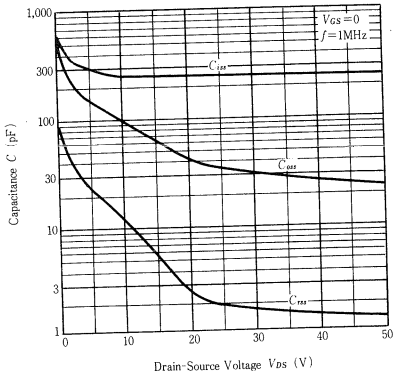
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



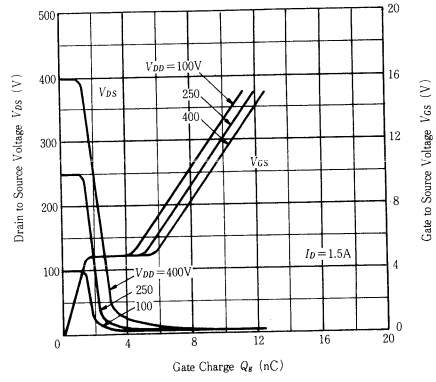
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



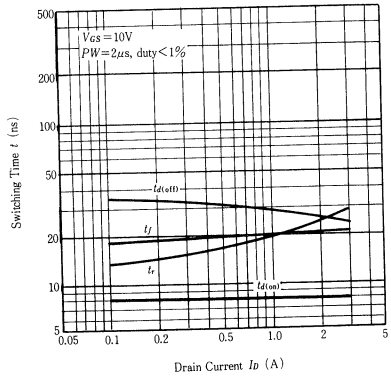
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



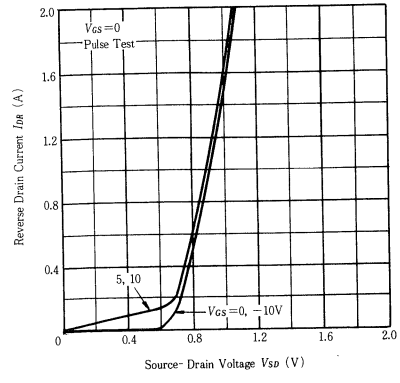
DYNAMIC INPUT CHARACTERISTICS



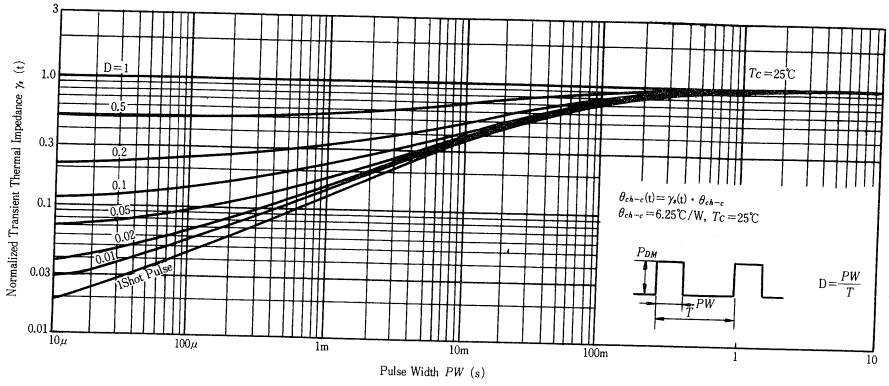
SWITCHING CHARACTERISTICS



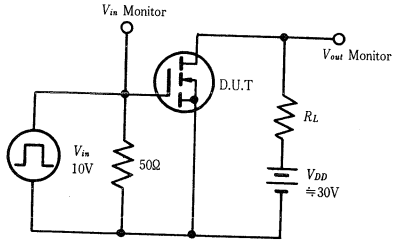
REVERSE DRAIN CURRENT VS. SOURCE - DRAIN VOLTAGE



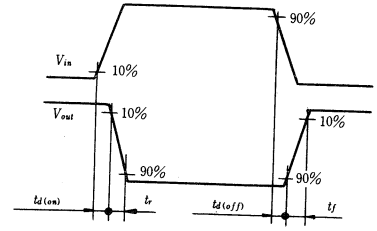
NORMALIZD TRANSIEMENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



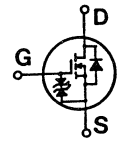
POWER MOS FET DII SERIES

2SK600

SILICON N CHANNEL MOS FET

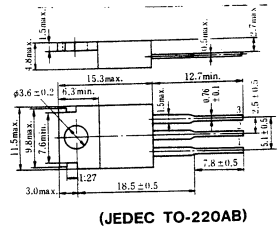
—Preliminary—

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

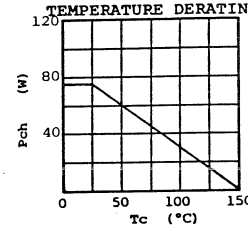
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±15	V
Drain Current	I_D	25	A
Drain Peak Current	$I_{D(pulse)}$*	100	A
Body-Drain Diode Reverse Drain Current	I_{DR}	25	A
Channel Dissipation	Pch**	75	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 ~ +150	°C

*PW≤10μs, duty cycle≤1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



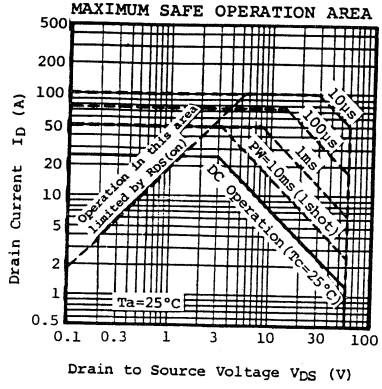
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	60	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±12V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=15A, V_{GS}=10V *	-	0.04	0.055	Ω
Foward Transfer Admittance	$\|Yfs\|$	I_D=15A, V_{DS}=10V *	9	15	-	S
Input Capacitance	Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	2000	-	pF
Output Capacitance	Coss		-	1200	-	pF
Reverse Transfer Capacitance	Crss		-	80	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=15A, V_{GS}=10V R_L=2Ω	-	30	-	ns
Rise Time	t_r		-	100	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	110	-	ns
Fall Time	t_f		-	85	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=25A, V_{GS}=0	-	1.3	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=25A, V_{GS}=0 dIF/dt=50 A/μs	-	350	-	ns

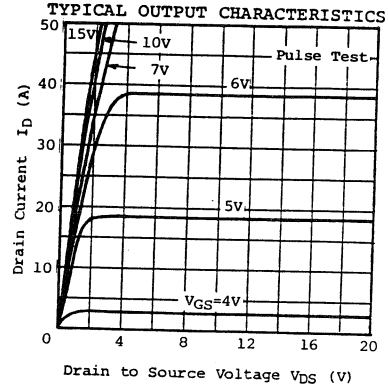
*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

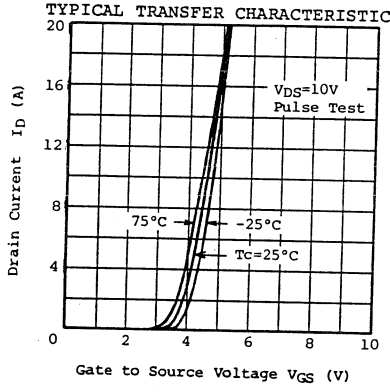
MAXIMUM SAFE OPERATION AREA



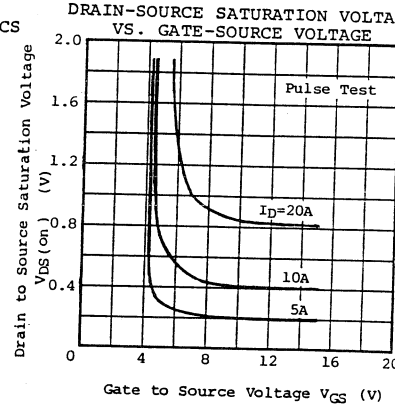
TYPICAL OUTPUT CHARACTERISTICS



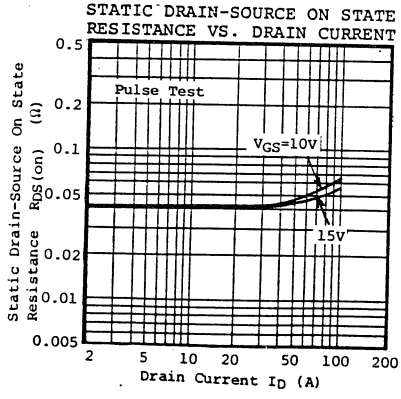
TYPICAL TRANSFER CHARACTERISTICS



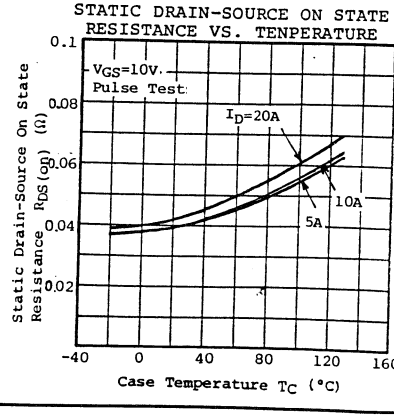
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



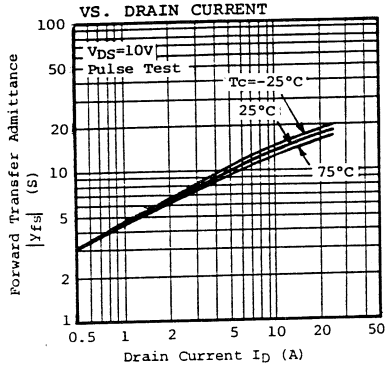
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



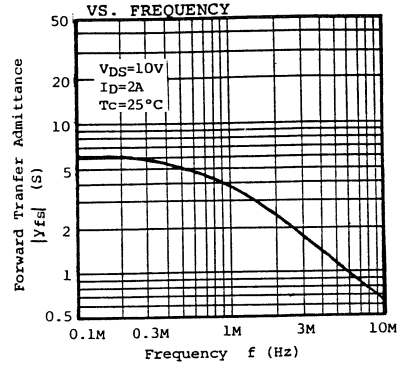
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



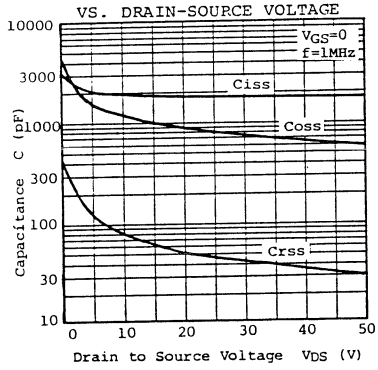
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



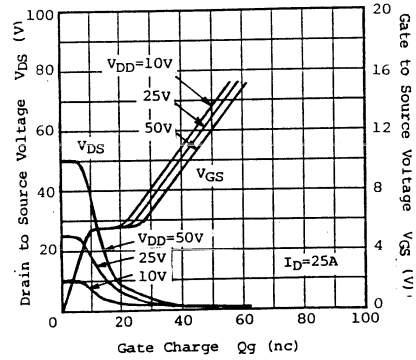
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



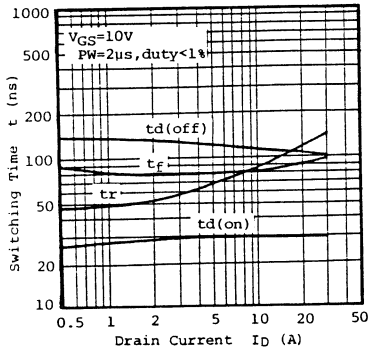
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



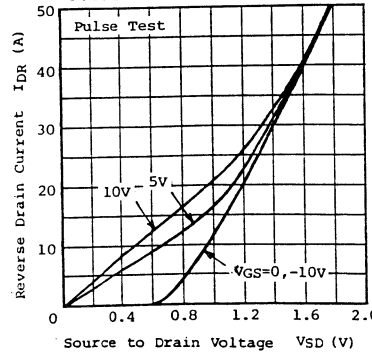
DYNAMIC INPUT CHARACTERISTICS



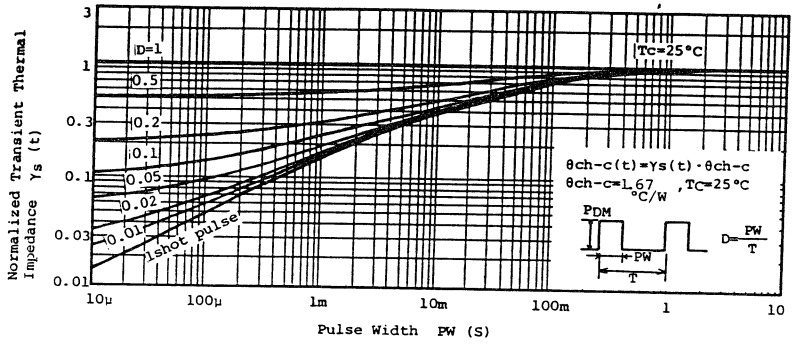
SWITCHING CHARACTERISTICS



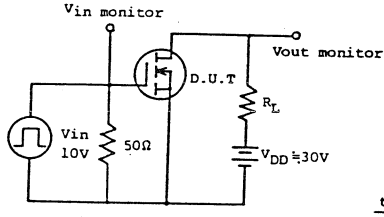
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



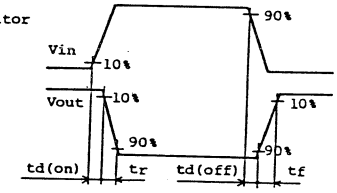
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS

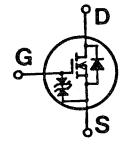


POWER MOS FET DII SERIES

2SK622

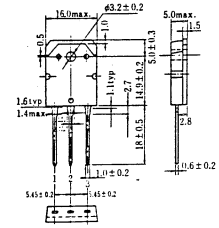
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls.



1. ゲート：Gate
2. ドレイン：Drain (フランジ) (Flange)
3. ソース：Source

(Dimensions in mm)

(TO-3P)

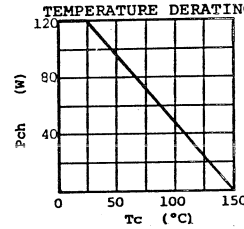
■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	150	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	20	A
Drain Peak Current	$I_{D(pulse)}$*	80	A
Body-Drain Diode Reverse Drain Current	I_{DR}	20	A
Channel Dissipation	Pch**	120	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55 ~ +150	°C

* PW=10μs, duty≤1%

**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING

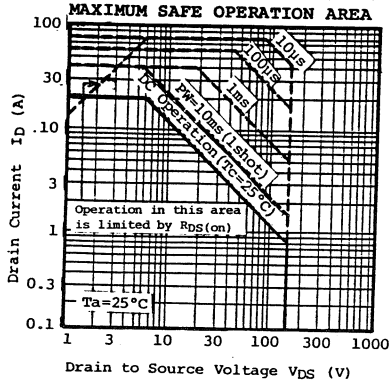


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

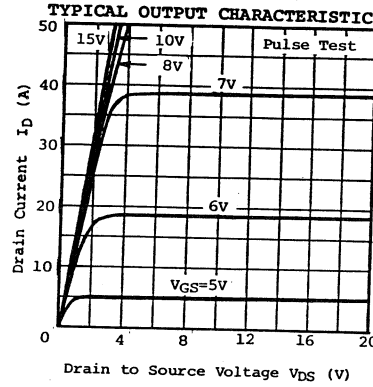
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	150	–	–	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{GS}=0	±20	–	–	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	–	–	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=120V, V_{GS}=0	–	–	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	–	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=10A, V_{GS}=10V *	–	0.06	0.075	Ω
Foward Transfer Admittance	|yfs|	I_D=10A, V_{DS}=10V *	9	15	–	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz	–	2200	–	pF
Output Capacitance	Coss		–	1000	–	pF
Reverse Transfer Capacitance	Crss		–	220	–	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=10A, V_{GS}=10V R_L=3Ω	–	35	–	ns
Rise Time	t_r		–	190	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	200	–	ns
Fall Time	t_f		–	160	–	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=20A, V_{GS}=0	–	1.2	–	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=20A, V_{GS}=0 dI_F/dt=50 A/μs	–	250	–	ns

*Pulse Test

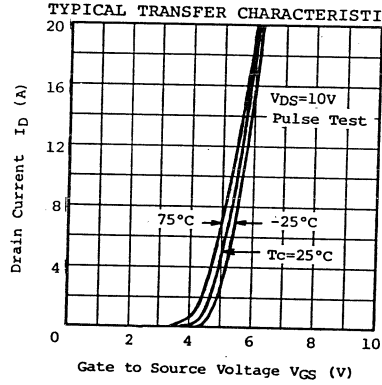
MAXIMUM SAFE OPERATION AREA



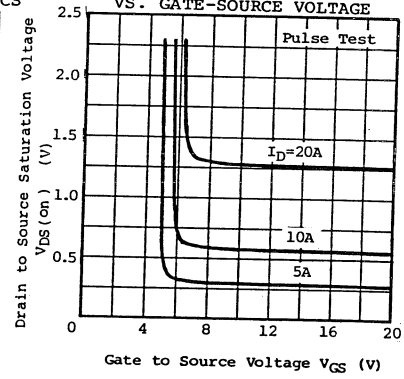
TYPICAL OUTPUT CHARACTERISTICS



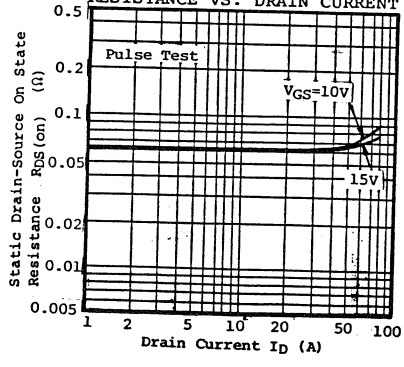
TYPICAL TRANSFER CHARACTERISTICS



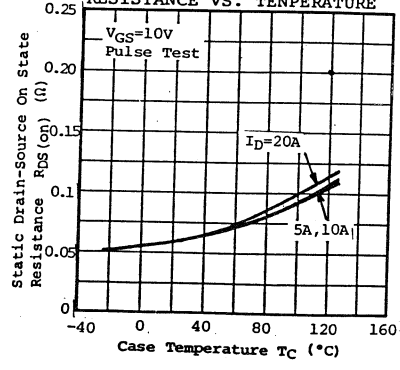
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



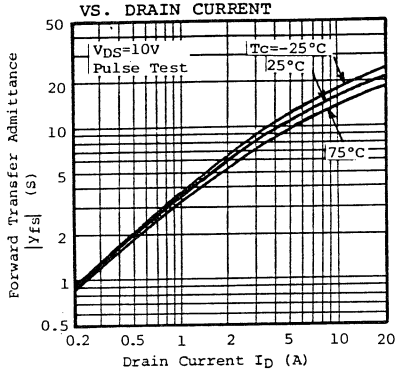
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



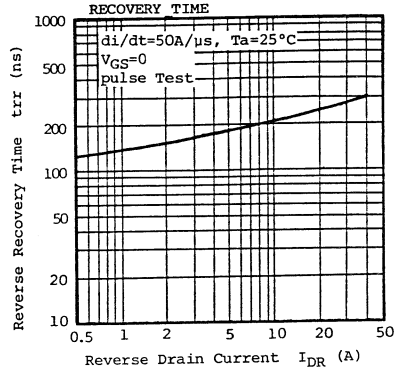
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



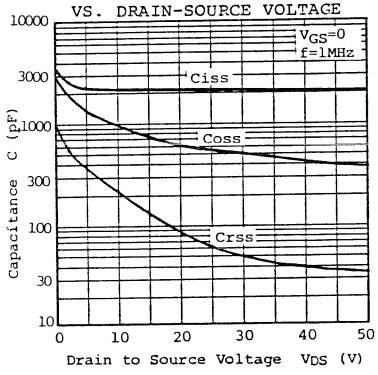
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



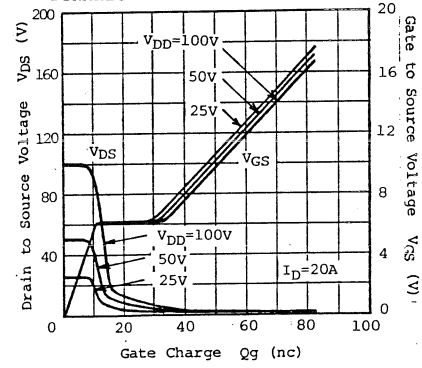
BODY-DRAIN DIODE REVERSE RECOVERY TIME



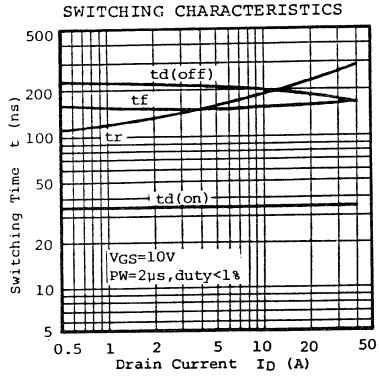
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



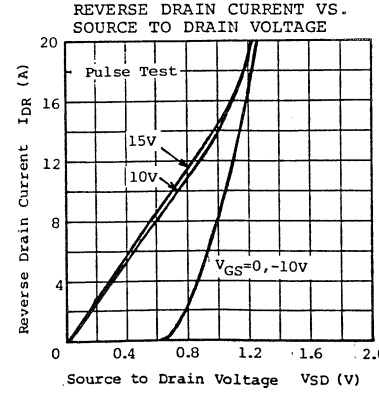
DYNAMIC INPUT CHARACTERISTICS



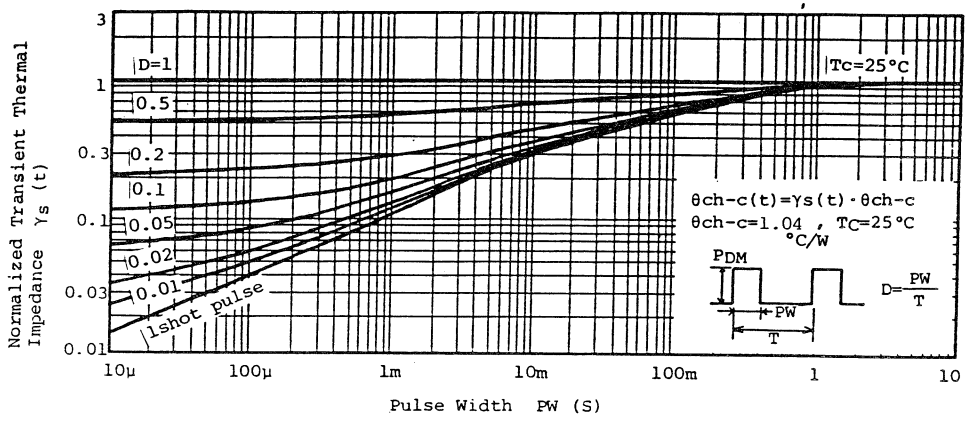
SWITCHING CHARACTERISTICS



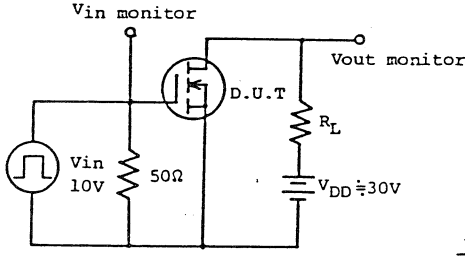
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



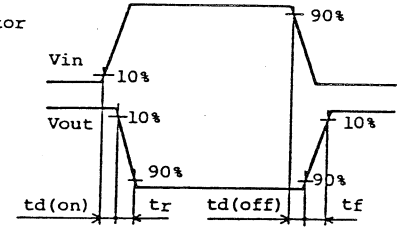
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



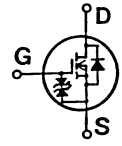
Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

POWER MOS FET DII SERIES

2SK623

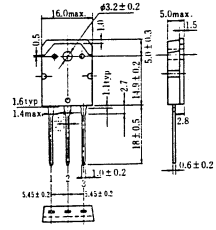
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls.



1. ゲート：Gate
2. ドレイン：Drain (フランジ) (Flange)
3. ソース：Source

(Dimensions in mm)

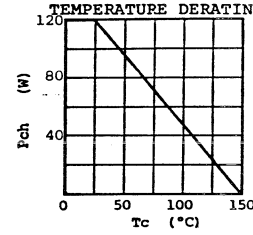
(TO-3P)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	250	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	20	A
Drain Peak Current	$I_{D(pulse)}$*	80	A
Body-Drain Diode Reverse Drain Current	I_{DR}	20	A
Channel Dissipation	Pch**	120	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55～+150	°C

* PW≦10μs, duty≦1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING

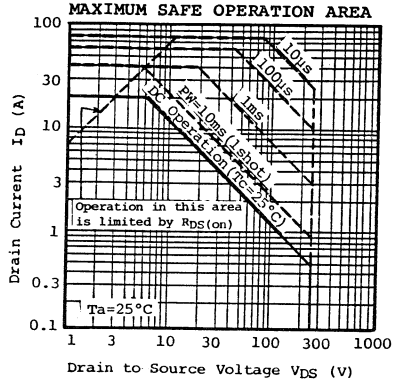


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

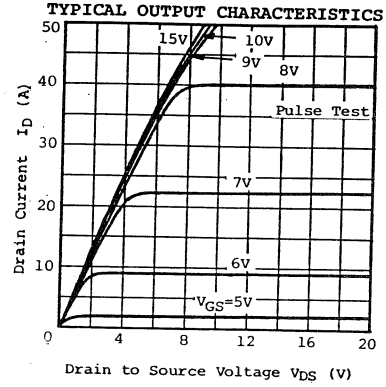
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	250	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=200V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=10A, V_{GS}=10V *	-	0.12	0.15	Ω
Foward Transfer Admittance	$\|yfs\|$	I_D=10A, V_{DS}=10V *	7	12	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz	-	2000	-	pF
Output Capacitance	Coss		-	950	-	pF
Reverse Transfer Capacitance	Crss		-	270	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=10A, V_{GS}=10V R_L=3Ω	-	25	-	ns
Rise Time	t_r		-	200	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	200	-	ns
Fall Time	t_f		-	160	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=20A, V_{GS}=0	-	1.2	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=20A, V_{GS}=0 dI_F/dt=50 A/μs	-	450	-	ns

*Pulse Test

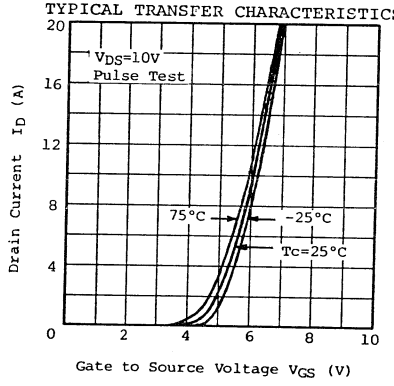
MAXIMUM SAFE OPERATION AREA



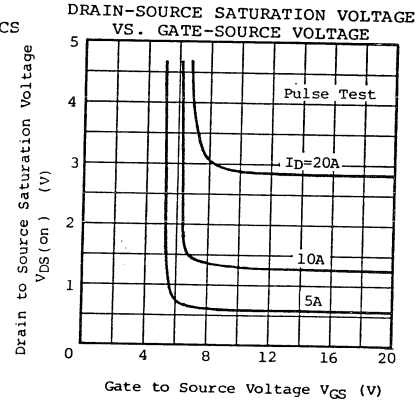
TYPICAL OUTPUT CHARACTERISTICS



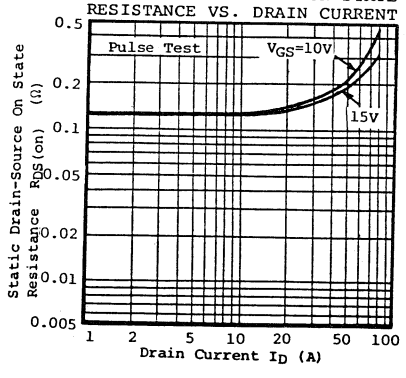
TYPICAL TRANSFER CHARACTERISTICS



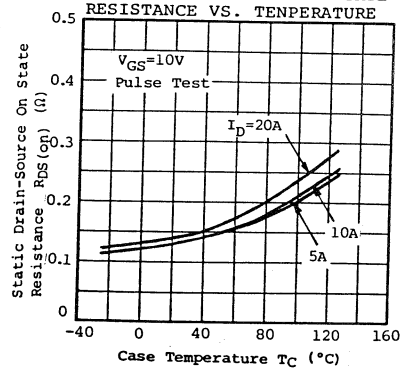
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



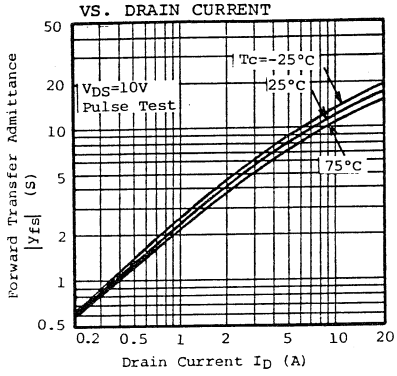
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



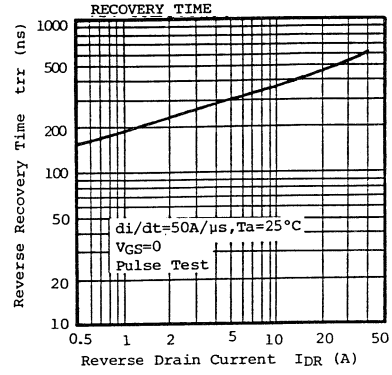
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



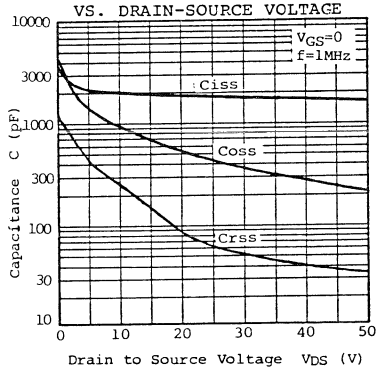
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



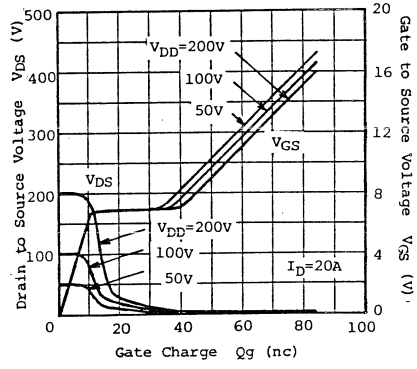
BODY-DRAIN DIODE REVERSE RECOVERY TIME



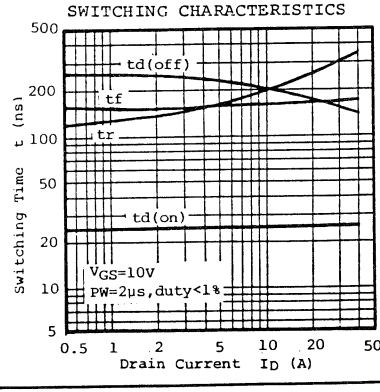
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



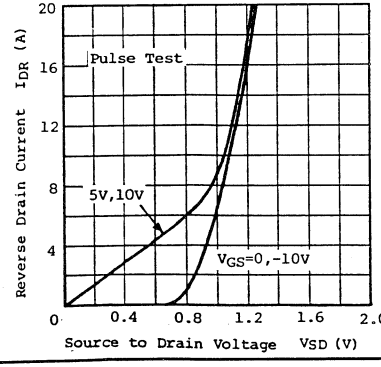
DYNAMIC INPUT CHARACTERISTICS



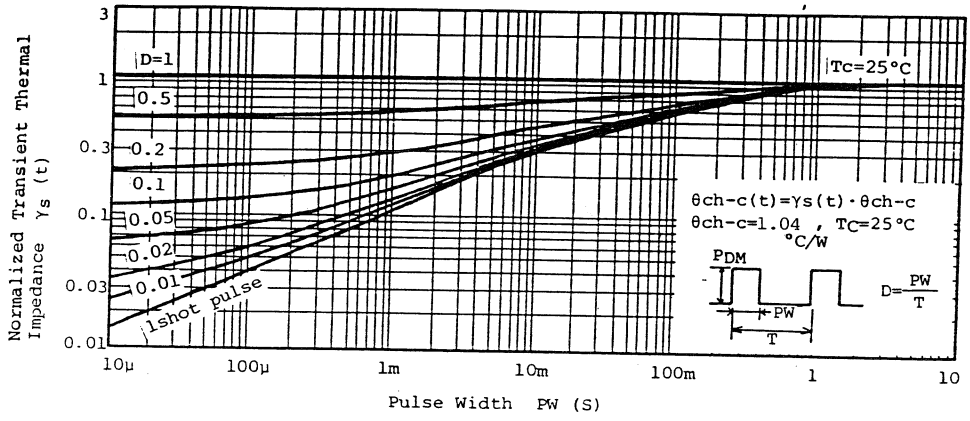
SWITCHING CHARACTERISTICS



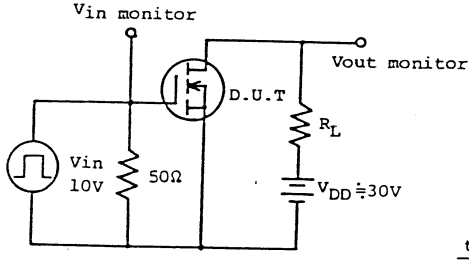
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



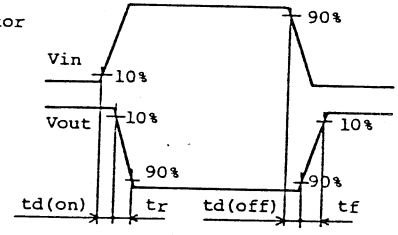
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



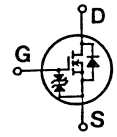
Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

POWER MOS FET DII SERIES

2SK641, 2SK642 —Preliminary—

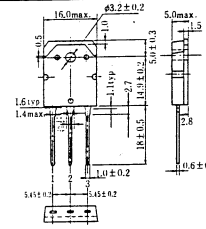
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls.



1. ゲート：Gate
2. ドレイン：Drain (フランジ) (Flange)
3. ソース：Source

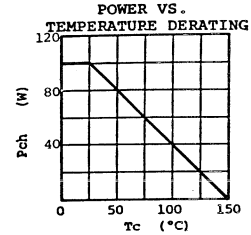
(Dimensions in mm)

(TO-3P)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	K641	K642	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±15		V
Drain Current	I_D	10		A
Drain Peak Current	$I_{D(pulse)}^*$	30		A
Body-Drain Diode Reverse Drain Current	I_{DR}	10		A
Channel Dissipation	Pch**	100		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	−55 ~ +150		°C

*PW≤10μs, duty cycle≤1%　　**Value at Tc=25°C



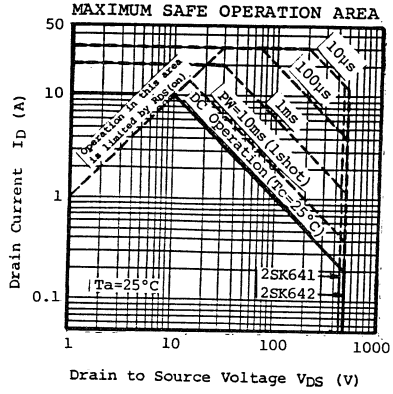
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item		Symbol	Test Condition		min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	K641	$V_{(BR)DSS}$	I_D= 10mA , V_{GS}=0		450	-	-	V
	K642				500	-	-	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0		±15	-	-	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=± 12V, V_{DS}=0		-	-	±10	μA
Zero Gate Voltage Drain Current	K641	I_{DSS}	V_{DS}=360V , V_{GS}=0		-	-	250	μA
	K642		V_{DS}=400V , V_{GS}=0					
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D= 1mA , V_{DS}= 10V		2.0	-	4.0	V
Static Drain-Source on State Resistance	K641	$R_{DS(on)}$	I_D= 5A , V_{GS}=10V	*	-	0.6	0.8	Ω
	K642				-	0.7	1.0	
Foward Transfer Admittance		$\|yfs\|$	I_D= 5A , V_{DS}= 10V	*	4.0	7.0	-	S
Input Capacitance		Ciss	V_{DS}= 10 V, V_{GS}=0 f=1MHz		-	1300	-	pF
Output Capacitance		Coss			-	470	-	pF
Reverse Transfer Capacitance		Crss			-	65	-	pF
Turn-On Delay Time		$t_{d(on)}$	I_D=5A , V_{GS}=10V R_L= 6Ω		-	15	-	ns
Rise Time		t_r			-	55	-	ns
Turn-Off Delay Time		$t_{d(off)}$			-	100	-	ns
Fall Time		t_f			-	60	-	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F= 10A , V_{GS}=0		-	1.0	-	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F= 10A , V_{GS}=0 dI_F/dt=100A/μs		-	450	-	ns

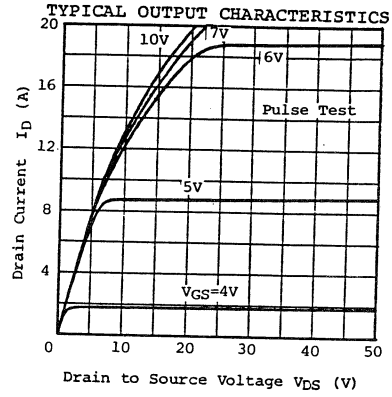
*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

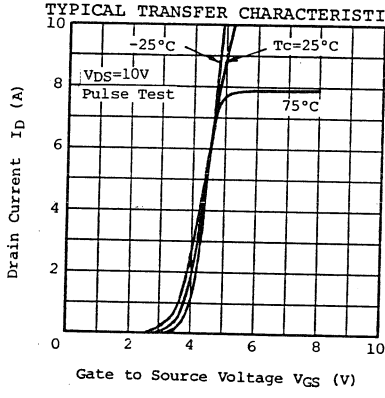
MAXIMUM SAFE OPERATION AREA



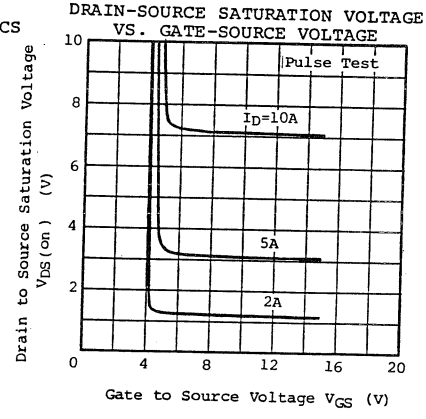
TYPICAL OUTPUT CHARACTERISTICS



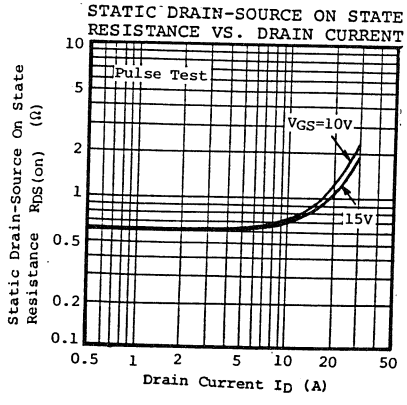
TYPICAL TRANSFER CHARACTERISTICS



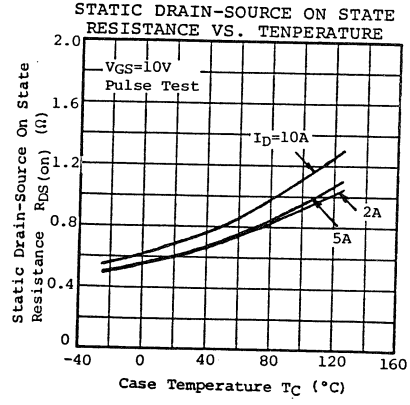
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



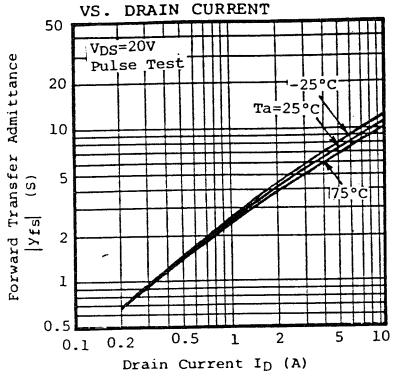
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



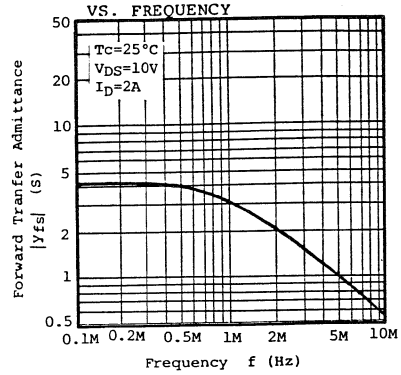
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



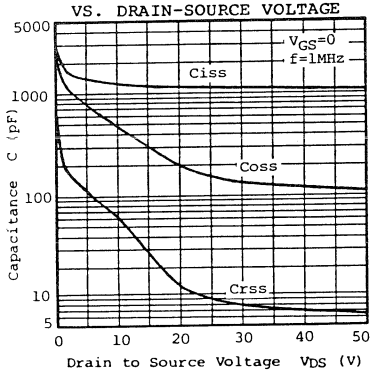
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



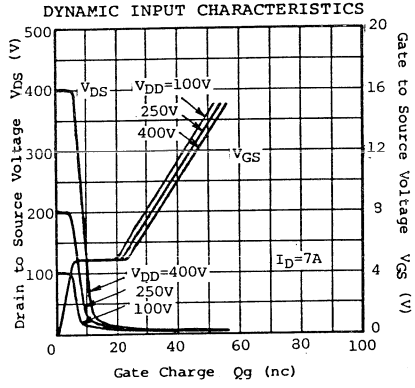
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



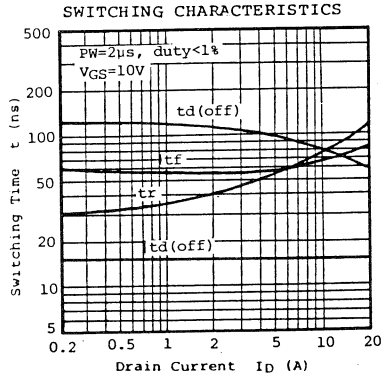
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



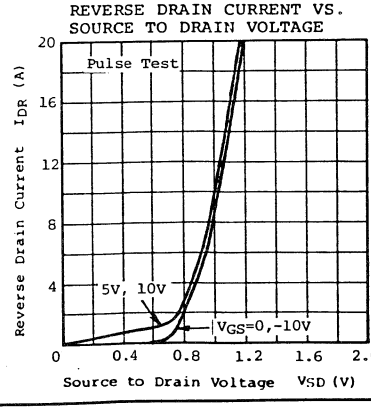
DYNAMIC INPUT CHARACTERISTICS



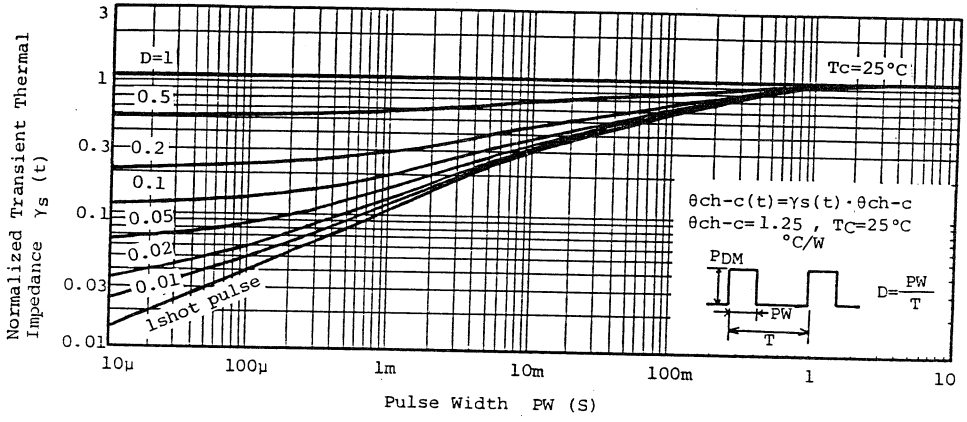
SWITCHING CHARACTERISTICS



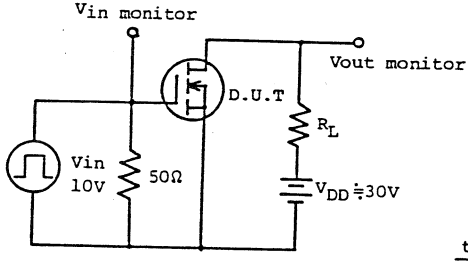
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



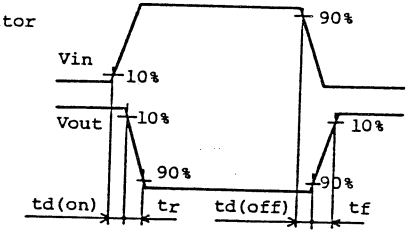
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



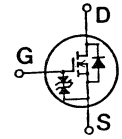
Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

POWER MOS FET DII-F SERIES

2SK682, 2SK683

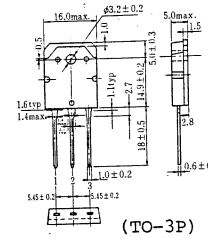
SILICON N-CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls, and Ultrasonic Power Oscillators.



1. Gate
2. Drain (Flange)
3. Sourece

(Dimensions in mm)

(TO-3P)

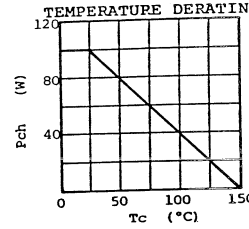
■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	2SK682	2SK683	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	12		A
Drain Peak Current	$I_{D(pulse)}$*	48		A
Body-Drain Diode Reverse Drain Current	I_{DR}	12		A
Channel Dissipation	Pch**	100		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	-55 ~ +150		°C

*PW≤10μs, duty cycle≤1%

**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING

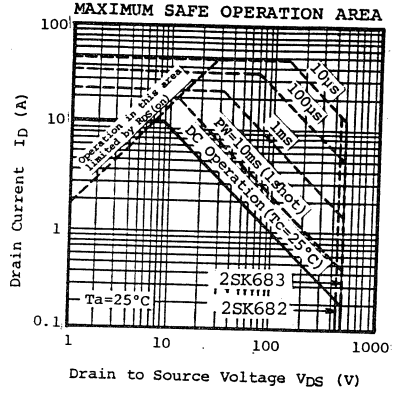


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

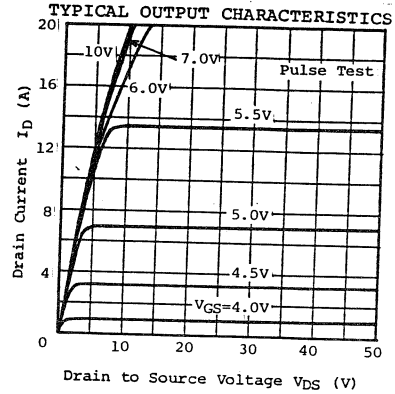
Item		Symbol	Test Condition		min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK682	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0		450	-	-	V
	2SK683				500	-	-	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0		±20	-	-	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±16V, V_{DS}=0		-	-	±10	μA
Zero Gate Voltage Drain Current	2SK682	I_{DSS}	V_{DS}=360V, V_{GS}=0		-	-	250	μA
	2SK683		V_{DS}=400V, V_{GS}=0					
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V		2.0	-	4.0	V
Static Drain-Source on State Resistance	2SK682	$R_{DS(on)}$	I_D=6A, V_{GS}=10V	*	-	0.4	0.55	Ω
	2SK683				-	0.45	0.60	
Foward Transfer Admittance		$\|Yfs\|$	I_D=6A, V_{DS}=10V	*	6	10	-	S
Input Capacitance		Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz		-	2050	-	pF
Output Capacitance		Coss			-	720	-	pF
Reverse Transfer Capacitance		Crss			-	80	-	pF
Turn-On Delay Time		$t_{d(on)}$	I_D=6A, V_{GS}=10V R_L=5Ω		-	25	-	ns
Rise Time		t_r			-	85	-	ns
Turn-Off Delay Time		$t_{d(off)}$			-	145	-	ns
Fall Time		t_f			-	85	-	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=12A, V_{GS}=0		-	1.0	-	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=12A, V_{GS}=0 dI_F/dt=100A/μs		-	120	-	ns

*Pulse Test

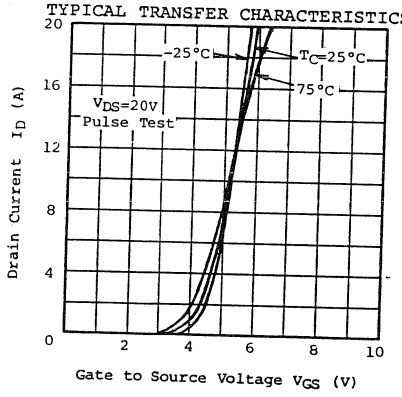
MAXIMUM SAFE OPERATION AREA



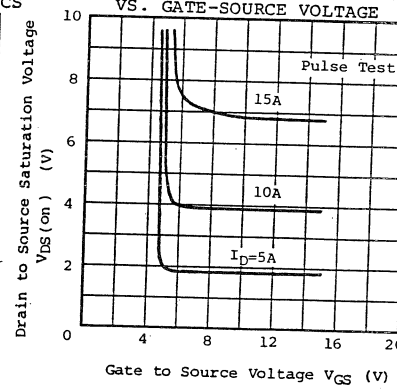
TYPICAL OUTPUT CHARACTERISTICS



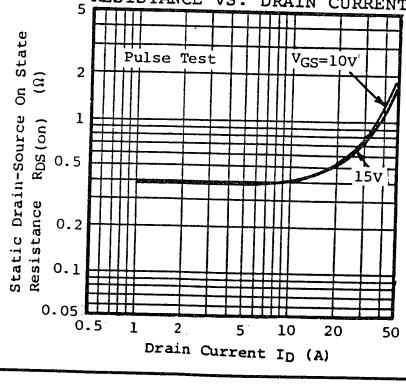
TYPICAL TRANSFER CHARACTERISTICS



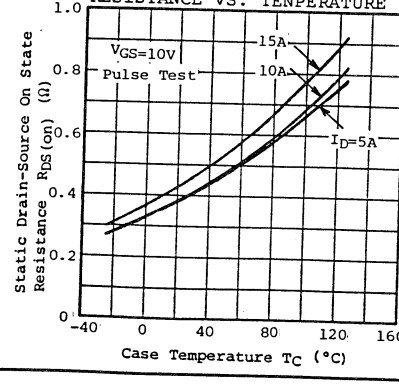
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



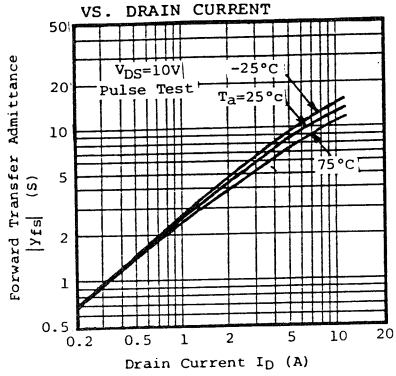
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



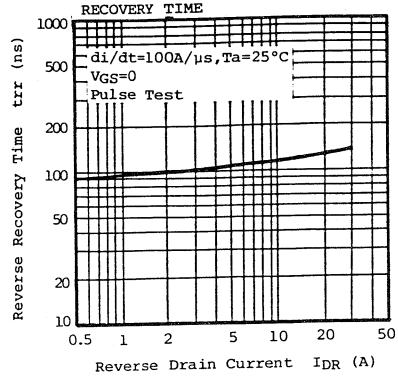
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



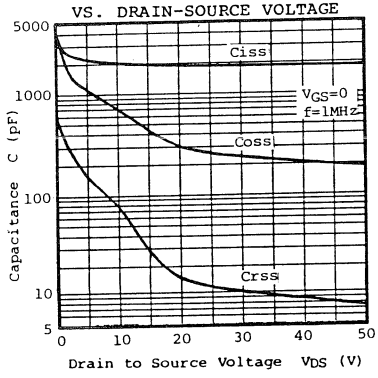
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



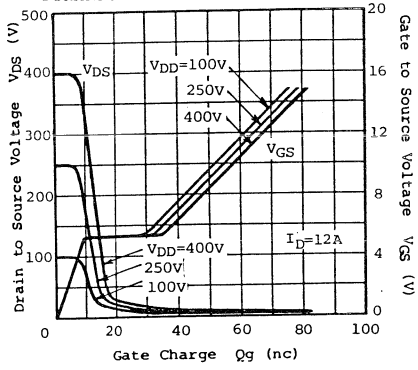
BODY DRAIN DIODE REVERSE RECOVERY TIME



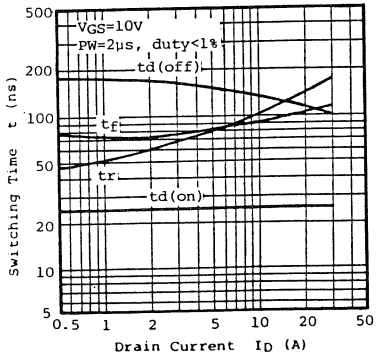
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



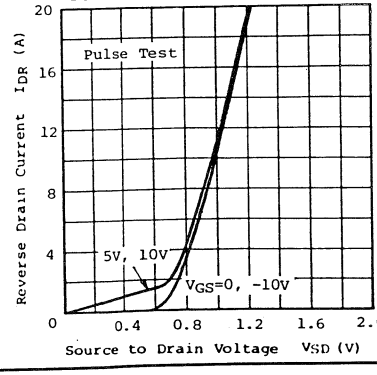
DYNAMIC INPUT CHARACTERISTICS



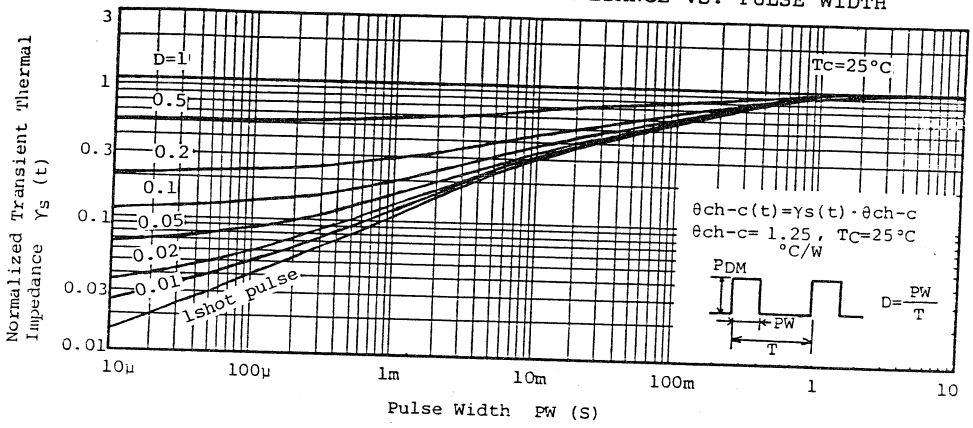
SWITCHING CHARACTERISTICS



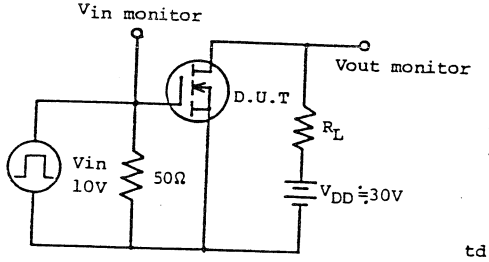
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



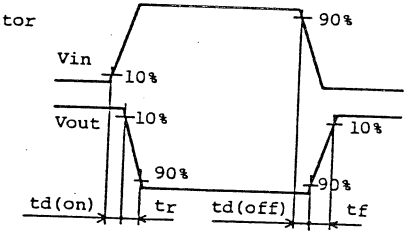
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

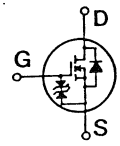
POWER MOS FET DII SERIES

2SK684

—Preliminary—

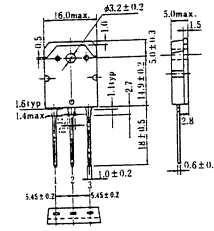
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

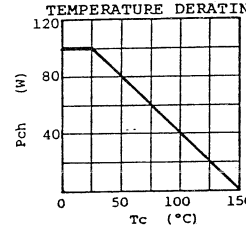
(TO-3P)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	800	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	7	A
Drain Peak Current	$I_{D(pulse)}$*	20	A
Body-Drain Diode Reverse Drain Current	I_{DR}	7	A
Channel Dissipation	Pch**	100	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55 ~ +150	°C

*PW≦10μs, duty≦1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



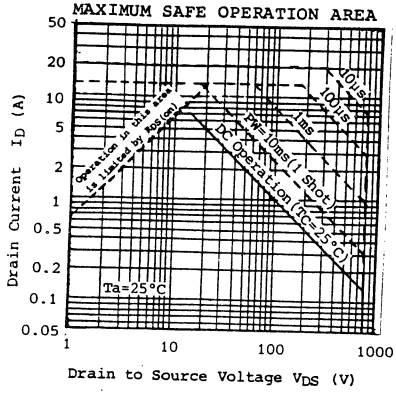
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	800	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=640V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=4A , V_{GS}=10V *	-	1.0	1.5	Ω
Foward Transfer Admittance	$\|yfs\|$	I_D=4A , V_{DS}=20V *	2.5	4.0	-	S
Input Capacitance	Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	1830	-	pF
Output Capacitance	Coss		-	1150	-	pF
Reverse Transfer Capacitance	Crss		-	730	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=4A , V_{GS}=10V R_L=7.5Ω	-	20	-	ns
Rise Time	t_r		-	230	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	220	-	ns
Fall Time	t_f		-	220	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=7A , V_{GS}=0	-	1.0	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=7A , V_{GS}=0 dI_F/dt=100A/μs	-	1000	-	ns

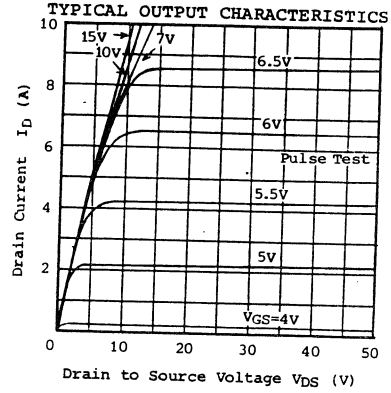
*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

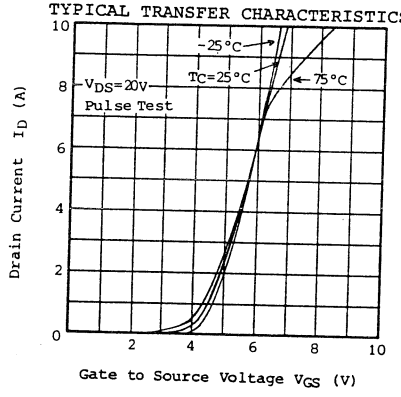
MAXIMUM SAFE OPERATION AREA



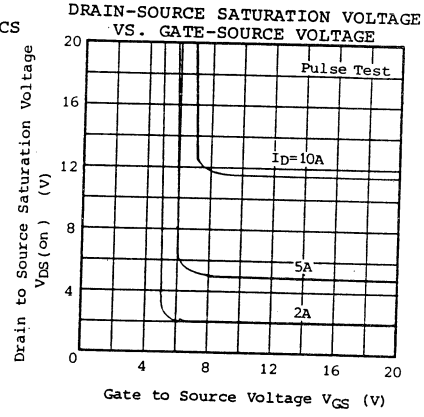
TYPICAL OUTPUT CHARACTERISTICS



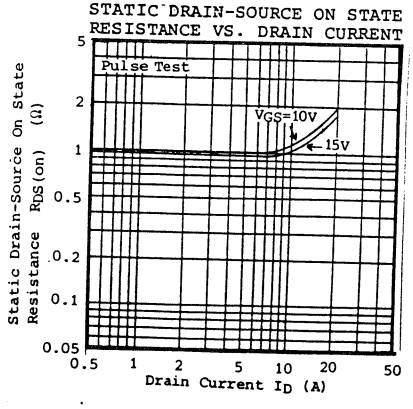
TYPICAL TRANSFER CHARACTERISTICS



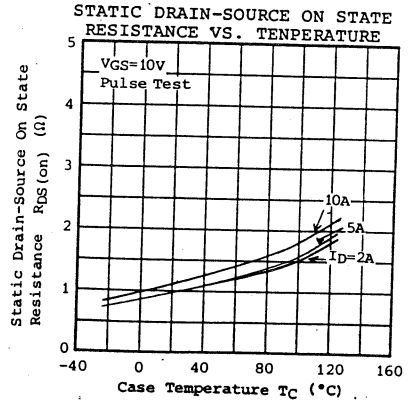
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



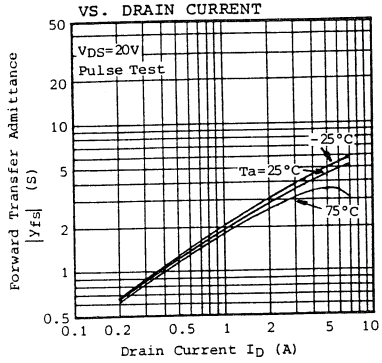
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



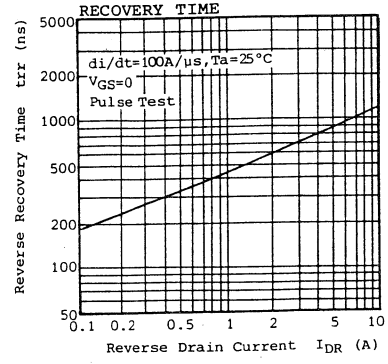
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



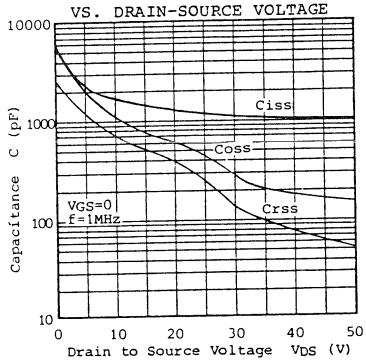
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



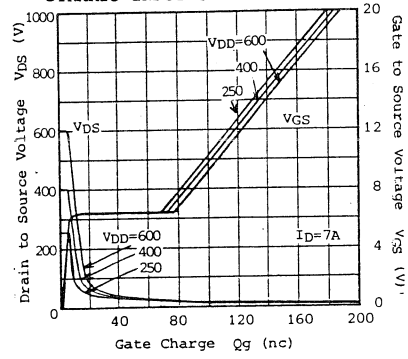
BODY DRAIN DIODE REVERSE RECOVERY TIME



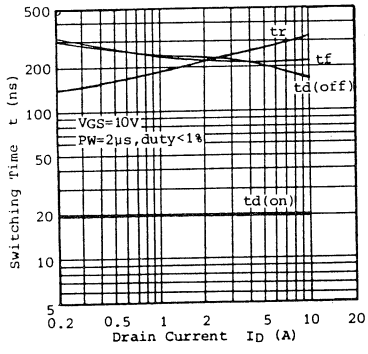
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



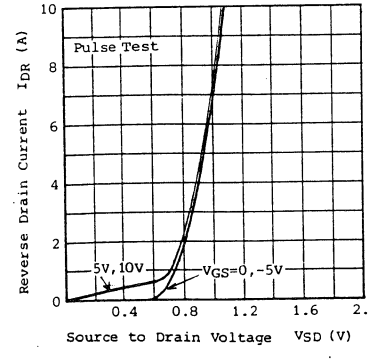
DYNAMIC INPUT CHARACTERISTICS



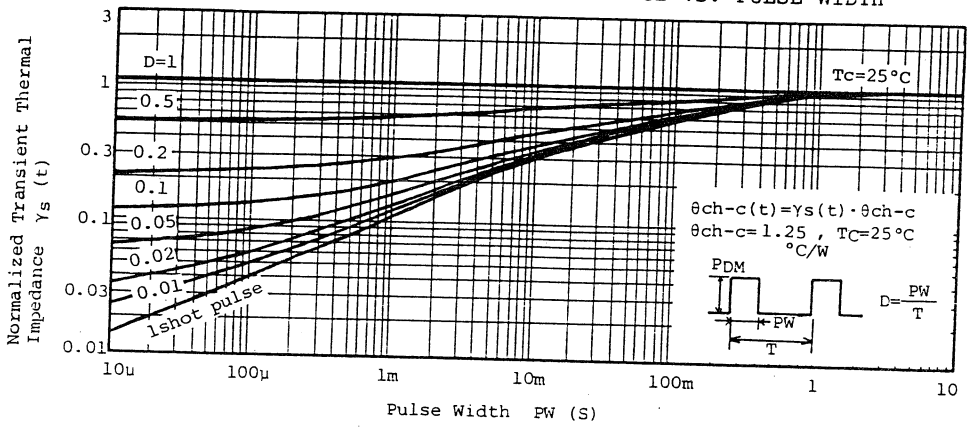
SWITCHING CHARACTERISTICS



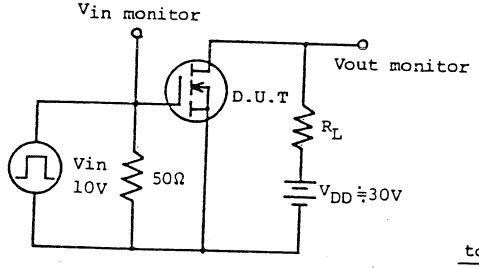
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



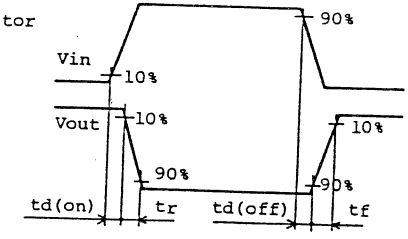
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

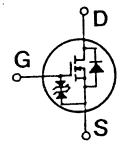
POWER MOS FET DⅢ-F SERIES

2SK685

—Preliminary—

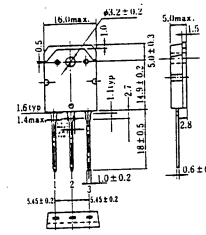
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

(TO-3P)

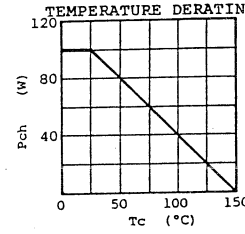
■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	1000	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	5	A
Drain Peak Current	$I_{D(pulse)}$*	15	A
Body-Drain Diode Reverse Drain Current	I_{DR}	5	A
Channel Dissipation	Pch**	100	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 ~ +150	°C

*PW≦10μs, duty≦1%

**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



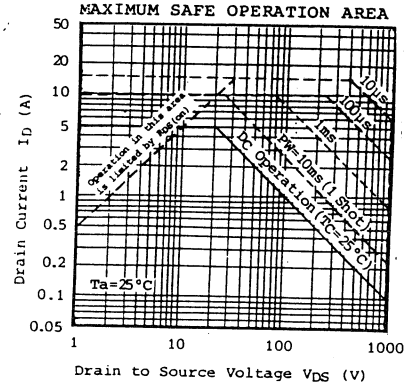
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	1000	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=± 16v, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=800V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D= 3A , V_{GS}=10V *	-	1.5	2.0	Ω
Foward Transfer Admittance	|yfs|	I_D=3A , V_{DS}=20V *	2.0	3.5	-	S
Input Capacitance	Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	1900	-	pF
Output Capacitance	Coss		-	1200	-	pF
Reverse Transfer Capacitance	Crss		-	760	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D= 3A , V_{GS}=10V R_L=10Ω	-	25	-	ns
Rise Time	t_r		-	240	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	220	-	ns
Fall Time	t_f		-	230	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=5A , V_{GS}=0	-	1.3	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=5A , V_{GS}=0 dI_F/dt=100A/μs	-	150	-	ns

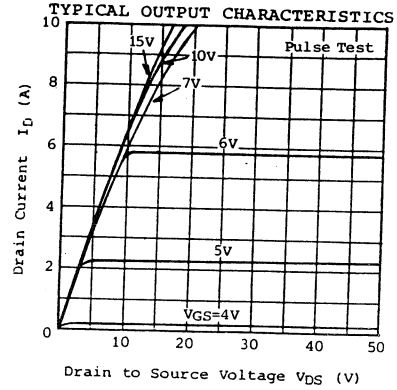
*Pulse Test

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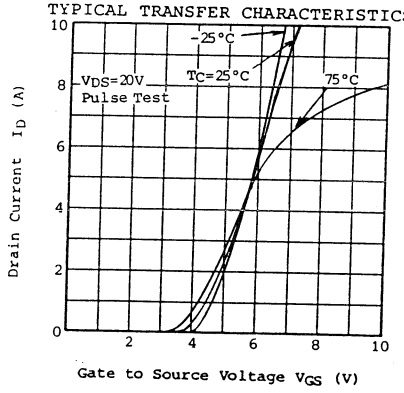
MAXIMUM SAFE OPERATION AREA



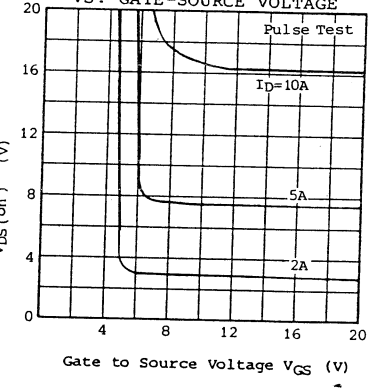
TYPICAL OUTPUT CHARACTERISTICS



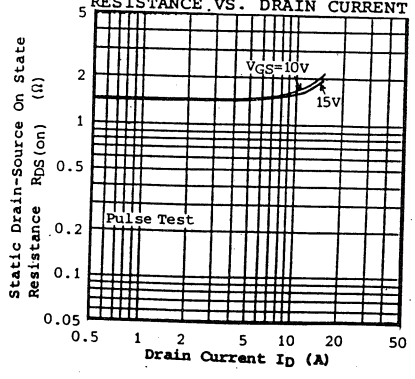
TYPICAL TRANSFER CHARACTERISTICS



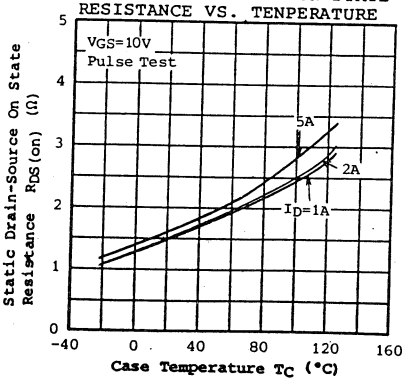
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



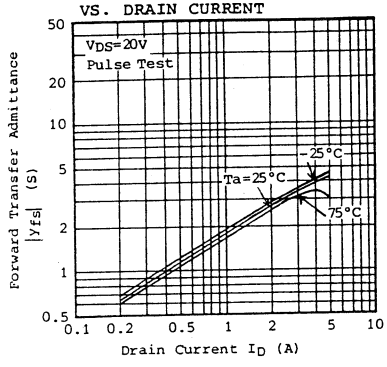
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



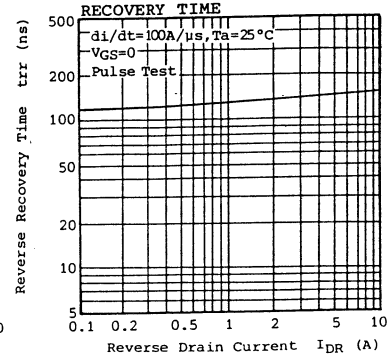
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



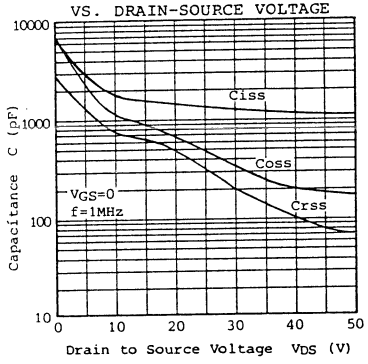
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



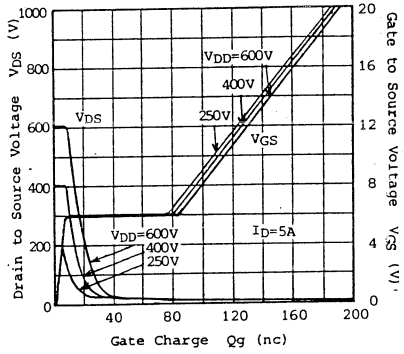
BODY DRAIN DIODE REVERSE RECOVERY TIME



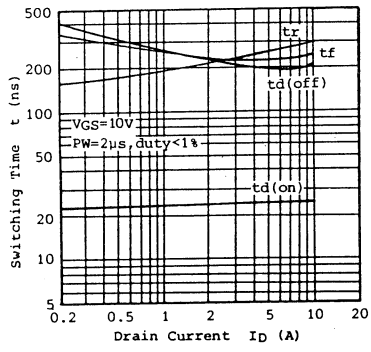
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



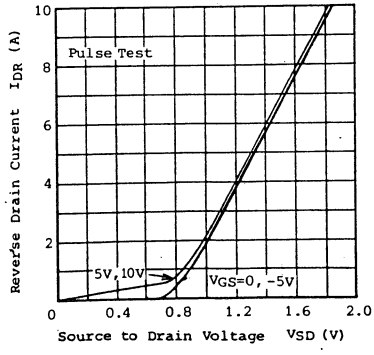
DYNAMIC INPUT CHARACTERISTICS



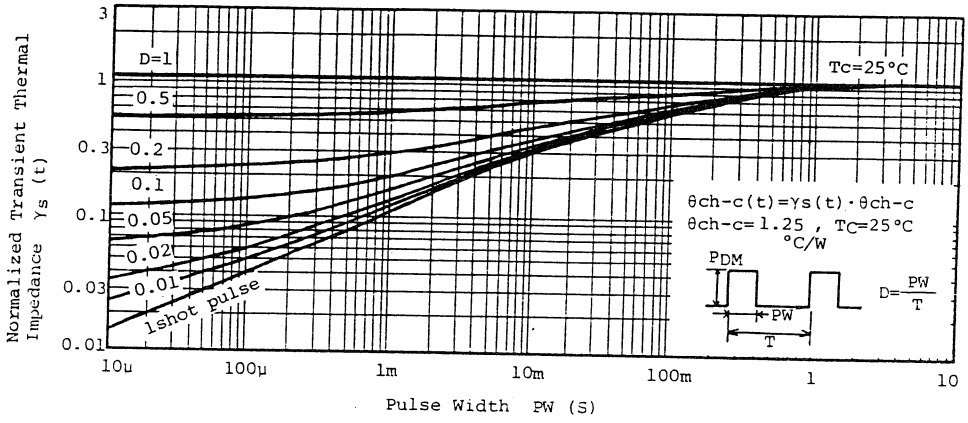
SWITCHING CHARACTERISTICS



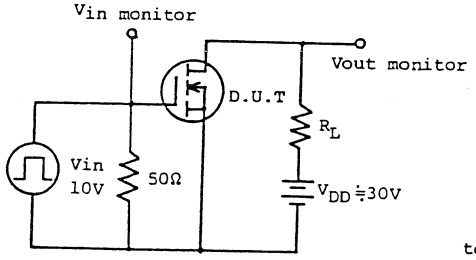
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



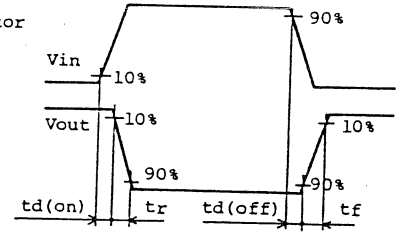
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

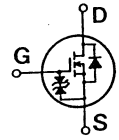
POWER MOS FET DII SERIES

2SK695

—Preliminary—

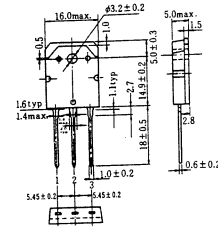
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls.

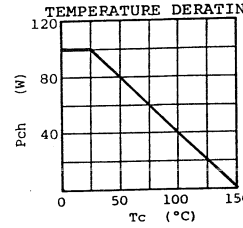


■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	800	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	5	A
Drain Peak Current	$I_{D(pulse)}$*	15	A
Body-Drain Diode Reverse Drain Current	I_{DR}	5	A
Channel Dissipation	Pch**	100	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 ~ +150	°C

*PW≤10μs, duty≤1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



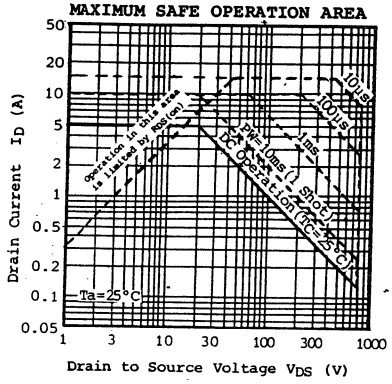
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	800	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=640V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=3A , V_{GS}=10V *	-	2.0	3.0	Ω
Foward Transfer Admittance	$\|yfs\|$	I_D=3A , V_{DS}=20V *	1.5	2.5	-	S
Input Capacitance	Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	1150	-	pF
Output Capacitance	Coss		-	610	-	pF
Reverse Transfer Capacitance	Crss		-	420	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=3A , V_{GS}=10V R_L=10Ω	-	20	-	ns
Rise Time	t_r		-	155	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	120	-	ns
Fall Time	t_f		-	120	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=5A , V_{GS}=0	-	1.0	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=5A , V_{GS}=0 dIF/dt=100A/μs	-	800	-	ns

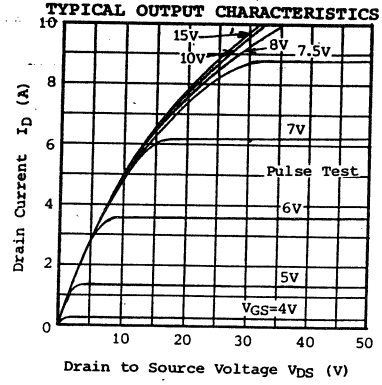
*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

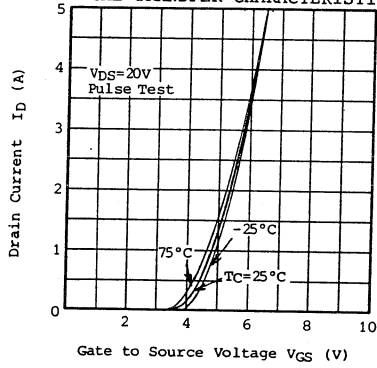
MAXIMUM SAFE OPERATION AREA



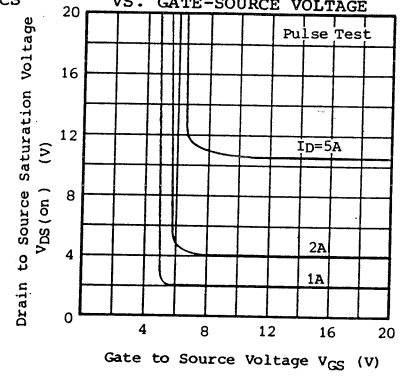
TYPICAL OUTPUT CHARACTERISTICS



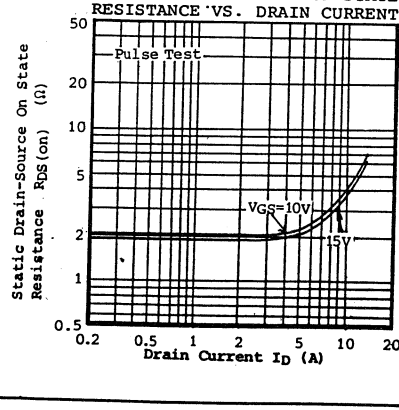
TYPICAL TRANSFER CHARACTERISTICS



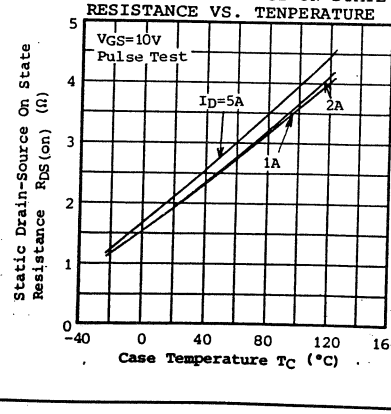
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



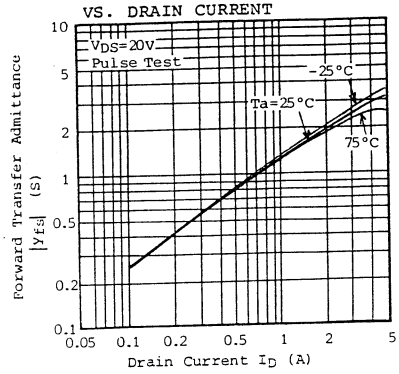
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



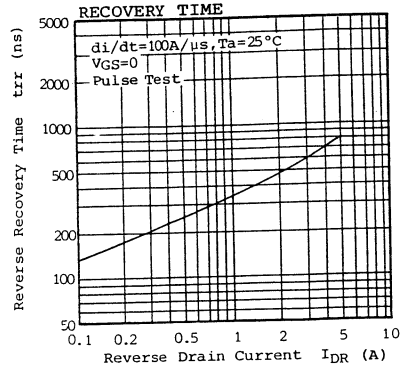
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



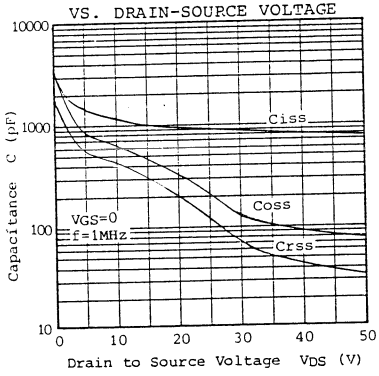
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



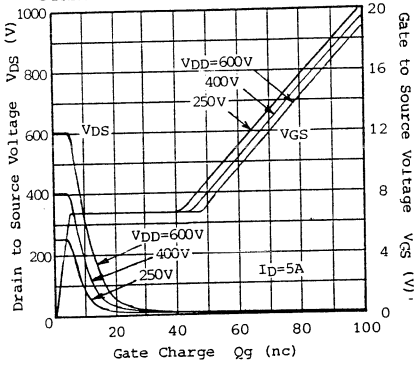
BODY DRAIN DIODE REVERSE RECOVERY TIME



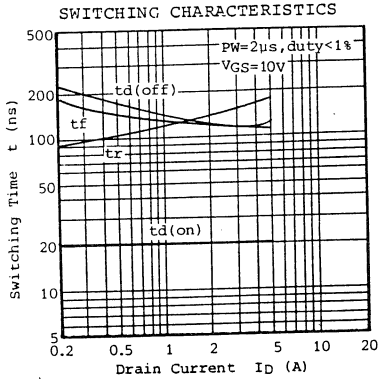
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



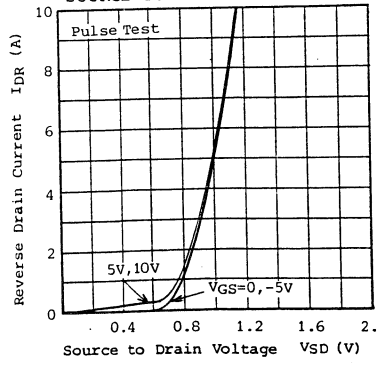
DYNAMIC INPUT CHARACTERISTICS



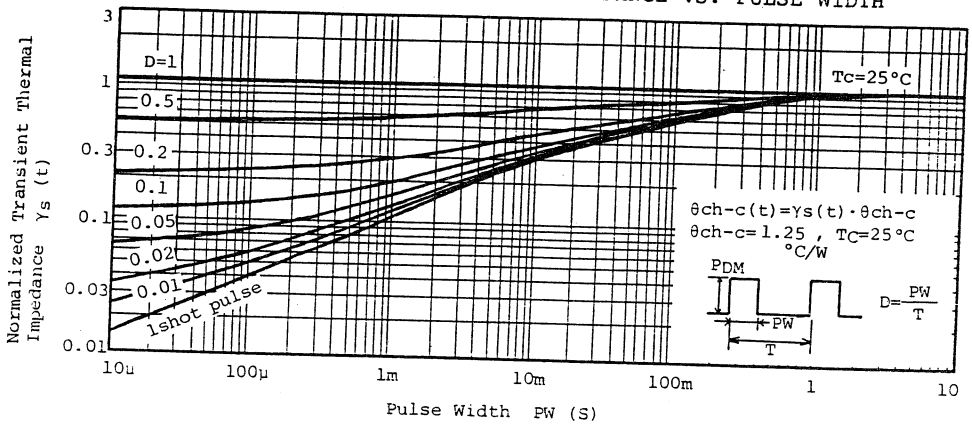
SWITCHING CHARACTERISTICS



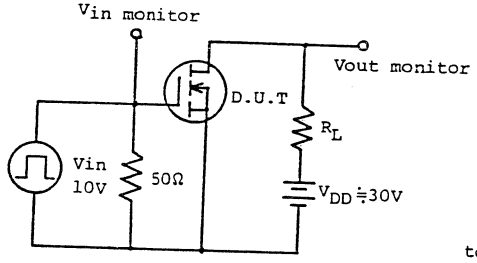
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



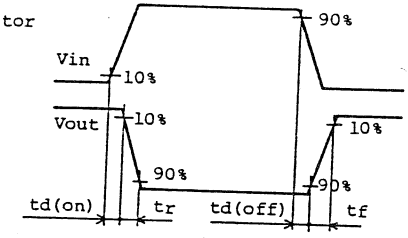
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

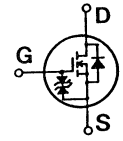
POWER MOS FET DII SERIES

2SK696

—Preliminary—

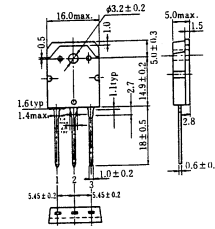
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

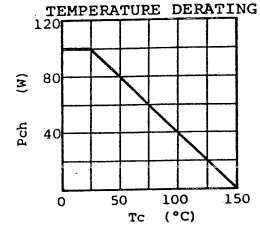
(TO-3P)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	1000	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	3	A
Drain Peak Current	$I_{D(pulse)}$*	10	A
Body-Drain Diode Reverse Drain Current	I_{DR}	3	A
Channel Dissipation	Pch **	100	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55 ~ +150	°C

*PW≤10μs, duty≤1%　　** Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



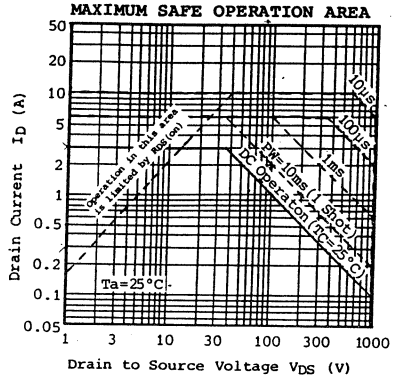
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D= 10mA , V_{GS}=0	1000	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=800V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}= 10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=2A , V_{GS}=10V *	-	3.0	4.0	Ω
Foward Transfer Admittance	$\|Yfs\|$	I_D= 2A , V_{DS}= 20V *	1.2	2.4	-	S
Input Capacitance	Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	1170	-	pF
Output Capacitance	Coss		-	610	-	pF
Reverse Transfer Capacitance	Crss		-	420	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D= 2A , V_{GS}=10V R_L= 15Ω	-	20	-	ns
Rise Time	t_r		-	125	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	135	-	ns
Fall Time	t_f		-	115	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F= 3A , V_{GS}=0	-	0.9	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F= 3A , V_{GS}=0 dIF/dt=100A/μs	-	1000	-	ns

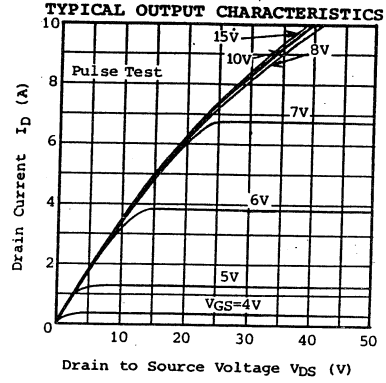
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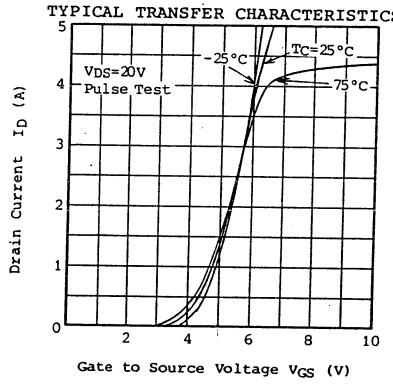
MAXIMUM SAFE OPERATION AREA



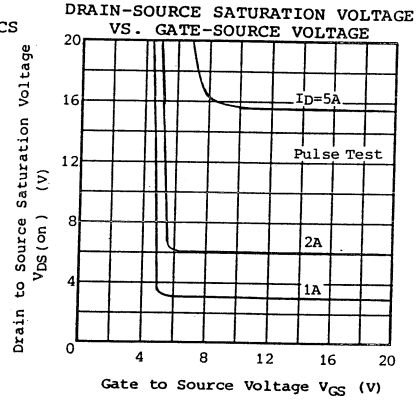
TYPICAL OUTPUT CHARACTERISTICS



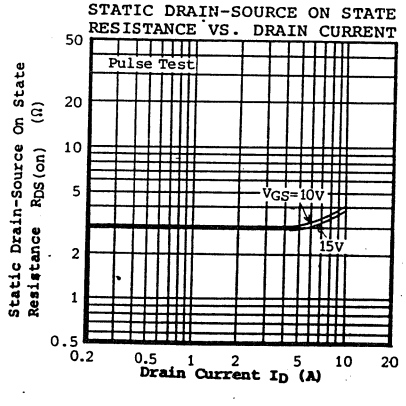
TYPICAL TRANSFER CHARACTERISTICS



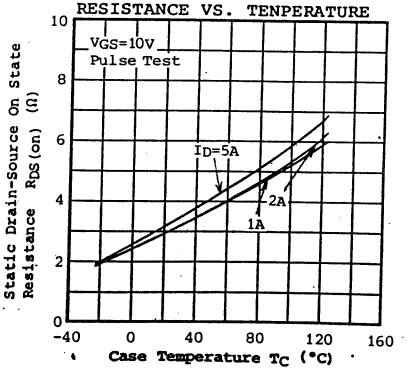
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



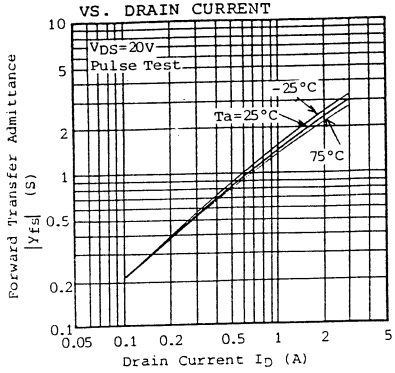
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



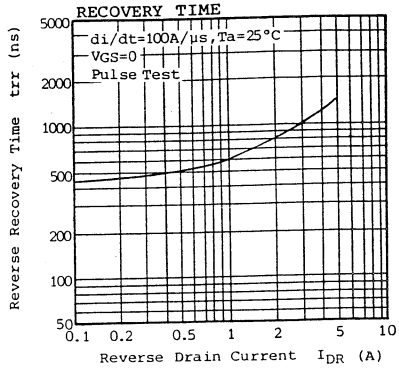
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



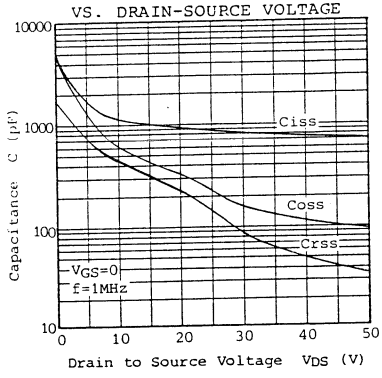
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



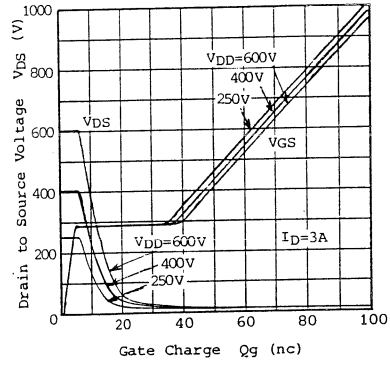
BODY DRAIN DIODE REVERSE RECOVERY TIME



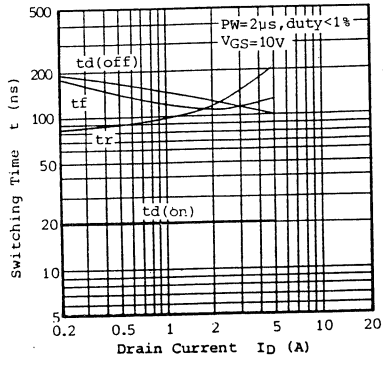
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



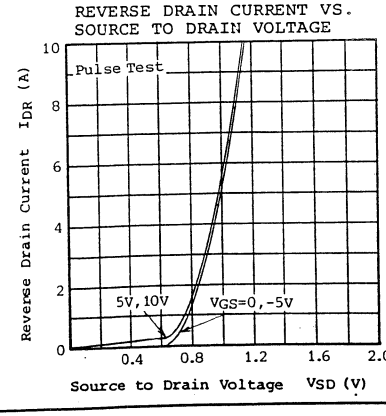
DYNAMIC INPUT CHARACTERISTICS



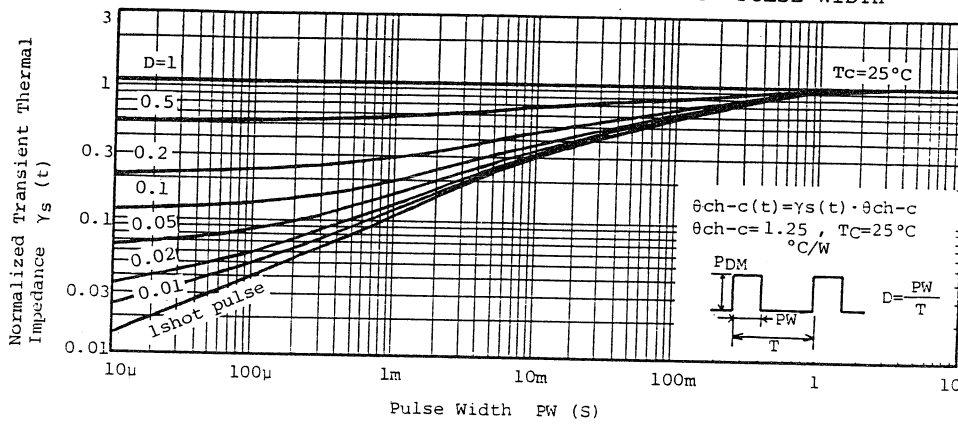
SWITCHING CHARACTERISTICS



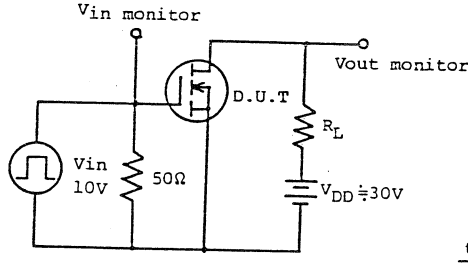
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



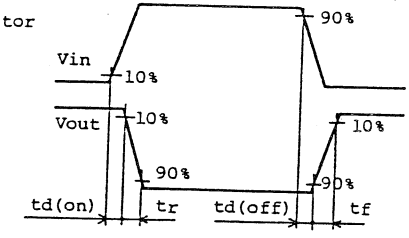
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

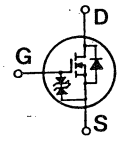
POWER MOS FET DII SERIES

2SK740

—Preliminary—

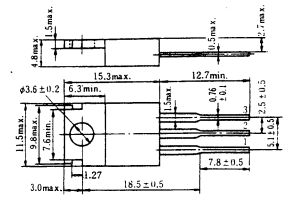
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

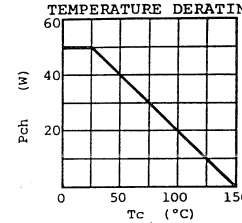
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	150	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	10	A
Drain Peak Current	$I_{D(pulse)}$*	40	A
Body-Drain Diode Reverse Drain Current	I_{DR}	10	A
Channel Dissipation	Pch**	50	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55 ~ +150	°C

*PW≤10μs, duty cycle≤1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



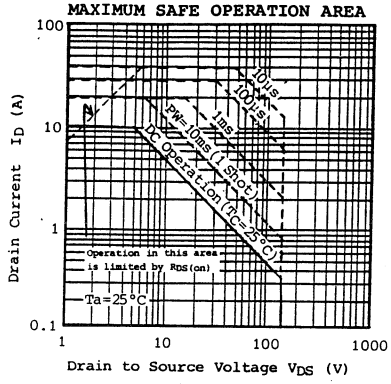
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	150	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=120V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=5A, V_{GS}=10V *	-	0.12	0.15	Ω
Foward Transfer Admittance	$\|yfs\|$	I_D=5A, V_{DS}=10V *	4.0	7.0	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz	-	1200	-	pF
Output Capacitance	Coss		-	550	-	pF
Reverse Transfer Capacitance	Crss		-	85	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=5A, V_{GS}=10V R_L=6Ω	-	20	-	ns
Rise Time	t_r		-	50	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	70	-	ns
Fall Time	t_f		-	40	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=10A, V_{GS}=0	-	1.2	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=10A, V_{GS}=0 dI_F/dt=50 A/μs	-	220	-	ns

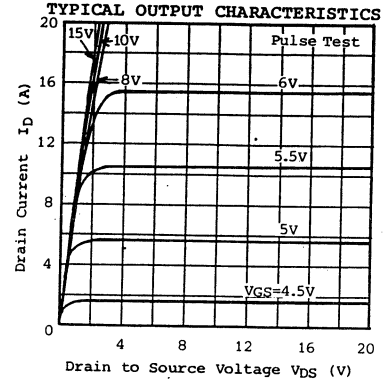
*Pulse Test

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

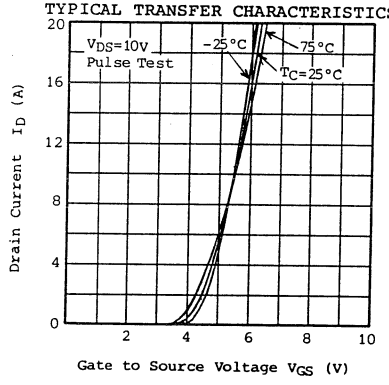
MAXIMUM SAFE OPERATION AREA



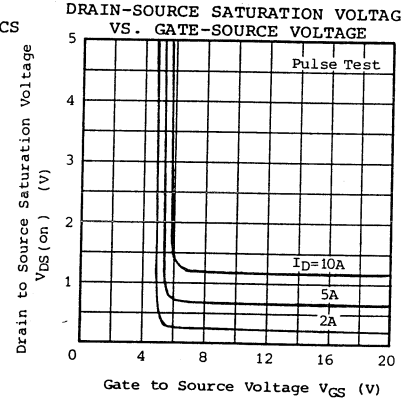
TYPICAL OUTPUT CHARACTERISTICS



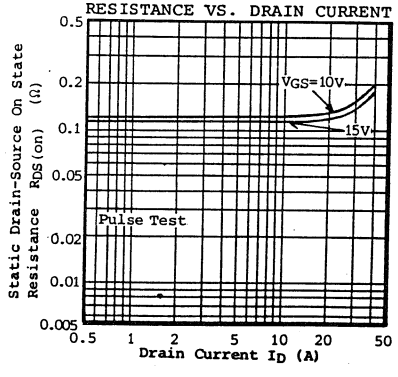
TYPICAL TRANSFER CHARACTERISTICS



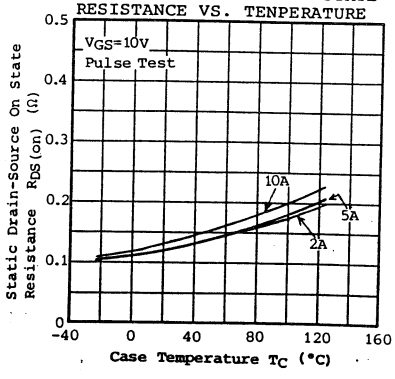
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



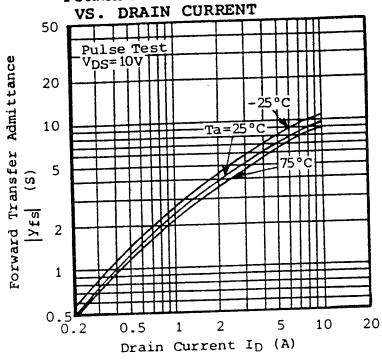
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



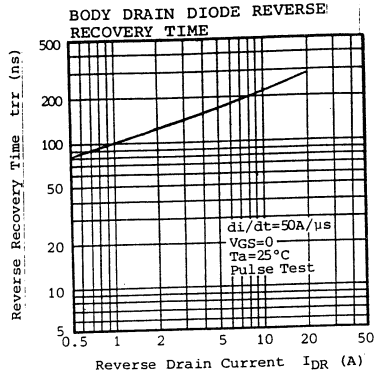
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



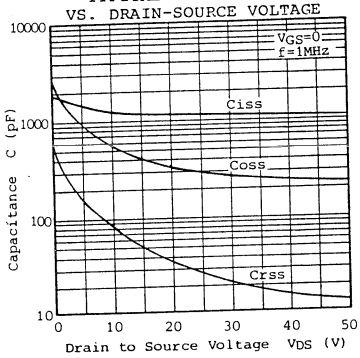
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



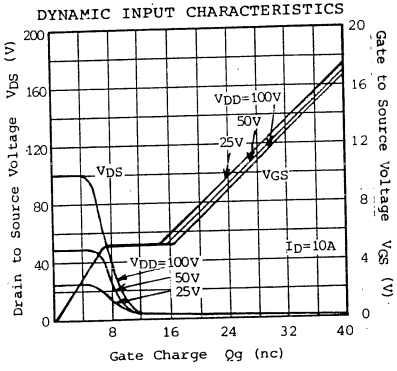
BODY DRAIN DIODE REVERSE RECOVERY TIME



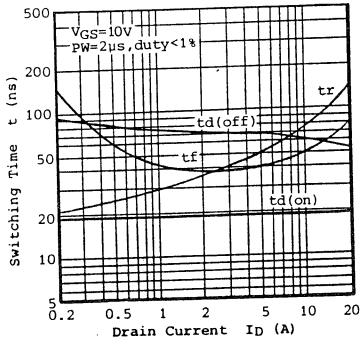
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



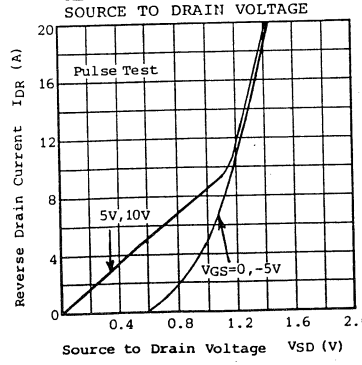
DYNAMIC INPUT CHARACTERISTICS



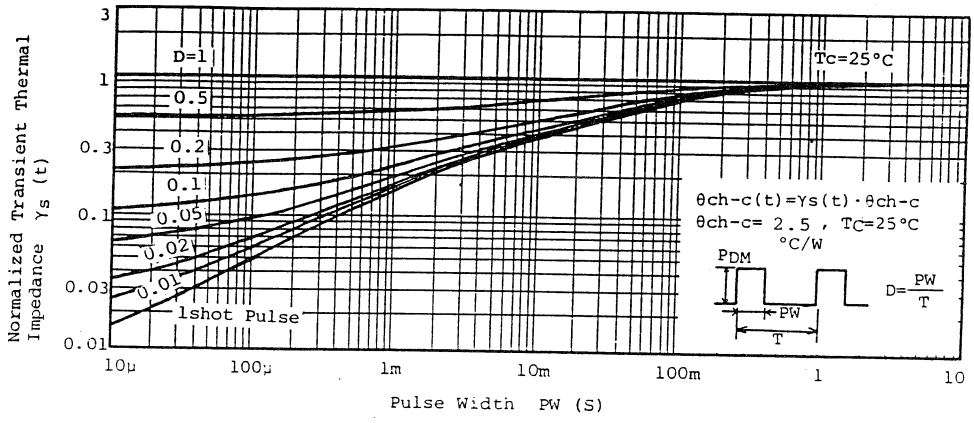
SWITCHING CHARACTERISTICS



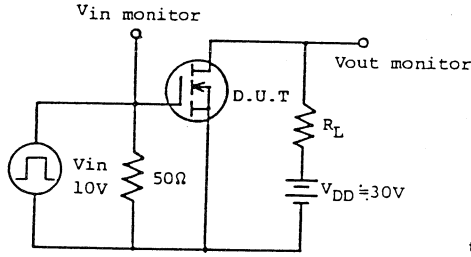
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



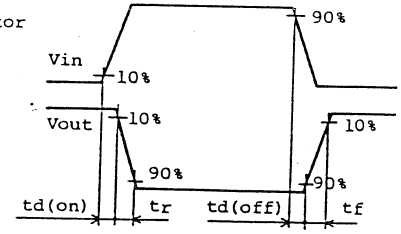
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

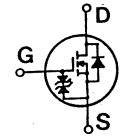
POWER MOS FET DII SERIES

2SK741

—Preliminary—

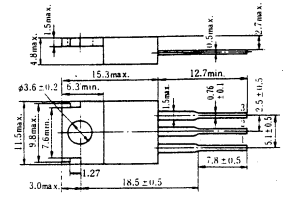
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter, Motor Controls.



(JEDEC TO-220AB)

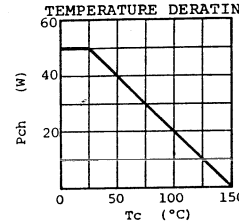
■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	250	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	7	A
Drain Peak Current	$I_{D(pulse)}$*	28	A
Body-Drain Diode Reverse Drain Current	I_{DR}	7	A
Channel Dissipation	Pch**	50	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 ~ +150	°C

*PW≦10μs, duty cycle≦1%

**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



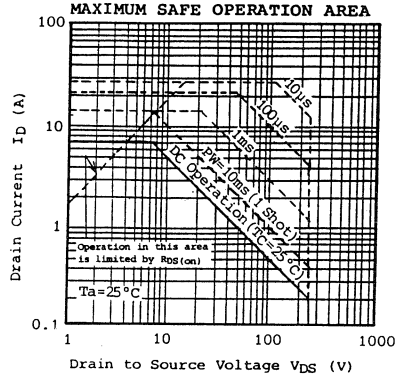
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	250	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=200V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=4A, V_{GS}=10V *	-	0.40	0.55	Ω
Foward Transfer Admittance	$\|Yfs\|$	I_D=4A, V_{DS}=10V *	2.7	4.5	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz	-	820	-	pF
Output Capacitance	Coss		-	370	-	pF
Reverse Transfer Capacitance	Crss		-	115	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=4A, V_{GS}=10V R_L=7.5Ω	-	12	-	ns
Rise Time	t_r		-	48	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	70	-	ns
Fall Time	t_f		-	50	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=7A, V_{GS}=0	-	1.2	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=7A, V_{GS}=0 dI_F/dt=50 A/μs	-	400	-	ns

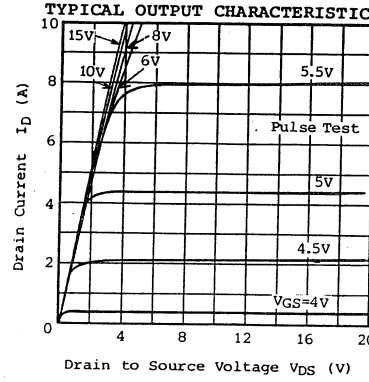
*Pulse Test

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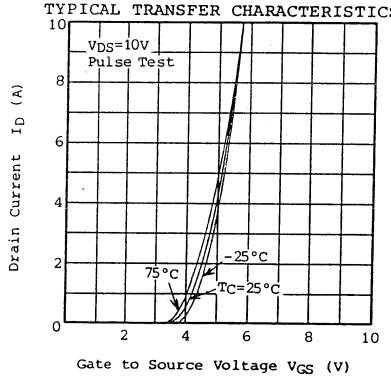
MAXIMUM SAFE OPERATION AREA



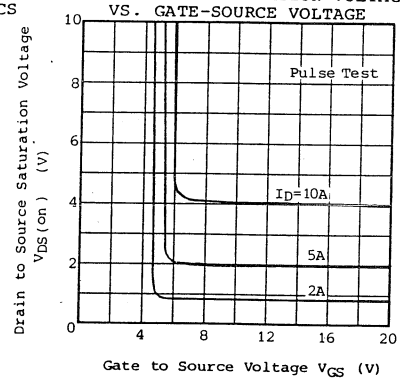
TYPICAL OUTPUT CHARACTERISTICS



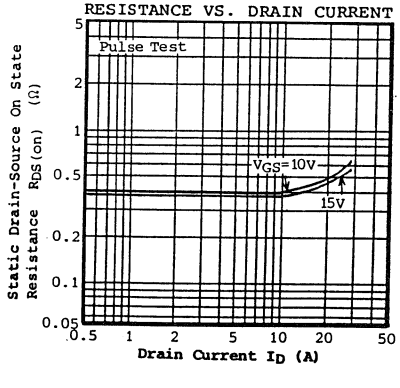
TYPICAL TRANSFER CHARACTERISTICS



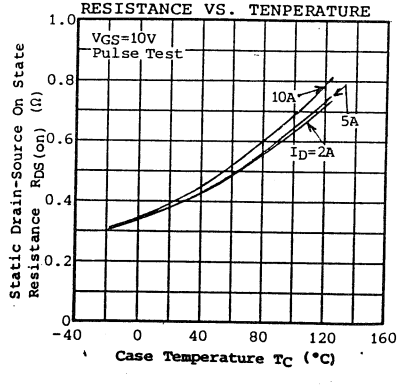
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



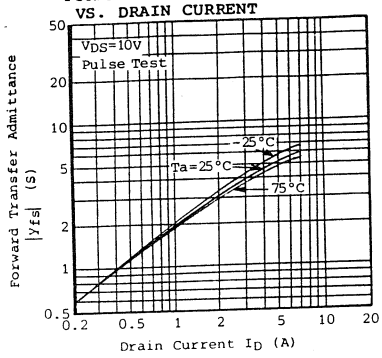
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



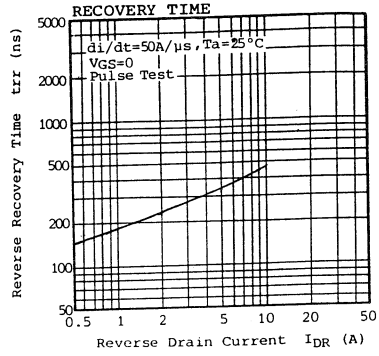
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



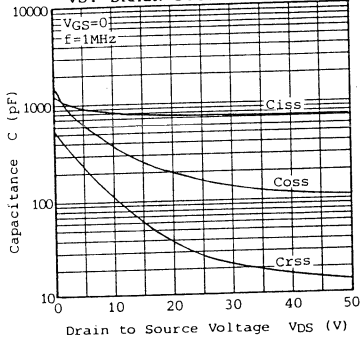
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



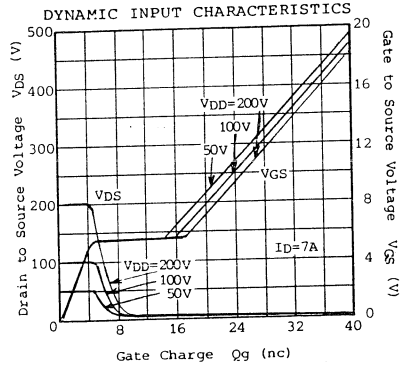
BODY DRAIN DIODE REVERSE RECOVERY TIME



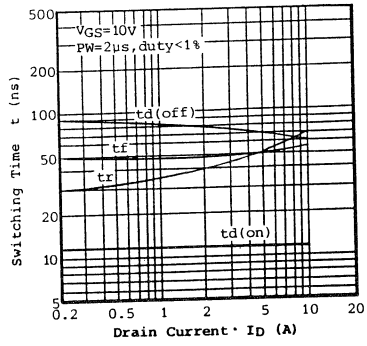
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



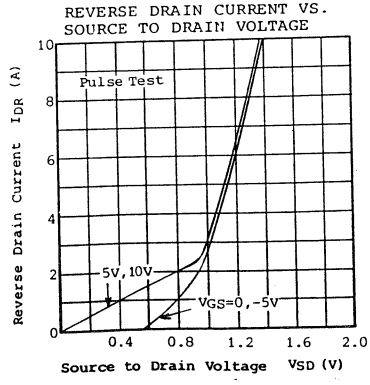
DYNAMIC INPUT CHARACTERISTICS



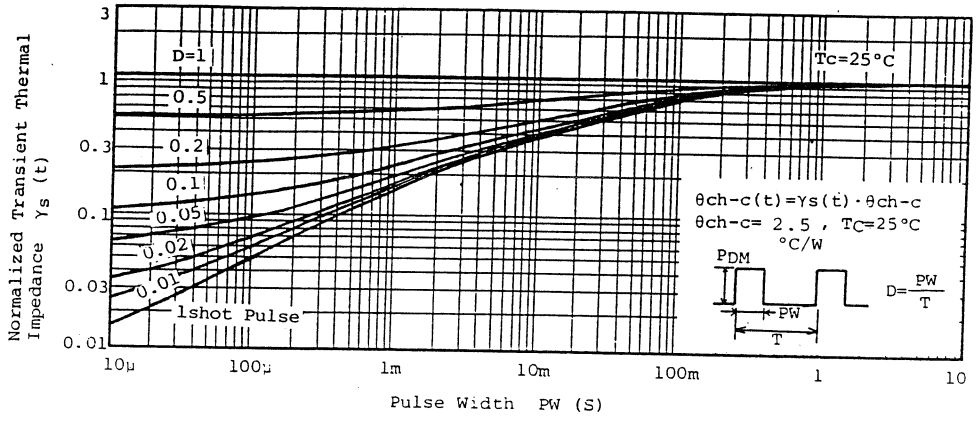
SWITCHING CHARACTERISTICS



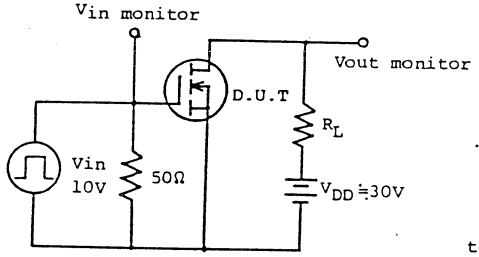
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



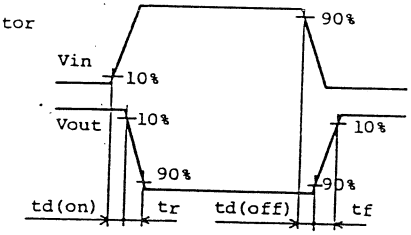
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



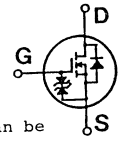
Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

POWER MOS FET DⅢ SERIES

2SK970 —Preliminary—

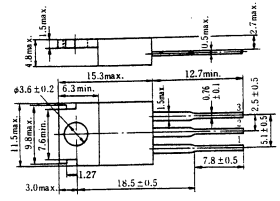
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- 4V Gate Drive Device Can be Driven From 5V Source.
- Suitable for DC-DC Convertor, Motor Drive, Power Switch, Solenoid Drive.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

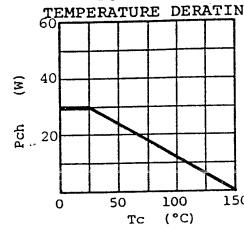
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	10	A
Drain Peak Current	$I_{D(pulse)}$*	40	A
Body-Drain Diode Reverse Drain Current	I_{DR}	10	A
Channel Dissipation	Pch**	30	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55 ~ +150	°C

*PW≤10μs, duty cycle≤1% ** Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



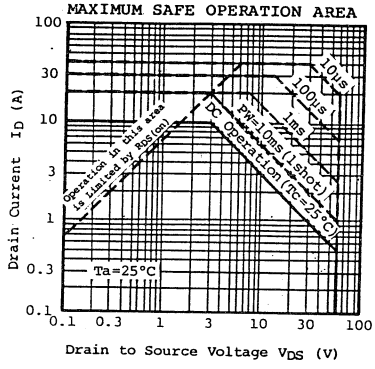
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D= 10mA , V_{GS}=0	60	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V , V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}= 10V	1.0	-	2.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=5A , V_{GS}=10V *	-	0.12	0.15	Ω
		I_D=5A , V_{GS}=4V *	-	0.17	0.22	Ω
Foward Transfer Admittance	|yfs|	I_D=5A , V_{DS}=10V *	3.5	6.0	-	S
Input Capacitance	Ciss	V_{DS}= 10 V, V_{GS}=0 f=1MHz	-	400	-	pF
Output Capacitance	Coss		-	220	-	pF
Reverse Transfer Capacitance	Crss		-	60	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D= 5A , V_{GS}= 10V R_L= 6Ω	-	5	-	ns
Rise Time	t_r		-	55	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	140	-	ns
Fall Time	t_f		-	90	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F= 10A , V_{GS}=0	-	1.2	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F= 10A , V_{GS}=0 dIF/dt= 50 A/μs	-	125	-	ns

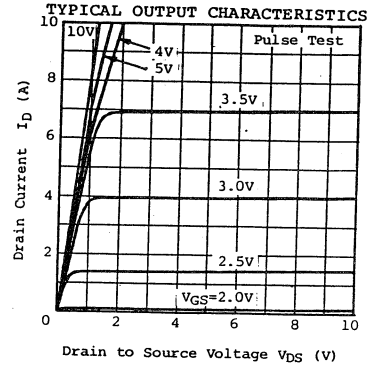
*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

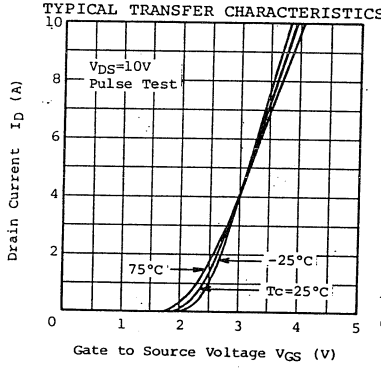
MAXIMUM SAFE OPERATION AREA



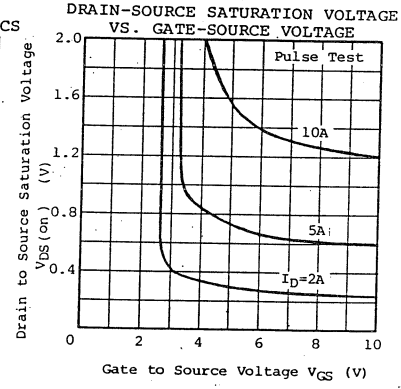
TYPICAL OUTPUT CHARACTERISTICS



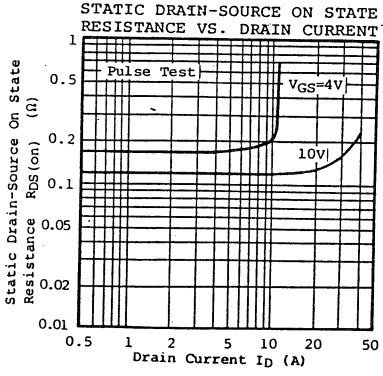
TYPICAL TRANSFER CHARACTERISTICS



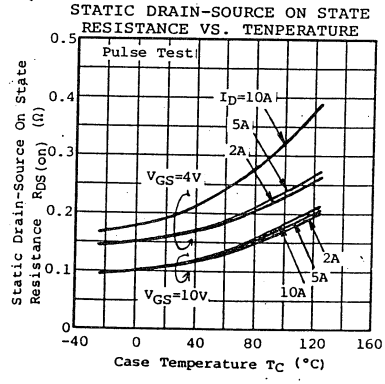
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



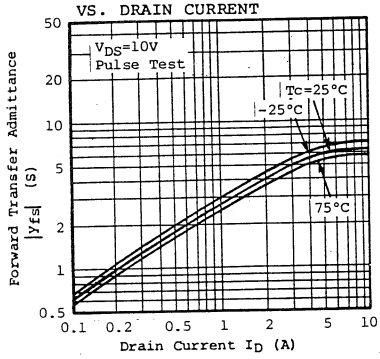
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



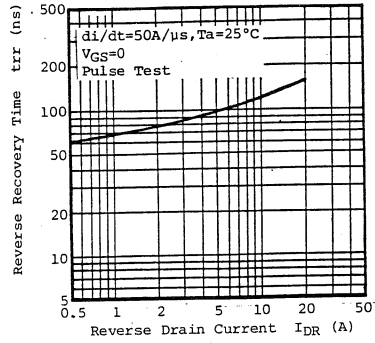
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



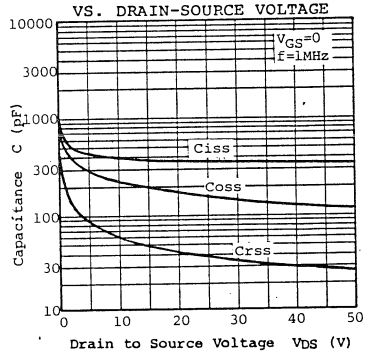
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



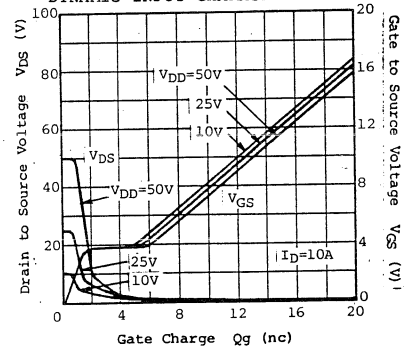
BODY-DRAIN DIODE REVERSE RECOVERY TIME



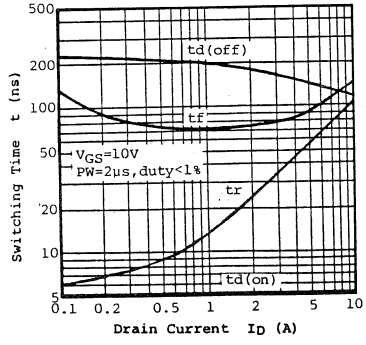
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



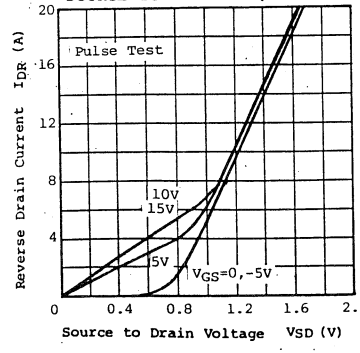
DYNAMIC INPUT CHARACTERISTICS



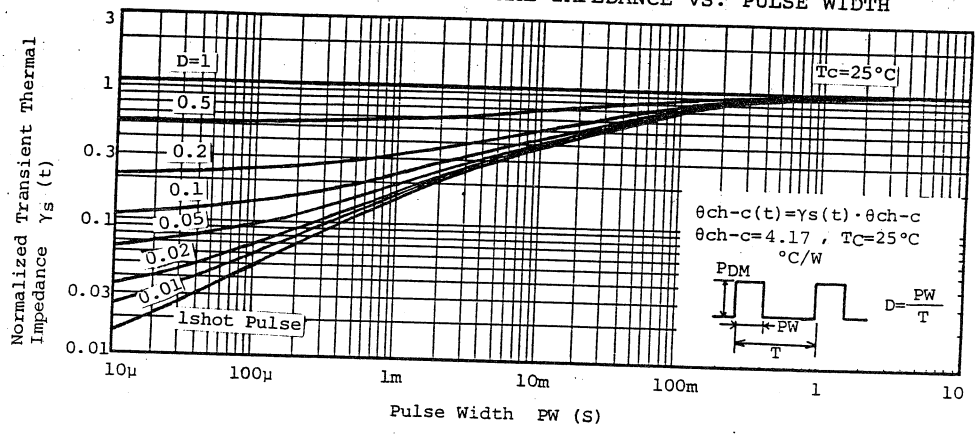
SWITCHING CHARACTERISTICS



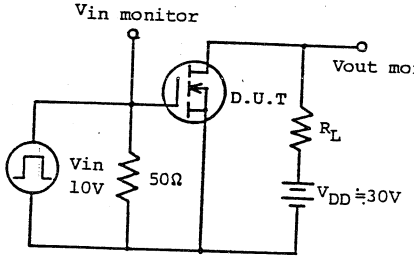
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



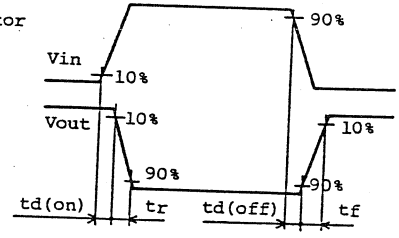
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



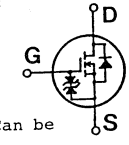
Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

POWER MOS FET DⅢ SERIES

2SK971 —Preliminary—

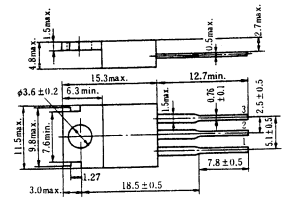
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- 4V Gate Drive Device Can be Driven From 5V Source.
- Suitable for DC-DC Convertor, Motor Drive, Power Switch, Solenoid Drive.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

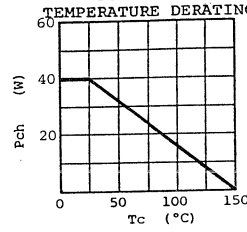
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	15	A
Drain Peak Current	$I_{D(pulse)}$*	60	A
Body-Drain Diode Reverse Drain Current	I_{DR}	15	A
Channel Dissipation	Pch**	40	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55 ~ +150	°C

*PW≤10μs, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING

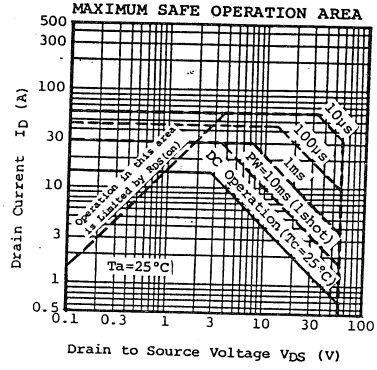


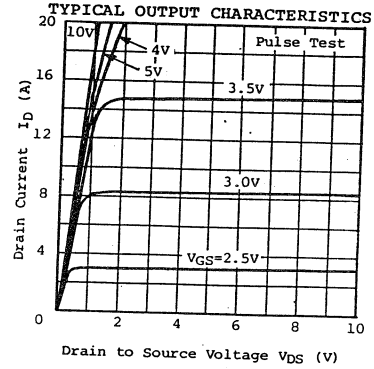
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

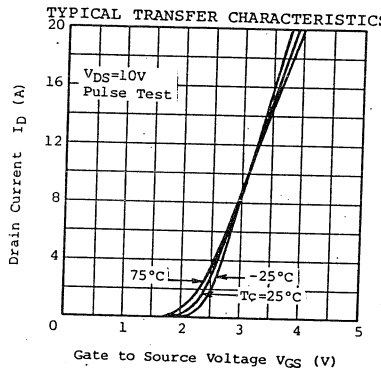
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	60	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V , V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	1.0	-	2.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=8A , V_{GS}=10V *	-	0.055	0.065	Ω
		I_D=8A , V_{GS}=4V *	-	0.075	0.095	
Foward Transfer Admittance	$\|yfs\|$	I_D=8A , V_{DS}=10V *	7	12	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz	-	860	-	pF
Output Capacitance	Coss		-	450	-	pF
Reverse Transfer Capacitance	Crss		-	140	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=8A , V_{GS}=10V R_L=3.75Ω	-	10	-	ns
Rise Time	t_r		-	70	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	180	-	ns
Fall Time	t_f		-	120	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=15A , V_{GS}=0	-	1.3	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=15A , V_{GS}=0 dI_F/dt=50A/μs	-	135	-	ns

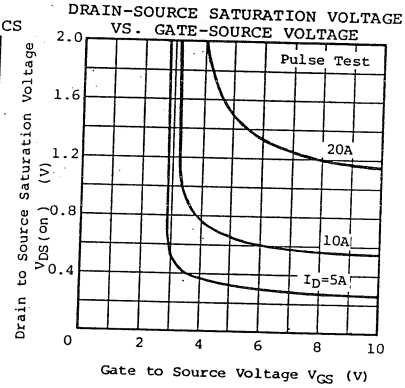
*Pulse Test

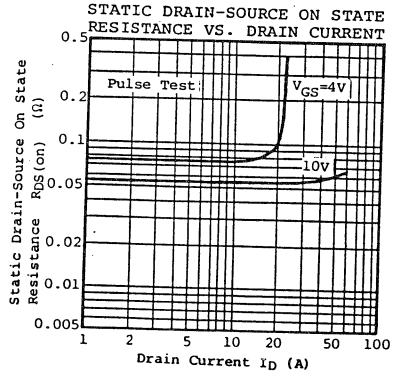
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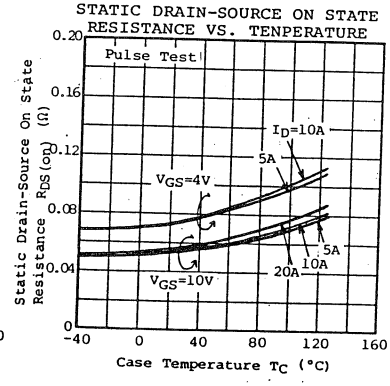

MAXIMUM SAFE OPERATION AREA
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
Operation is Limited by $R_{DS(on)}$
10μs
100μs
1ms
PW=10ms (1shot)
DC Operation (T_C=25°C)
Ta=25°C


TYPICAL OUTPUT CHARACTERISTICS
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
Pulse Test
10V
4V
5V
3.5V
3.0V
V_{GS}=2.5V

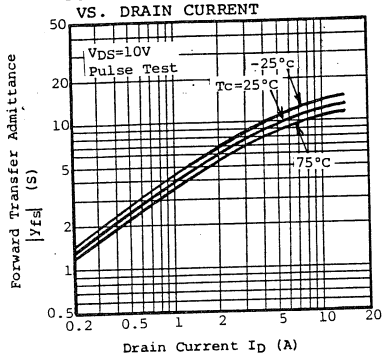

TYPICAL TRANSFER CHARACTERISTICS
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)
V_{DS}=10V
Pulse Test
75°C
-25°C
T_C=25°C


DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE
Drain to Source Saturation Voltage $V_{DS(on)}$ (V)
Gate to Source Voltage V_{GS} (V)
Pulse Test
20A
10A
I_D=5A

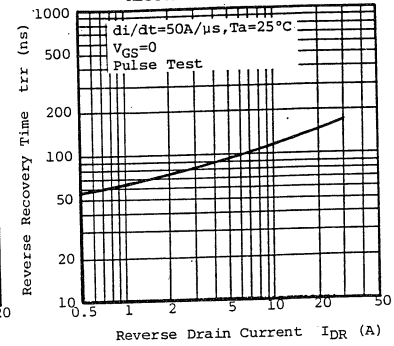

STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT
Static Drain-Source On State Resistance $R_{DS(on)}$ (Ω)
Drain Current I_D (A)
Pulse Test
V_{GS}=4V
10V


STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE
Static Drain-Source On State Resistance $R_{DS(on)}$ (Ω)
Case Temperature T_C (°C)
Pulse Test
I_D=10A
5A
V_{GS}=4V
5A
10A
20A
V_{GS}=10V

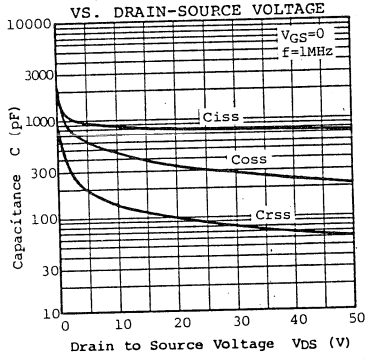
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



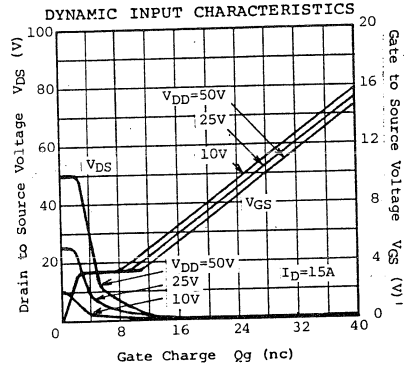
BODY-DRAIN DIODE REVERSE RECOVERY TIME



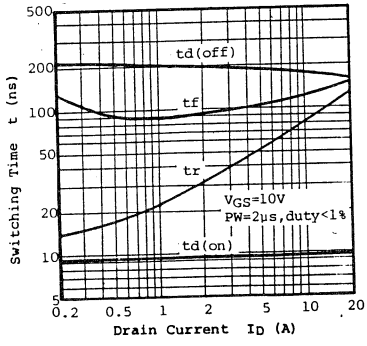
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



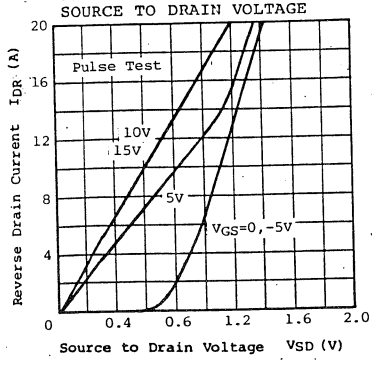
DYNAMIC INPUT CHARACTERISTICS



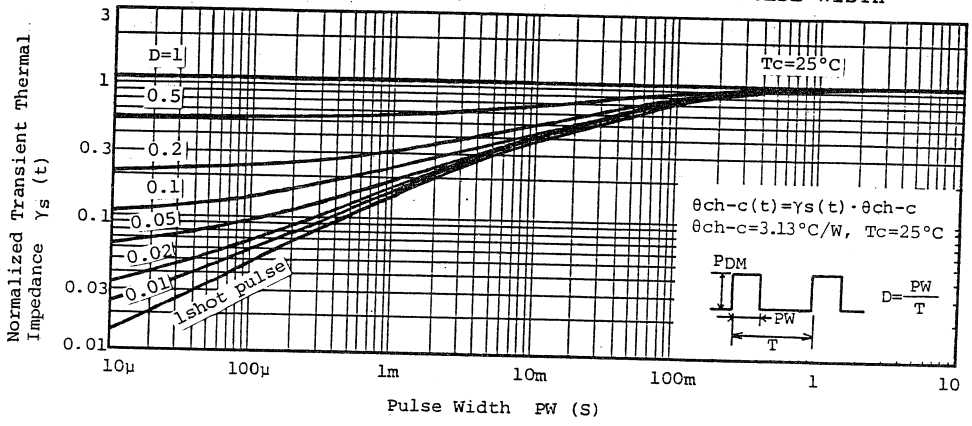
SWITCHING CHARACTERISTICS



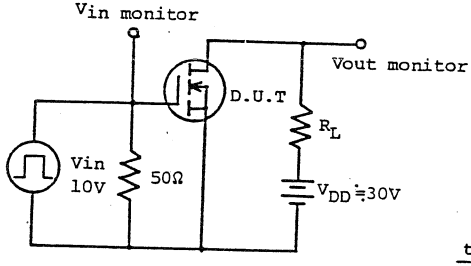
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



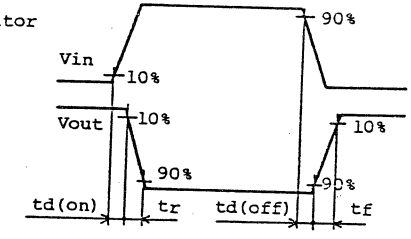
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



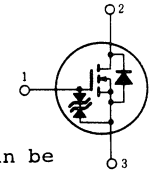
SWITCHING TIME TEST WAVEFORMS

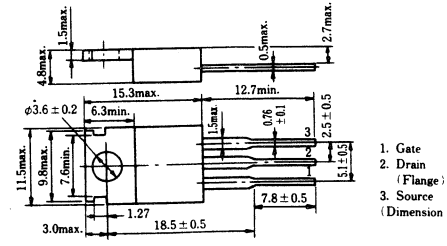


Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

2SK972

SILICON N-CHANNEL MOS FET





(JEDEC TO-220AB)

Features;

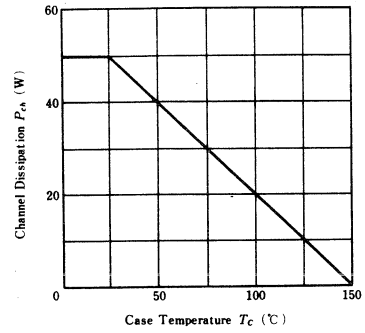
- Low On-Resistance.
- High Speed Switching.
- 4V Gate Drive Device Can be Driven From 5V Source.
- Suitable for DC-DC Convertor, Motor Drive, Power Switch, Solenoid Drive.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	25	A
Drain Peak Current	$I_{D(pulse)}$*	100	A
Body-Drain Diode Reverse Drain Current	I_{DR}	25	A
Channel Dissipation	P_{ch}**	50	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55~+150	°C

*PW≤10μs, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING

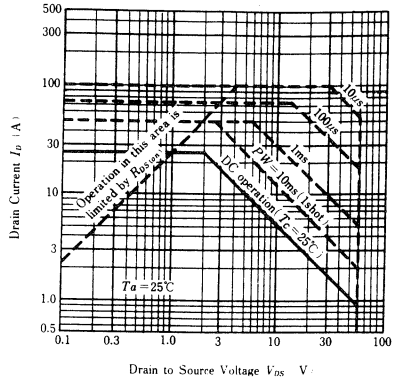


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

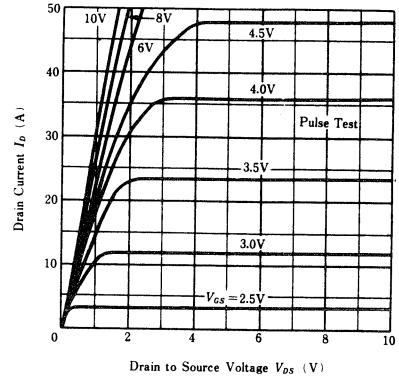
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	60	—	—	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	—	—	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V, V_{GS}=0	—	—	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	—	2.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=15A, V_{GS}=10V*	—	0.033	0.04	Ω
		I_D=15A, V_{GS}=4V*	—	0.05	0.06	
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=15A, V_{DS}=10V*	12	20	—	S
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	—	1400	—	pF
Output Capacitance	C_{oss}		—	720	—	pF
Reverse Transfer Capacitance	C_{rss}		—	220	—	pF
Turn-on Delay Time	$t_{d(on)}$	I_D=15A, V_{GS}=10V, R_L=2Ω	—	15	—	ns
Rise Time	t_r		—	130	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	270	—	ns
Fall Time	t_f		—	180	—	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=25A, V_{GS}=0	—	1.3	—	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=25A, V_{GS}=0 di_F/dt=50A/μs	—	135	—	ns

*Pulse Test

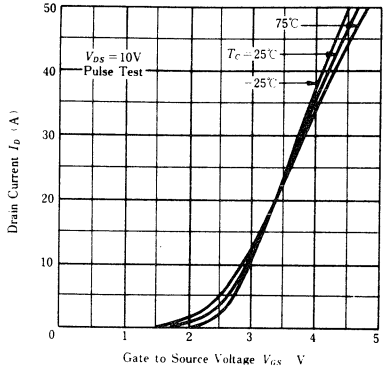
MAXIMUM SAFE OPERATION AREA



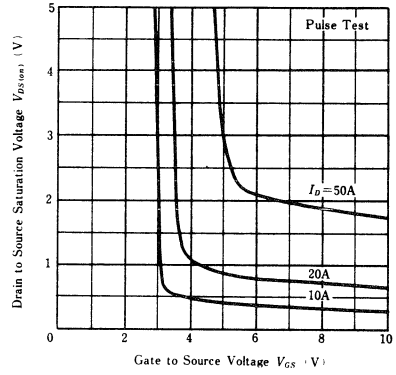
TYPICAL OUTPUT CHARACTERISTICS



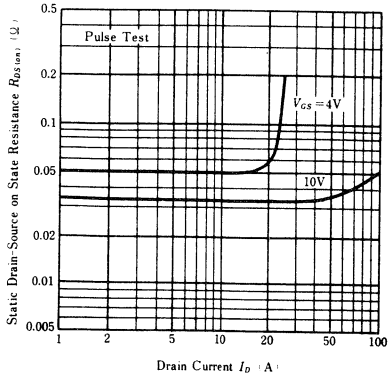
TYPICAL TRANSFER CHARACTERISTICS



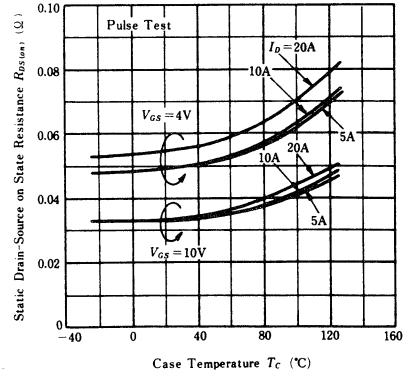
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



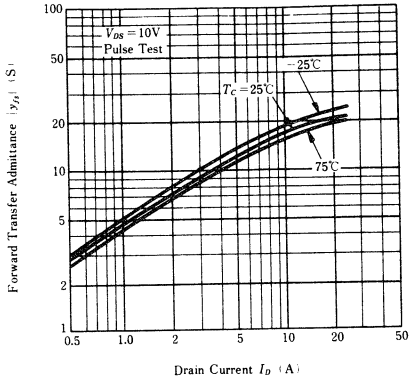
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



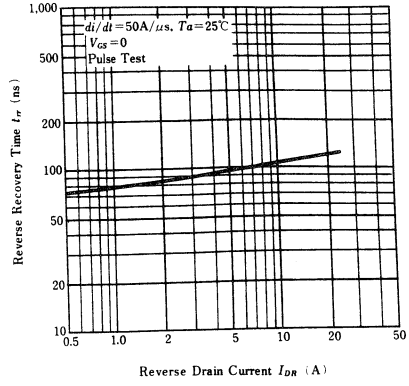
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



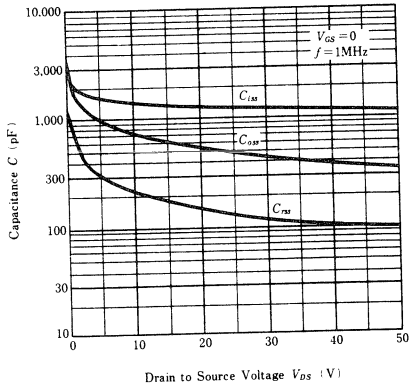
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



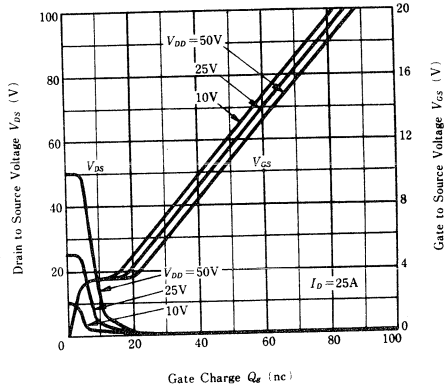
BODY-DRAIN DIODE REVERSE RECOVERY TIME



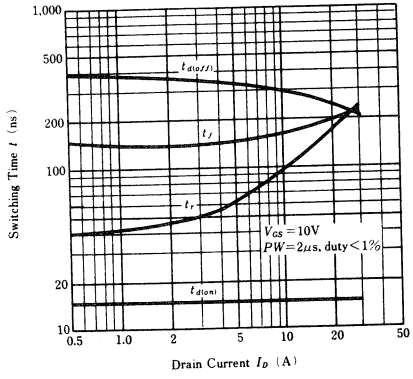
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



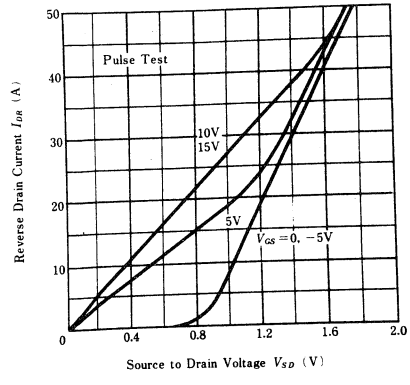
DYNAMIC INPUT CHARACTERISTICS



SWITCHING CHARACTERISTICS



REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE

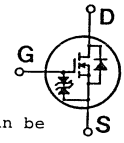


POWER MOS FET DⅢ SERIES

2SK973Ⓛ, 2SK973Ⓢ –Preliminary–

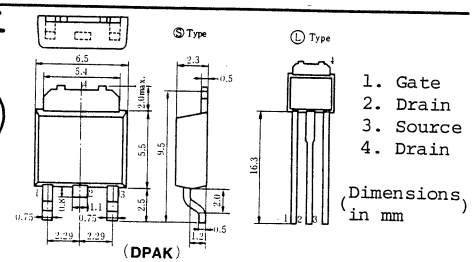
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- 4V Gate Drive Device Can be Driven From 5V Source.
- Suitable for DC-DC Convertor, Motor Drive, Power Switch, Solenoid Drive.



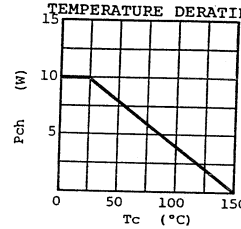
(DPAK)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	2	A
Drain Peak Current	$I_{D(pulse)}$*	8	A
Body-Drain Diode Reverse Drain Current	I_{DR}	2	A
Channel Dissipation	Pch**	10	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55 ~ +150	°C

*PW≤10μs, duty cycle≤1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

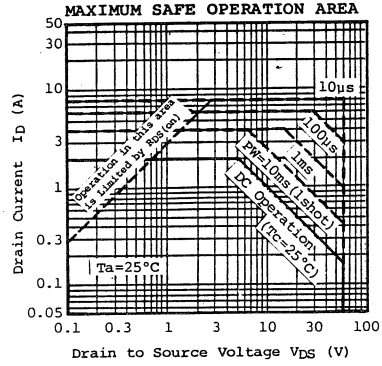
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D= 10mA , V_{GS}=0	60	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V, V_{GS}=0	-	-	100	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D= 1mA , V_{DS}= 10V	1.0	-	2.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=1A , V_{GS}=10V *	-	0.25	0.35	Ω
		I_D=1A , V_{GS}=4V *	-	0.40	0.50	
Foward Transfer Admittance	|Yfs|	I_D=1A , V_{DS}=10V *	1.2	2.0	-	S
Input Capacitance	Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	240	-	pF
Output Capacitance	Coss		-	115	-	pF
Reverse Transfer Capacitance	Crss		-	35	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=1A , V_{GS}=10V R_L=30Ω	-	4	-	ns
Rise Time	t_r		-	15	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	80	-	ns
Fall Time	t_f		-	40	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F= 2A , V_{GS}=0	-	1.0	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F= 2A , V_{GS}=0 dIF/dt= 50 A/μs	-	70	-	ns

*Pulse Test

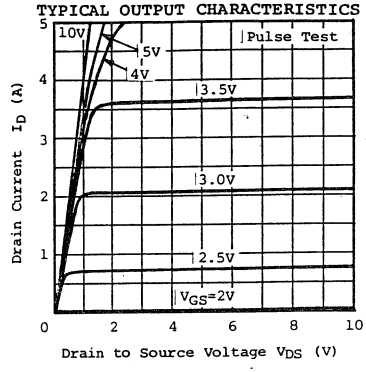
Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

HITACHI

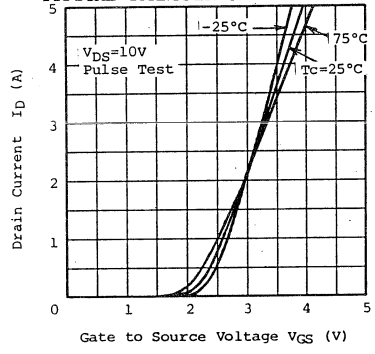
MAXIMUM SAFE OPERATION AREA



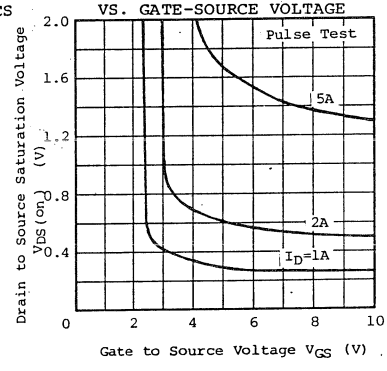
TYPICAL OUTPUT CHARACTERISTICS



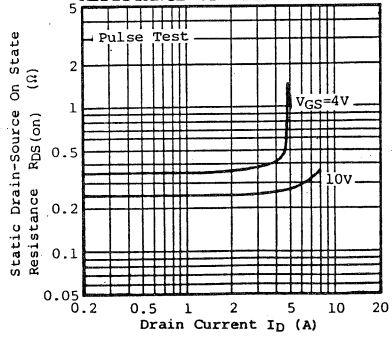
TYPICAL TRANSFER CHARACTERISTICS



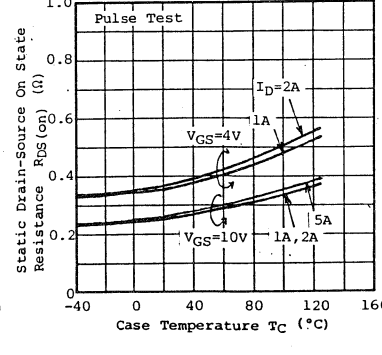
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



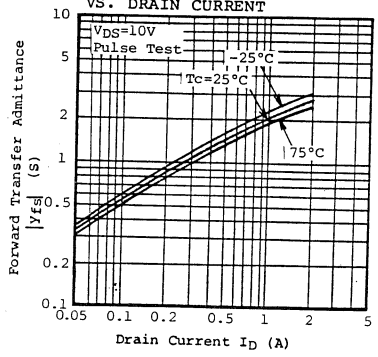
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



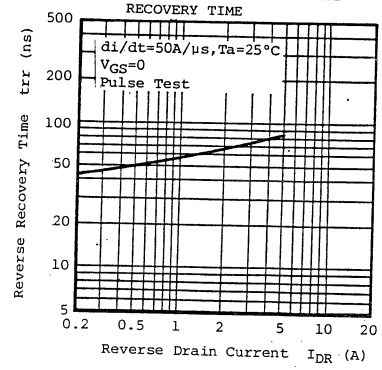
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



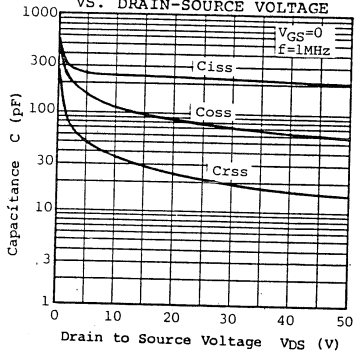
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



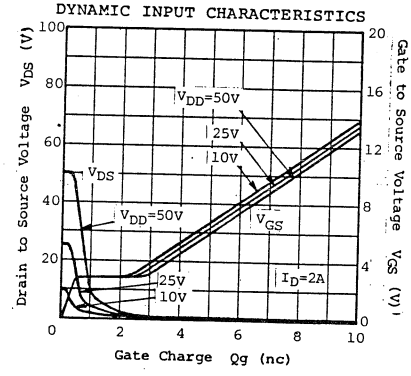
BODY-DRAIN DIODE REVERSE RECOVERY TIME



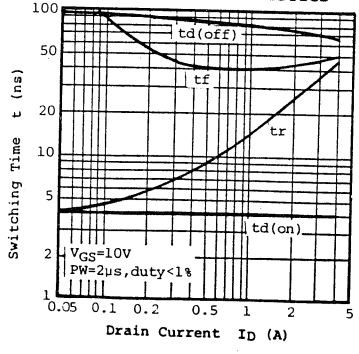
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



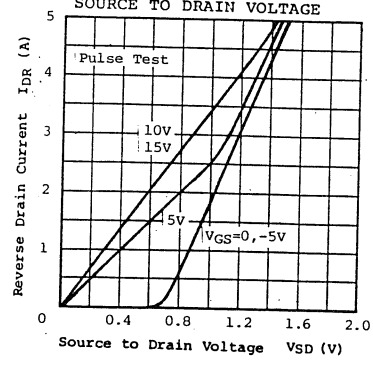
DYNAMIC INPUT CHARACTERISTICS



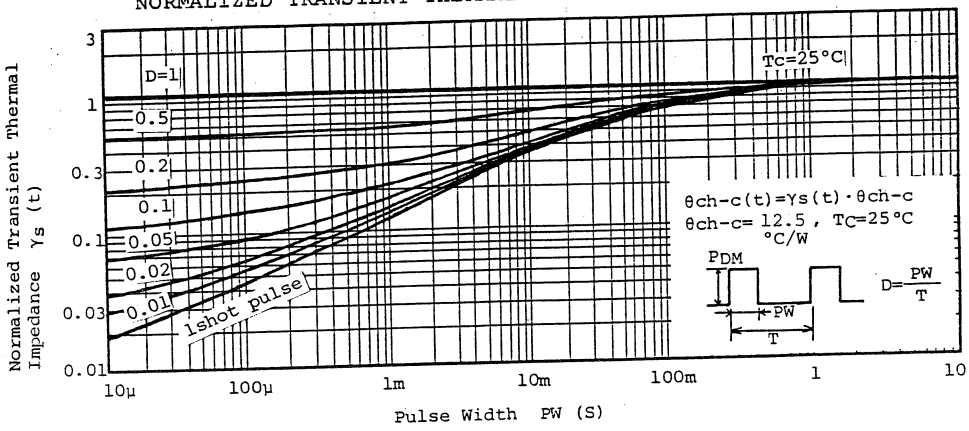
SWITCHING CHARACTERISTICS



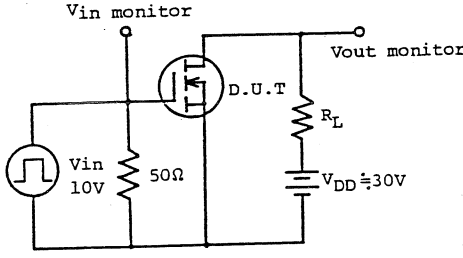
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



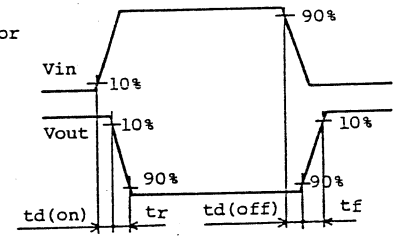
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



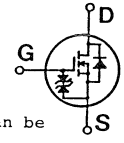
Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

POWER MOS FET DⅢ SERIES

2SK974Ⓛ, 2SK974Ⓢ –Preliminary–

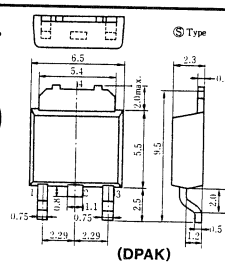
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- 4V Gate Drive Device Can be Driven From 5V Source.
- Suitable for DC-DC Convertor, Motor Drive, Power Switch, Solenoid Drive.



(DPAK)

1. Gate
2. Drain
3. Source
4. Drain

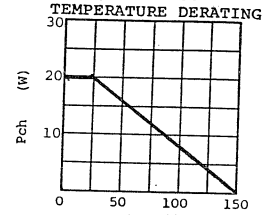
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	3	A
Drain Peak Current	$I_{D(pulse)}$*	12	A
Body-Drain Diode Reverse Drain Current	I_{DR}	3	A
Channel Dissipation	Pch**	20	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55～+150	°C

*PW≤10μs, duty cycle≤1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

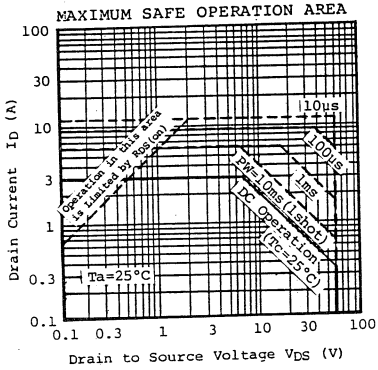
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	60	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=± 16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V , V_{GS}=0	-	-	100	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	1.0	-	2.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=2A , V_{GS}=10V *	-	0.15	0.18	Ω
		I_D=2A , V_{GS}=4V *	-	0.20	0.25	
Foward Transfer Admittance	|yfs|	I_D=2A , V_{DS}=10V *	2.4	4.0	-	S
Input Capacitance	Ciss	V_{DS}= 10 V, V_{GS}=0 f=1MHz	-	400	-	pF
Output Capacitance	Coss		-	230	-	pF
Reverse Transfer Capacitance	Crss		-	60	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D= 2A , V_{GS}=10V R_L= 15Ω	-	5	-	ns
Rise Time	t_r		-	25	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	180	-	ns
Fall Time	t_f		-	75	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F= 3A , V_{GS}=0	-	0.9	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F= 3A , V_{GS}=0 dIF/dt=50 A/μs	-	85	-	ns

*Pulse Test

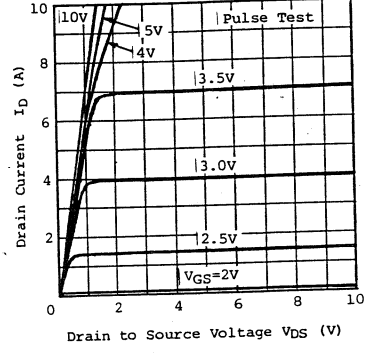
Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

HITACHI

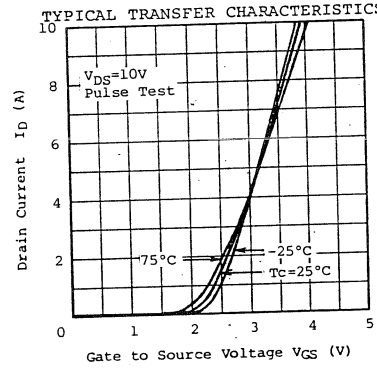
MAXIMUM SAFE OPERATION AREA



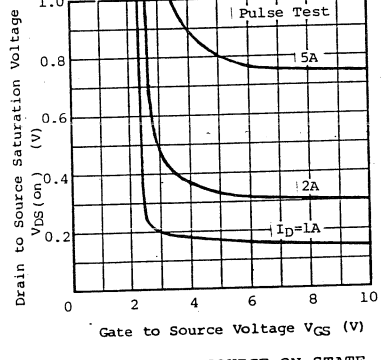
TYPICAL OUTPUT CHARACTERISTICS



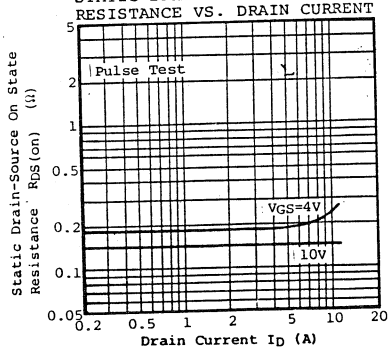
TYPICAL TRANSFER CHARACTERISTICS



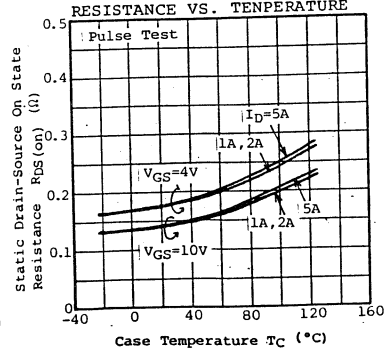
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



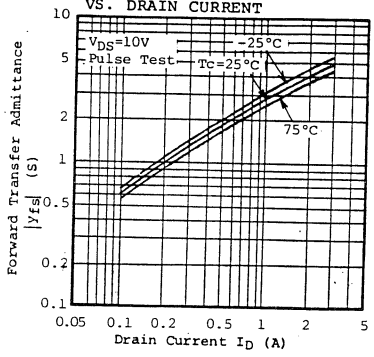
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



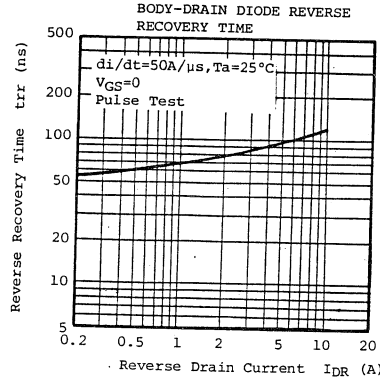
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



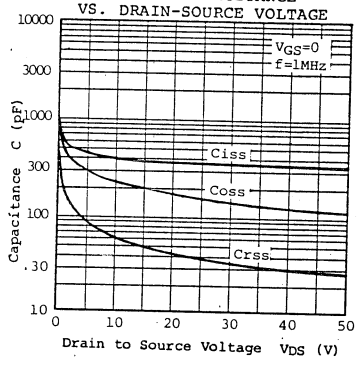
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



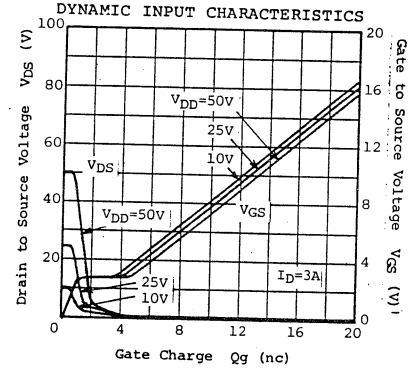
BODY-DRAIN DIODE REVERSE RECOVERY TIME



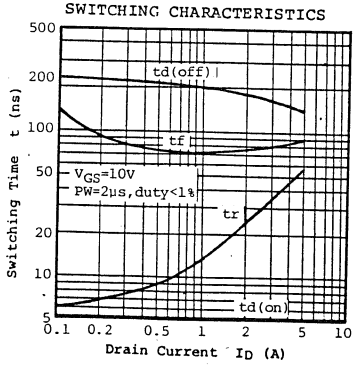
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



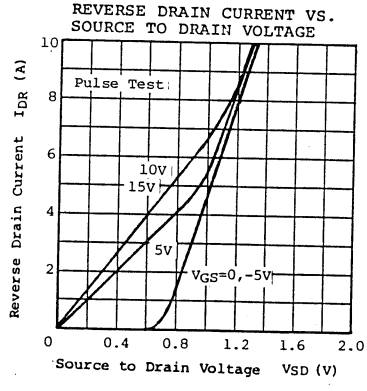
DYNAMIC INPUT CHARACTERISTICS



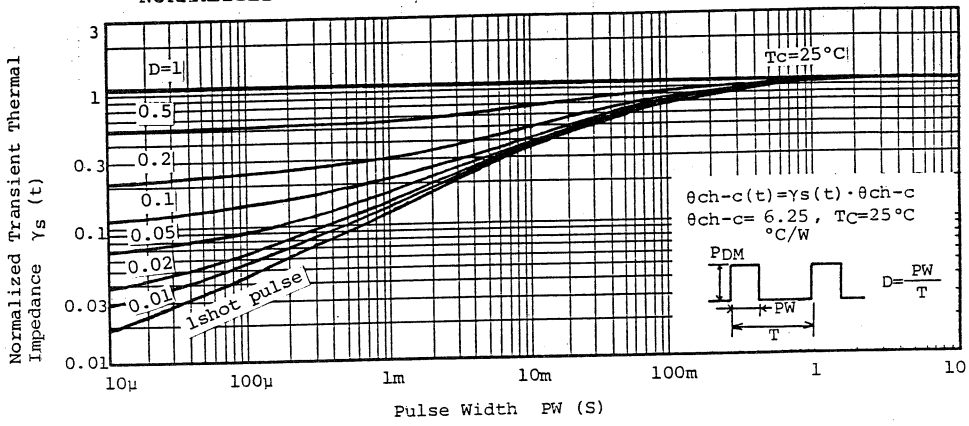
SWITCHING CHARACTERISTICS



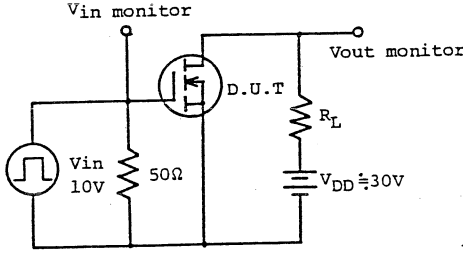
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



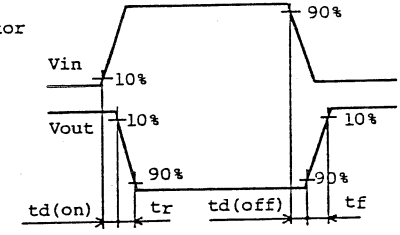
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



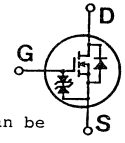
Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

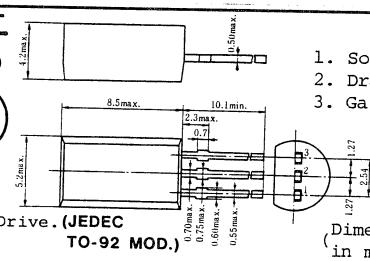
POWER MOS FET DⅢ SERIES

2SK975 —Preliminary—

SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING





1. Source
2. Drain
3. Gate

(JEDEC TO-92 MOD.)

(Dimensions in mm)

Features;

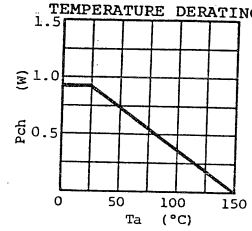
- Low On-Resistance.
- High Speed Switching.
- 4V Gate Drive Device Can be Driven From 5V Source.
- Suitable for DC-DC Convertor, Motor Drive, Power Switch, Solenoid Drive.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	1.5	A
Drain Peak Current	$I_{D(pulse)}$*	4.5	A
Body-Drain Diode Reverse Drain Current	I_{DR}	1.5	A
Channel Dissipation	Pch	900	mW
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 ~ +150	°C

*PW≦10μs, duty cycle≦1%

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

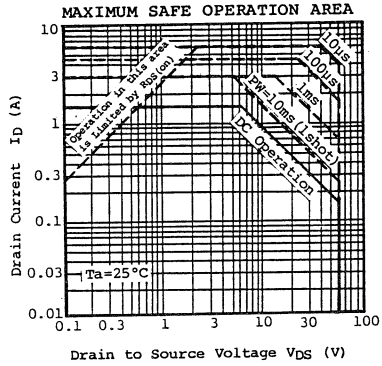
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	60	-	-	V
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Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V , V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V , V_{GS}=0	-	-	100	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	1.0	-	2.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=1A , V_{GS}=10V *	-	0.3	0.4	Ω
		I_D=1A V_{GS}=4V *	-	0.4	0.55	
Foward Transfer Admittance	|yfs|	I_D=1A , V_{DS}=10V *	0.9	1.5	-	S
Input Capacitance	Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	140	-	pF
Output Capacitance	Coss		-	70	-	pF
Reverse Transfer Capacitance	Crss		-	20	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D= 1A , V_{GS}=10V R_L=30Ω	-	3	-	ns
Rise Time	t_r		-	12	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	50	-	ns
Fall Time	t_f		-	30	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=1.5A , V_{GS}=0	-	0.9	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=1.5A , V_{GS}=0 dIF/dt= 50 A/μs	-	45	-	ns

*Pulse Test

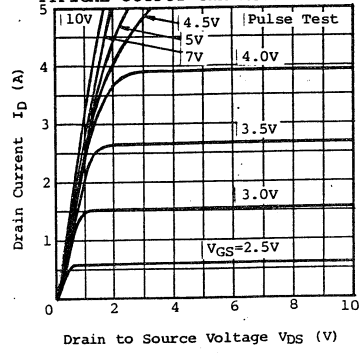
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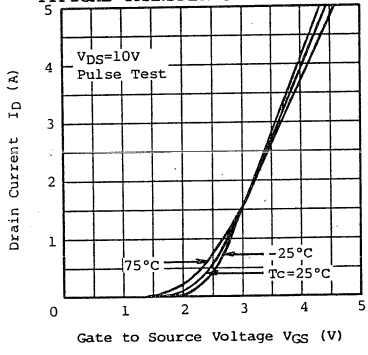
MAXIMUM SAFE OPERATION AREA



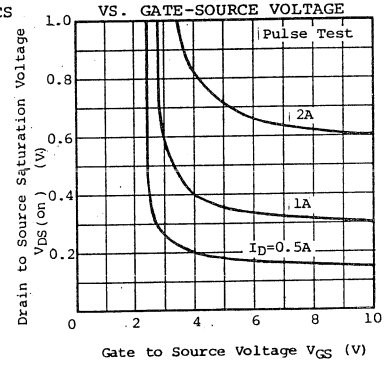
TYPICAL OUTPUT CHARACTERISTICS



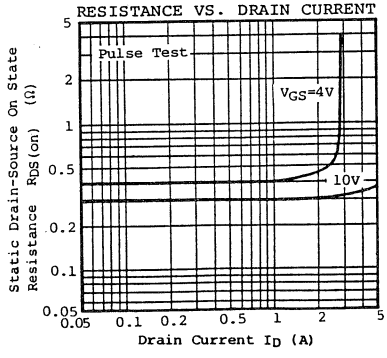
TYPICAL TRANSFER CHARACTERISTICS



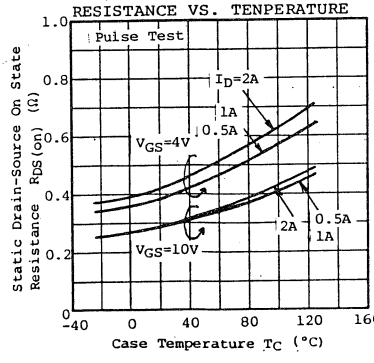
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



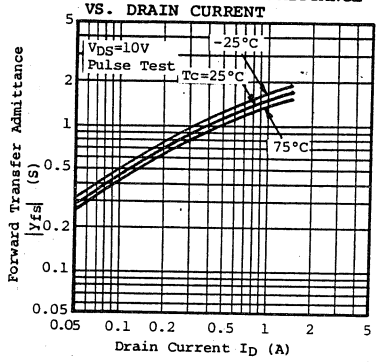
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



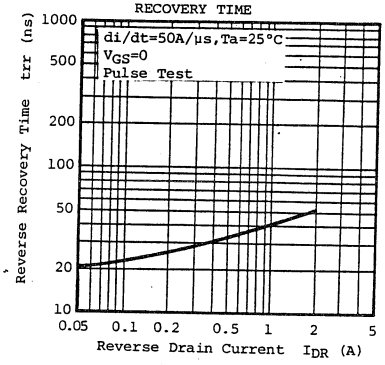
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



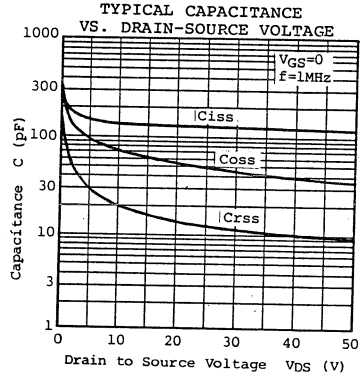
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



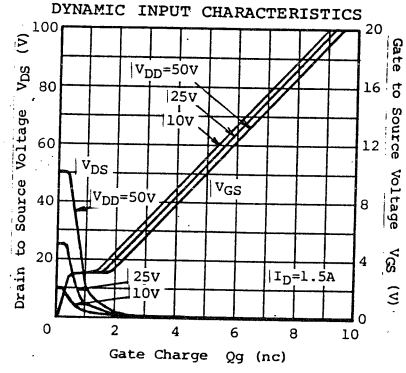
BODY-DRAIN DIODE REVERSE RECOVERY TIME



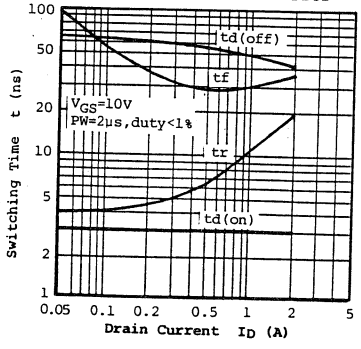
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



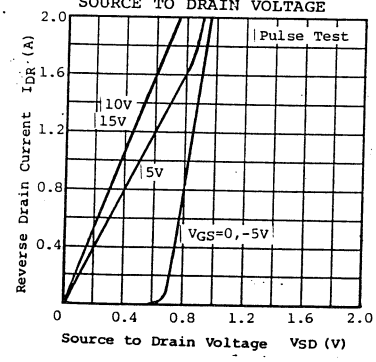
DYNAMIC INPUT CHARACTERISTICS



SWITCHING CHARACTERISTICS



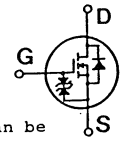
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



2SK1093 —Preliminary—

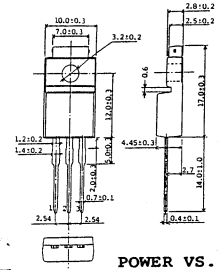
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- 4V Gate Drive Device Can be Driven From 5V Source.
- Suitable for DC-DC Convertor, Motor Drive, Power Switch, Solenoid Drive.



1. Gate
2. Drain
3. Source

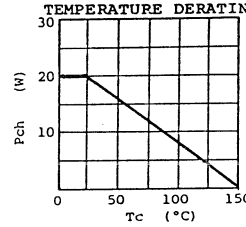
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
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Body-Drain Diode Reverse Drain Current	I_{DR}	10	A
Channel Dissipation	Pch**	20	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55 ~ +150	°C

*PW≤10μs, duty cycle≤1% ** Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



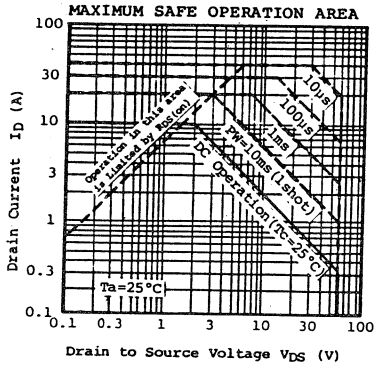
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Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V , V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V , V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}= 10V	1.0	-	2.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=5A , V_{GS}=10V *	-	0.12	0.15	Ω
		I_D=5A , V_{GS}=4V *	-	0.17	0.22	
Foward Transfer Admittance	|yfs|	I_D=5A , V_{DS}=10V *	3.5	6.0	-	S
Input Capacitance	Ciss	V_{DS}= 10 V, V_{GS}=0 f=1MHz	-	400	-	pF
Output Capacitance	Coss		-	220	-	pF
Reverse Transfer Capacitance	Crss		-	60	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D= 5A , V_{GS}= 10V R_L= 6Ω	-	5	-	ns
Rise Time	t_r		-	55	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	140	-	ns
Fall Time	t_f		-	90	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F= 10A , V_{GS}=0	-	1.2	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F= 10A , V_{GS}=0 dI_F/dt= 50 A/μs	-	125	-	ns

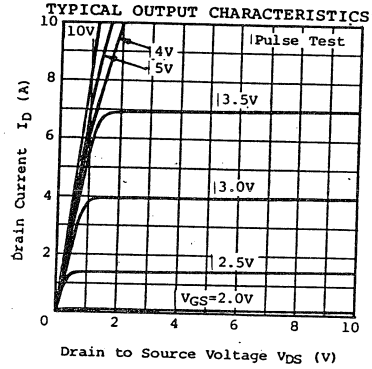
*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

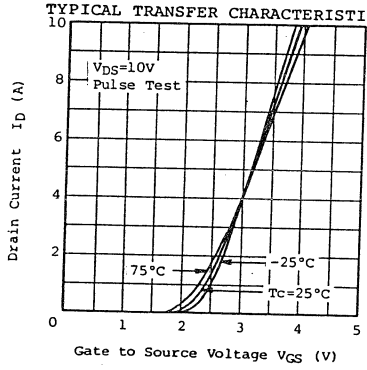
MAXIMUM SAFE OPERATION AREA



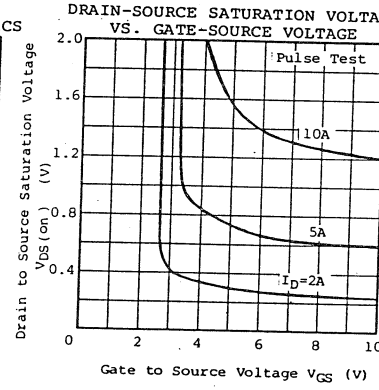
TYPICAL OUTPUT CHARACTERISTICS



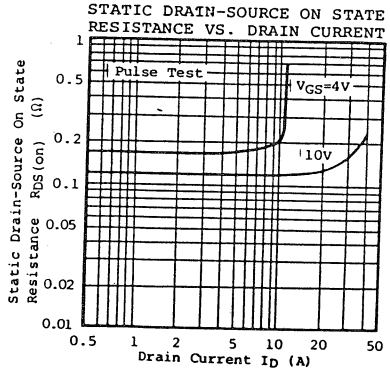
TYPICAL TRANSFER CHARACTERISTICS



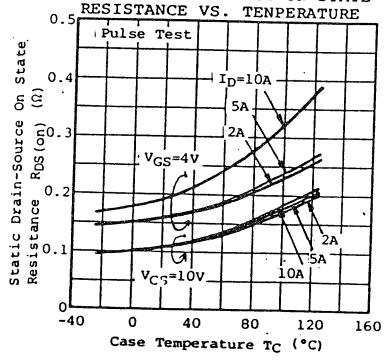
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



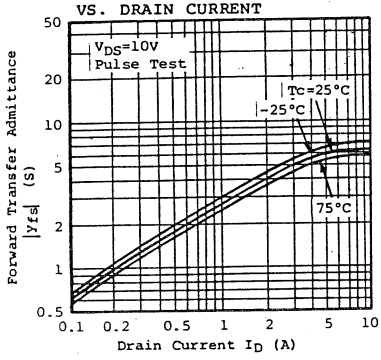
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



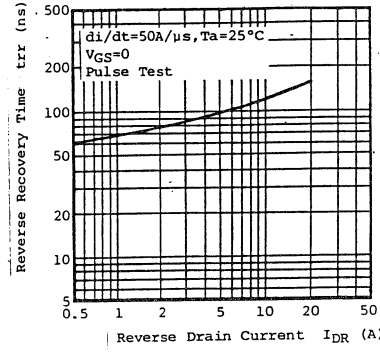
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



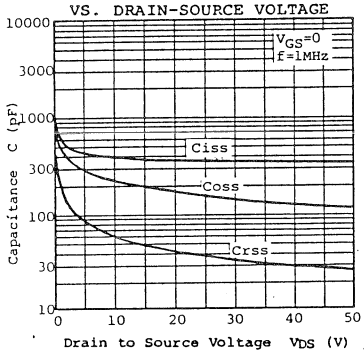
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



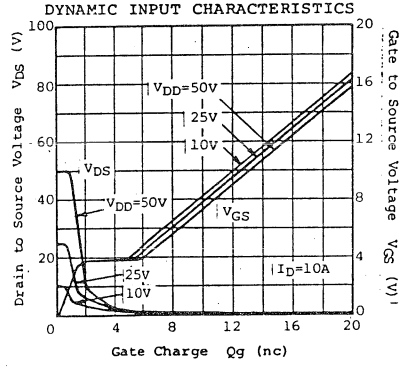
BODY-DRAIN DIODE REVERSE RECOVERY TIME



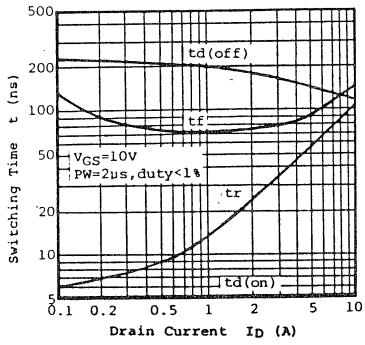
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



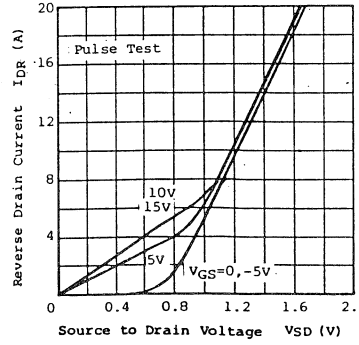
DYNAMIC INPUT CHARACTERISTICS



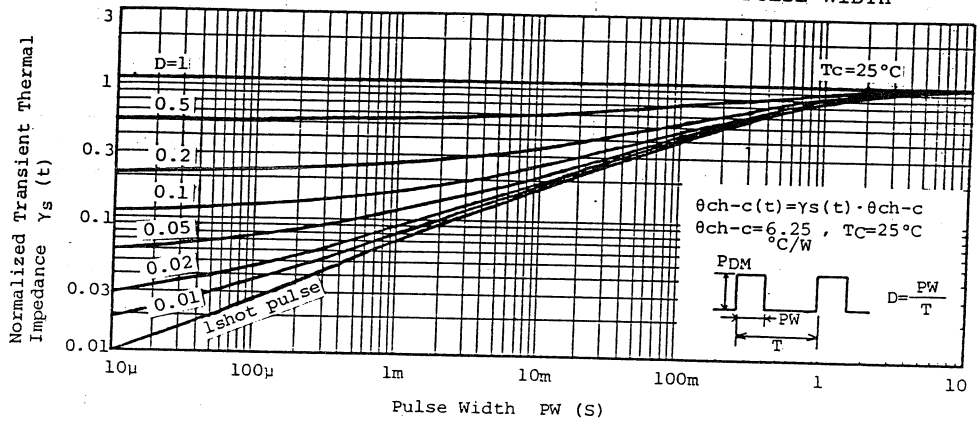
SWITCHING CHARACTERISTICS



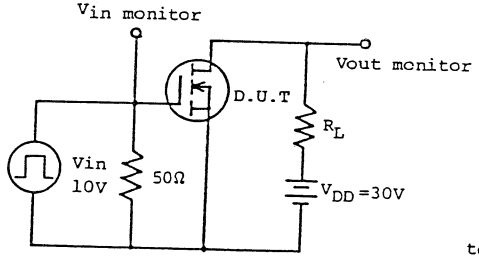
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



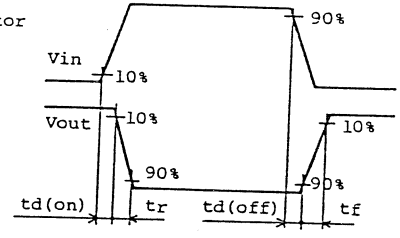
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS

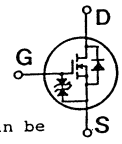


Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

2SK1094 —Preliminary—

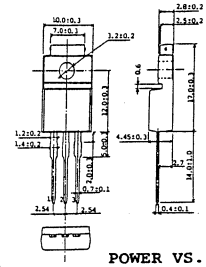
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- 4V Gate Drive Device Can be Driven From 5V Source.
- Suitable for DC-DC Convertor, Motor Drive, Power Switch, Solenoid Drive.



1. Gate
2. Drain
3. Source

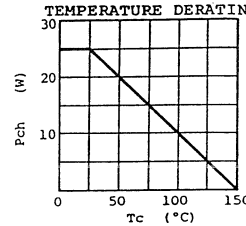
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	15	A
Drain Peak Current	$I_{D(pulse)}$*	60	A
Body-Drain Diode Reverse Drain Current	I_{DR}	15	A
Channel Dissipation	Pch**	25	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55 ~ +150	°C

*PW≤10μs, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



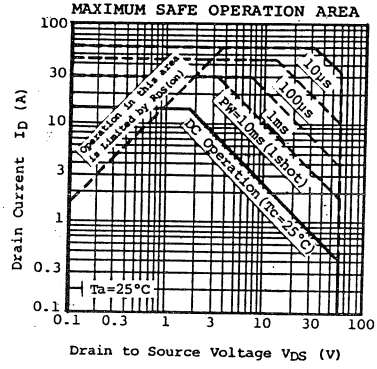
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	60	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V , V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V , V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	1.0	-	2.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=8A , V_{GS}=10V *	-	0.055	0.065	Ω
		I_D=8A , V_{GS}=4V *	-	0.075	0.095	
Foward Transfer Admittance	$\|yfs\|$	I_D=8A , V_{DS}=10V *	7	12	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz	-	860	-	pF
Output Capacitance	Coss		-	450	-	pF
Reverse Transfer Capacitance	Crss		-	140	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=8A , V_{GS}=10V R_L=3.75Ω	-	10	-	ns
Rise Time	t_r		-	70	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	180	-	ns
Fall Time	t_f		-	120	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=15A , V_{GS}=0	-	1.3	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=15A , V_{GS}=0 dI_F/dt=50 A/μs	-	135	-	ns

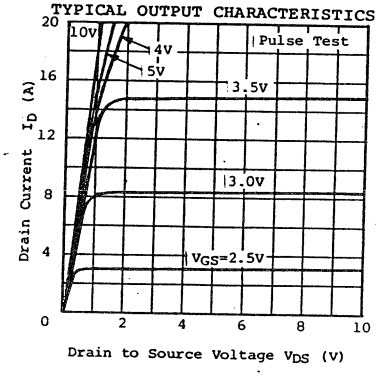
*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

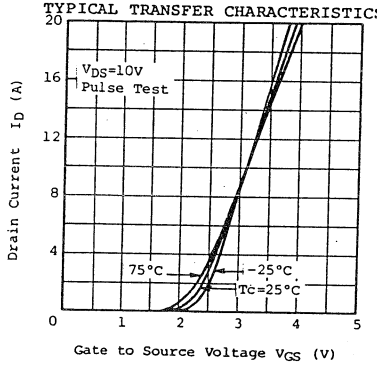
MAXIMUM SAFE OPERATION AREA



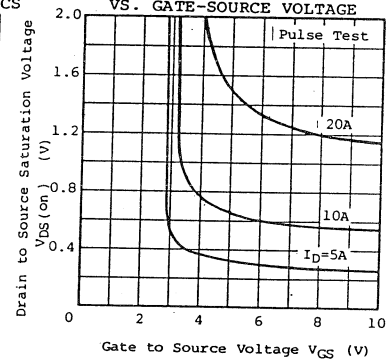
TYPICAL OUTPUT CHARACTERISTICS



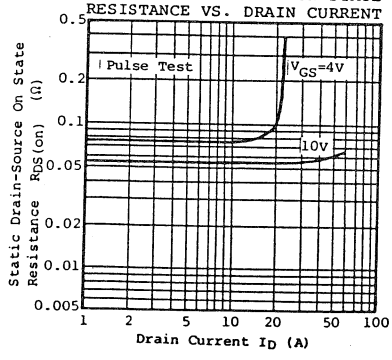
TYPICAL TRANSFER CHARACTERISTICS



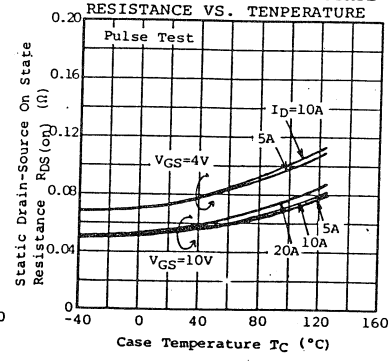
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



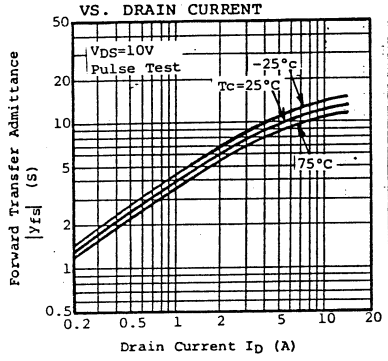
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



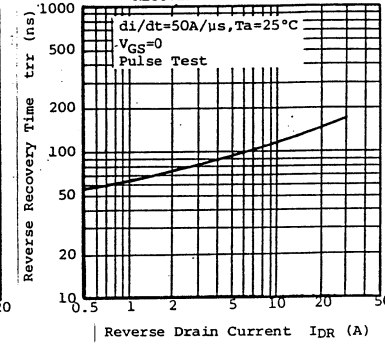
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



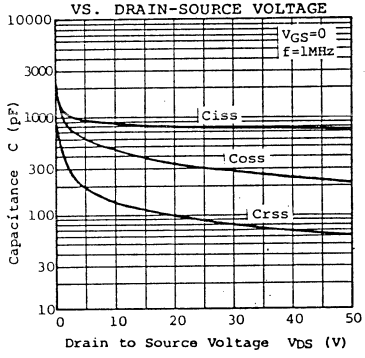
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



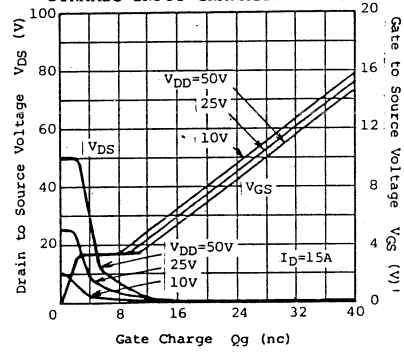
BODY-DRAIN DIODE REVERSE RECOVERY TIME



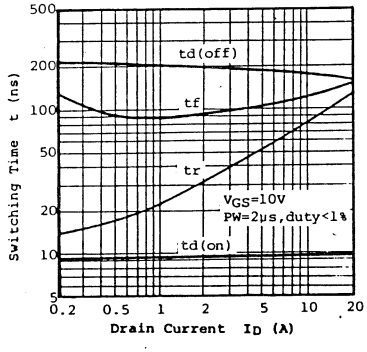
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



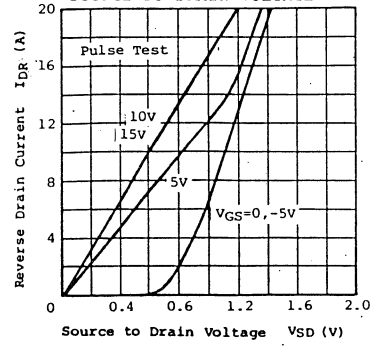
DYNAMIC INPUT CHARACTERISTICS



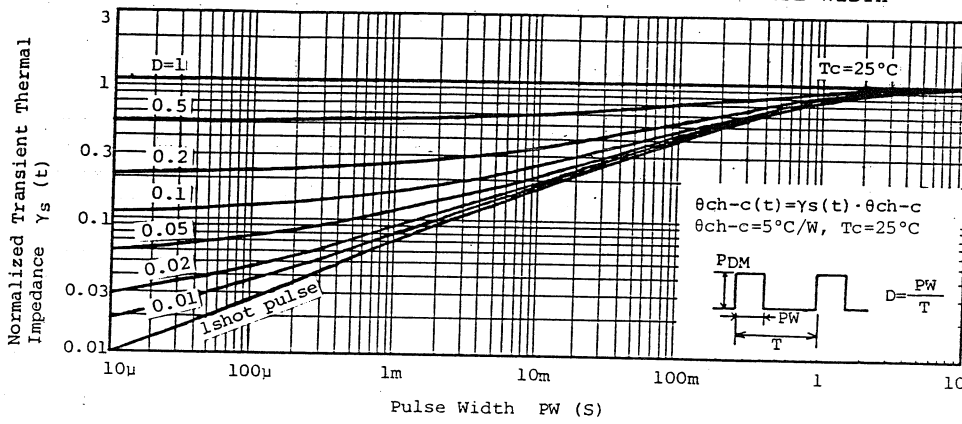
SWITCHING CHARACTERISTICS



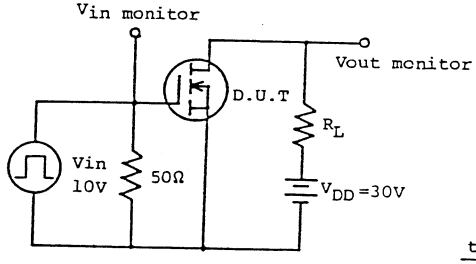
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



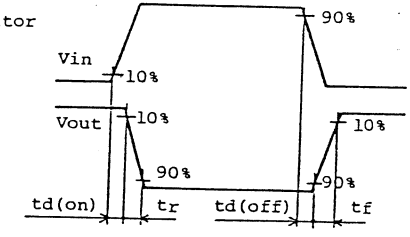
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS

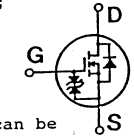


Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

2SK1095 —Preliminary—

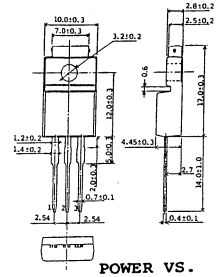
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- 4V Gate Drive Device.....can be Driven From 5V Source.
- Suitable for DC-DC Convertor, Motor Drive, Power Switch, Solenoid Drive.



1. Gate
2. Drain
3. Source

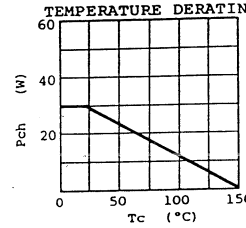
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	25	A
Drain Peak Current	$I_{D(pulse)}$*	100	A
Body-Drain Diode Reverse Drain Current	I_{DR}	25	A
Channel Dissipation	Pch**	30	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55 ~ +150	°C

*PW≤10μs, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



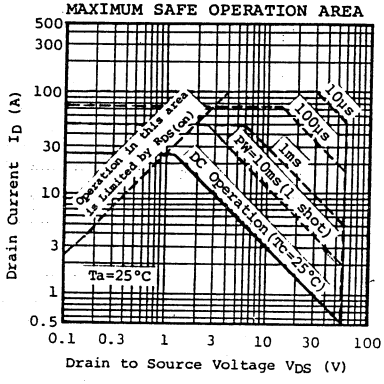
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D= 10mA , V_{GS}=0	60	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V , V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V *	1.0	-	2.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=15A , V_{GS}=10V *	-	0.033	0.04	Ω
		I_D=15A , V_{GS}=4V *	-	0.05	0.06	
Foward Transfer Admittance	|yfs|	I_D=15A , V_{DS}=10V	12	20	-	S
Input Capacitance	Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	1400	-	pF
Output Capacitance	Coss		-	720	-	pF
Reverse Transfer Capacitance	Crss		-	220	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D= 15A, V_{GS}= 10V, R_L= 2Ω	-	15	-	ns
Rise Time	t_r		-	130	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	270	-	ns
Fall Time	t_f		-	180	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F= 25A , V_{GS}=0	-	1.3	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F= 25A , V_{GS}=0 dIF/dt= 50 A/μs	-	135	-	ns

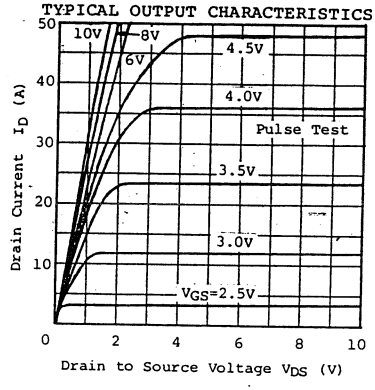
*Pulse Test

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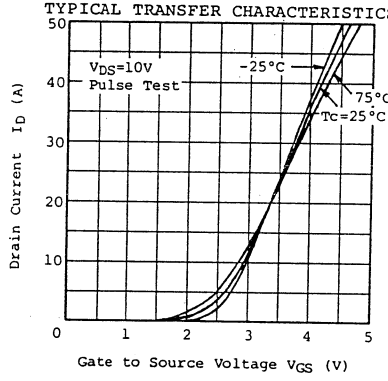
MAXIMUM SAFE OPERATION AREA



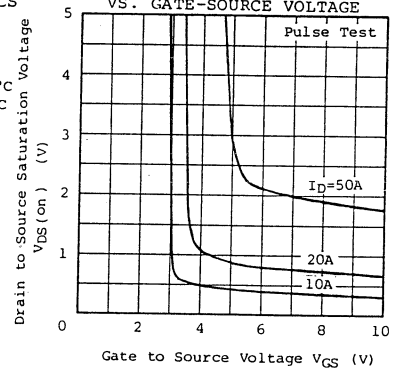
TYPICAL OUTPUT CHARACTERISTICS



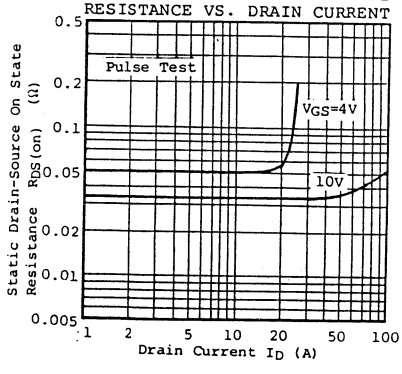
TYPICAL TRANSFER CHARACTERISTICS



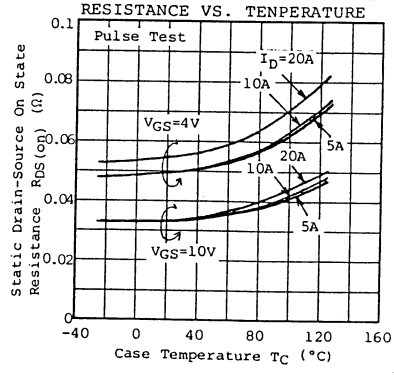
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



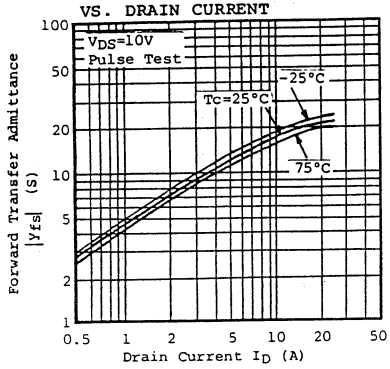
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



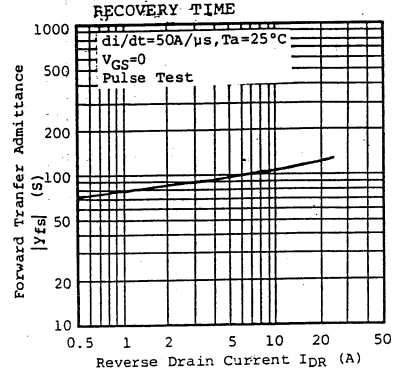
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



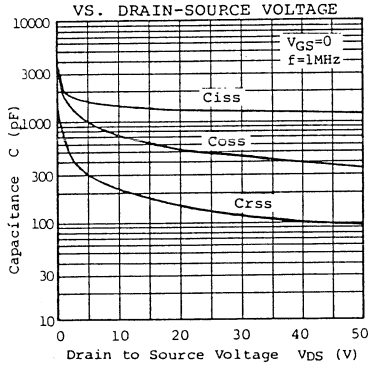
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



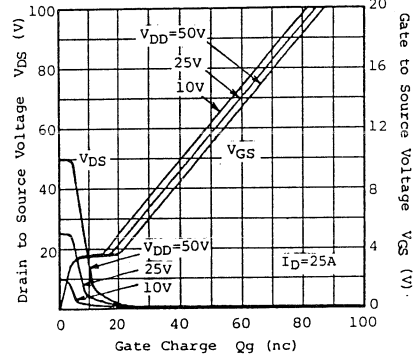
BODY-DRAIN DIODE REVERSE RECOVERY TIME



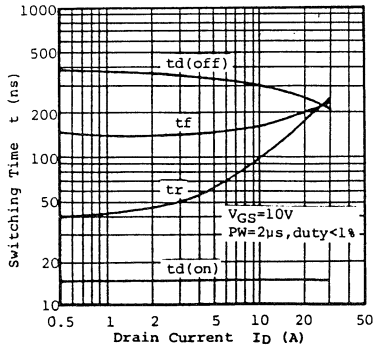
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



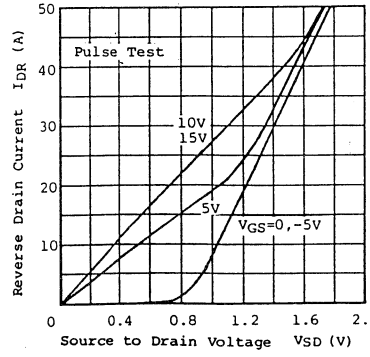
DYNAMIC INPUT CHARACTERISTICS



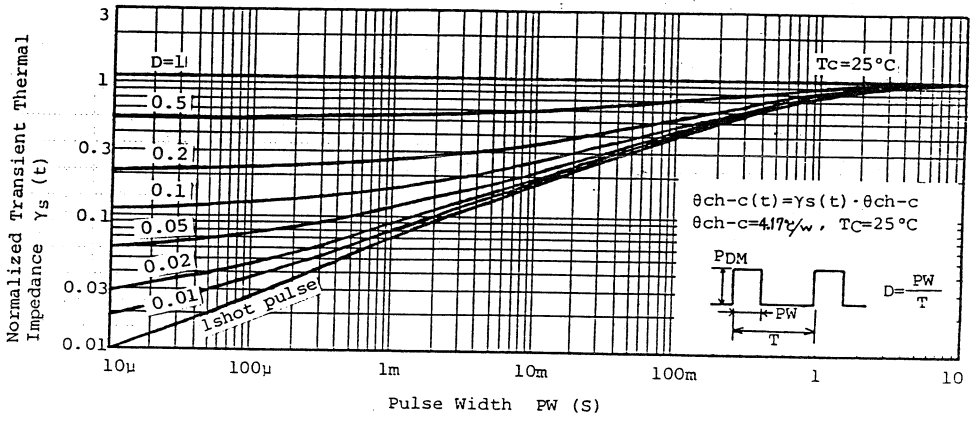
SWITCHING CHARACTERISTICS



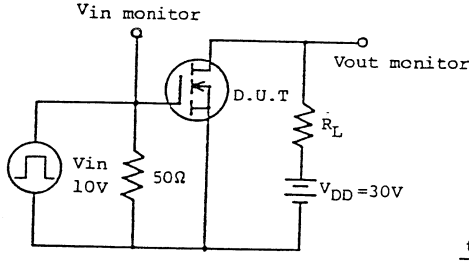
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



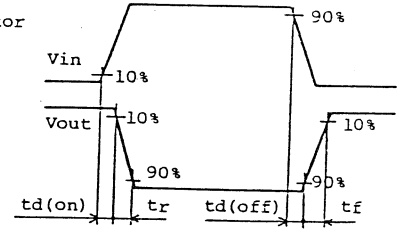
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS

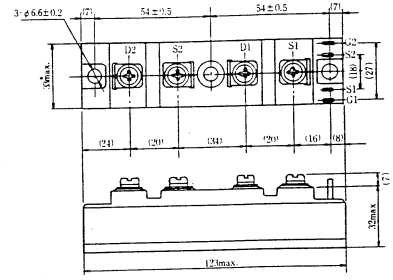


Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

PM45502C

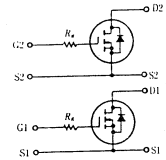
–Preliminary–

SILICON N-CHANNEL POWER MOSFET MODULE
HIGH SPEED POWER SWITCHING



■ FEATURES

- ●Power MOSFET Module
  - • Low On-Resistance
  - • High Speed Switching
  - • High Efficiency, Less Driving Loss and Simple Driving Circuit
  - • No Secondary Breakdown
- ●Inherent Parallel Diode between Source and Drain
- ●Isolated Base From Terminals
- ●Suitable for Switching Regulators, DC-DC Converters and Motor Drives



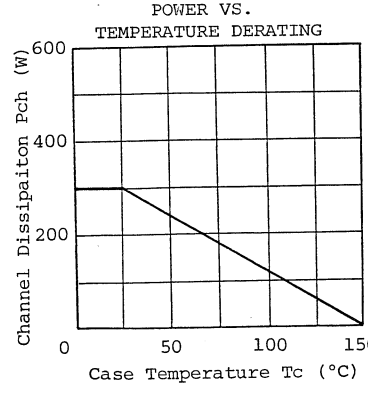
No.	Electrode	Terminals	Remarks
S1	Source 1	M5 Screw	Power terminals
D1	Drain 1	M5 Screw	Power terminals
S2	Source 2	M5 Screw	Power terminals
D2	Drain 2	M5 Screw	Power terminals
G1	Gate 1	#110	Signal terminals
S1	Source 1	#110	Signal terminals
G2	Gate 2	#110	Signal terminals
S2	Source 2	#110	Signal terminals

(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)
(Per FET Chip)

Item	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DSS}	450	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	50	A
Drain Peak Current	I_D(peak)	100	A
Body-Drain Diode Reverse Drain Current	I_{DR}	50	A
Body-Drain Diode Reverse Drain Peak Current	I_{DR}(peak)	100	A
Channel Dissipation	P_D*	300	W
Channel Temperature	Tch	150	℃
Storage Temperature	Tstg	−45～+125	℃
Insulation Dielectric	Visol**	2000	V

* Value at Tc=25℃
** Base to Terminals AC minute



Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

■ ELECTRICAL CHARACTERISTICS (Ta=25℃)

(Per FET chip)

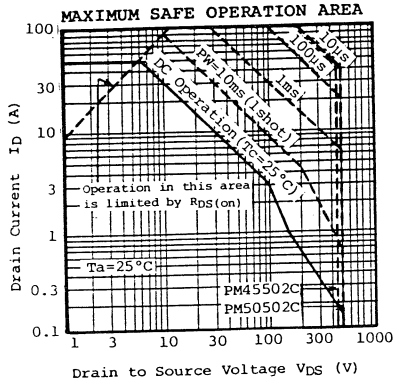
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain−Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 10mA$, $V_{GS} = 0$	450	−	−	V
Gate−Source Leak Current	I_{GSS}	$V_{GS} = \pm 16V$, $V_{DS} = 0$	−	−	±50	μA
Gate−Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = \pm 100\mu A$, $V_{DS} = 0$	±20	−	−	V
Gate Leak Current	I_{DSS}	$V_{DS} = 360V$, $V_{GS} = 0$	−	−	1	mA
Gate−Source Threshold Voltage	$V_{GS}(th)$	$I_D = 1mA$, $V_{DS} = 10V$	1.5	−	4.0	V
Drain−Source Saturation Voltage	$V_{DS(on)}$	$I_D = 25A$, $V_{GS} = 10V$*	−	2.0	3.0	V
Static Drain−Source On State Resistance	$R_{DS(on)}$	$I_D = 25A$, $V_{GS} = 10V$*	−	0.08	0.12	Ω
Forward Transfer Admittance	$\|yfs\|$	$I_D = 25A$, $V_{DS} = 10V$*	25	40	−	S
Input Capacitance	Ciss	$V_{DS} = 10v$, $V_{GS} = 0$ f = 1MHz	−	10250	−	pF
Output Capacitance	Coss		−	3600	−	pF
Reverse Transfer Capacitance	Crss		−	400	−	pF
Turn−on Delay Time	td(on)	$I_D = 25A$, $V_{GS} = 10V$ $R_L = 1.2\Omega$	−	150	−	ns
Rise Time	tr		−	700	−	ns
Turn−off Delay Time	td(off)		−	800	−	ns
Fall Time	tf		−	600	−	ns
Body−Drain Diode Forward Voltage	V_{DF}	$I_F = 25A$, $V_{GS} = 0$	−	1.2	−	V
Body−Drain Diode Reverse Recovery Time	trr	$I_F = 25A$, $V_{GS} = 0$ $di/dt = 100A/\mu s$	−	200	−	ns

*Pulse Test

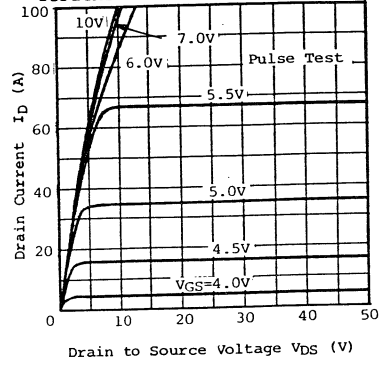
■ MECHANICAL CHARACTERISTICS

Item	Symbol	Condition	Rating	Unit
Fixing Strength	−	Mounted into main−terminal with M5 screw	15～20	kg cm
	−	Mounted into heat sink with M6 screw	20～30	kg cm
Weight	−	Typical value	300	g

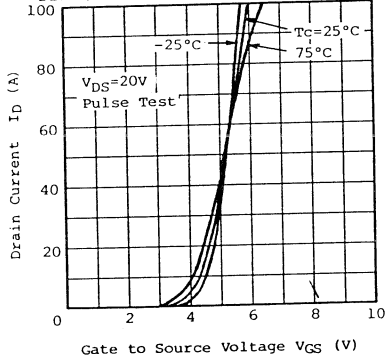
MAXIMUM SAFE OPERATION AREA



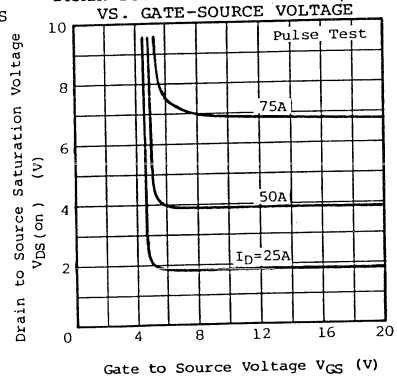
TYPICAL OUTPUT CHARACTERISTICS



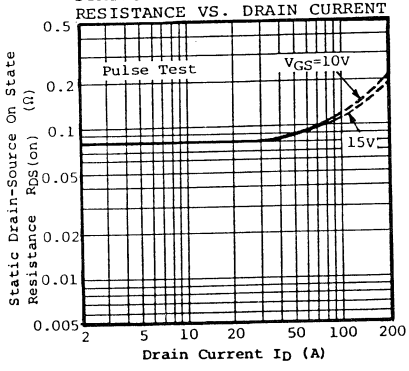
TYPICAL TRANSFER CHARACTERISTICS



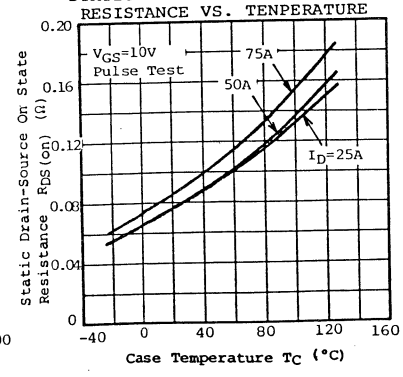
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



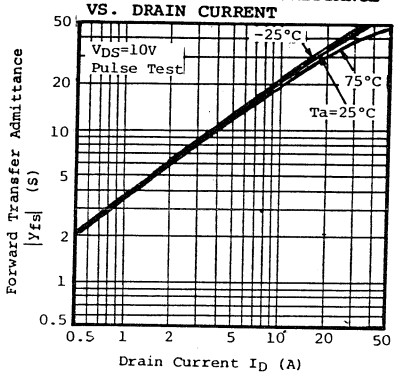
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



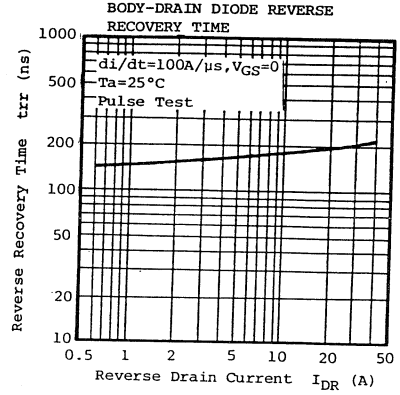
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



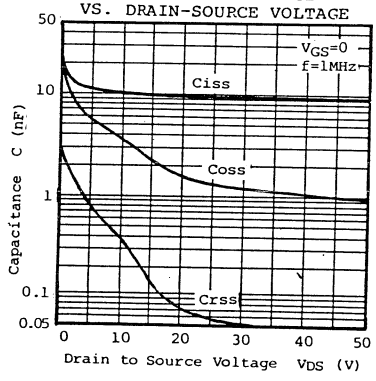
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



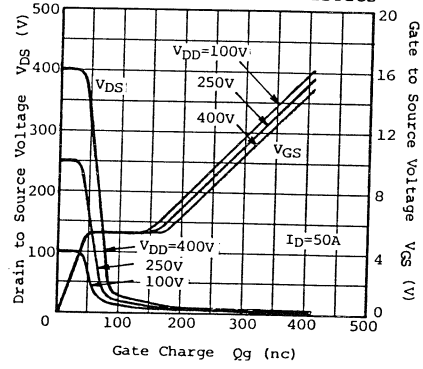
BODY-DRAIN DIODE REVERSE RECOVERY TIME



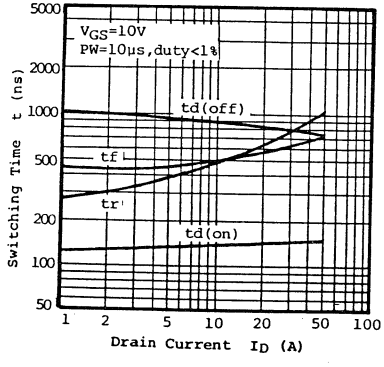
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



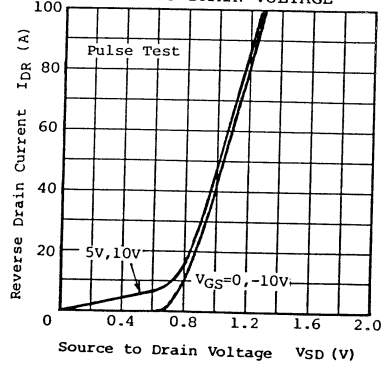
DYNAMIC INPUT CHARACTERISTICS



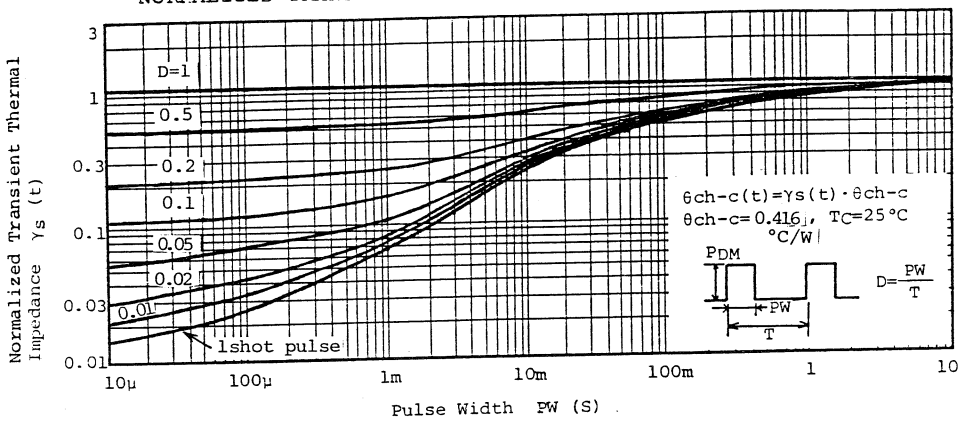
SWITCHING CHARACTERISTICS



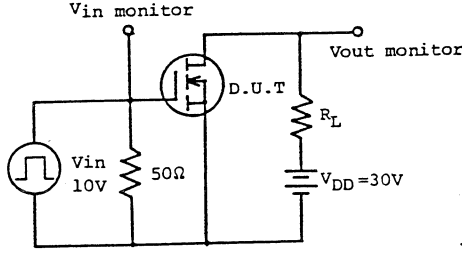
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



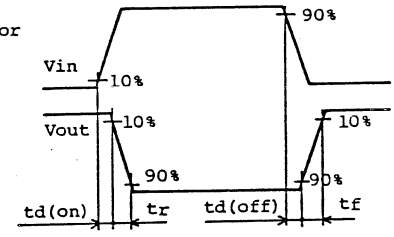
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

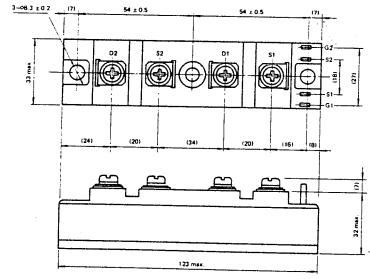
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—Preliminary—

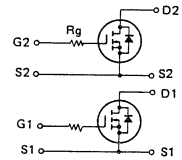
SILICON N-CHANNEL POWER MOSFET MODULE
HIGH SPEED POWER SWITCHING

FEATURES

- Power MOSFET Module
  - Low On-Resistance
  - High Speed Switching
  - High Efficiency, Less Driving Loss and Simple Driving Circuit
  - No Secondary Breakdown
- Inherent Parallel Diode between Source and Drain
- Isolated Base From Terminals
- Suitable for Switching Regulators, DC-DC Converters and Motor Drives



(Dimensions in mm)

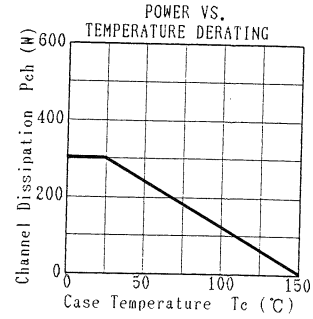


Symbol	Electrode	Terminals	Remarks
S1	Source 1	M5 Screw	Power terminals
D1	Drain 1	M5 Screw	Power terminals
S2	Source 2	M5 Screw	Power terminals
D2	Drain 2	M5 Screw	Power terminals
G1	Gate 1	#110	Signal terminals
S1	Source 1	#110	Signal terminals
G2	Gate 2	#110	Signal terminals
S2	Source 2	#110	Signal terminals

ABSOLUTE MAXIMUM RATINGS (Ta=25℃)
(Per FET Chip)

Item	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DSS}	500	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	50	A
Drain Peak Current	I_D(peak)	100	A
Body-Drain Diode Reverse Drain Current	I_{DR}	50	A
Body-Drain Diode Reverse Drain Peak Current	I_{DR}(peak)	100	A
Channel Dissipation	Pch*	300	W
Channel Temperature	Tch	150	℃
Storage Temperature	Tstg	−45～+125	℃
Insulation Dielectric	Visol**	2000	V

* Value at Tc=25℃
** Base to Terminals AC minute



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■ ELECTRICAL CHARACTERISTICS (Ta=25℃)

(Per FET chip)

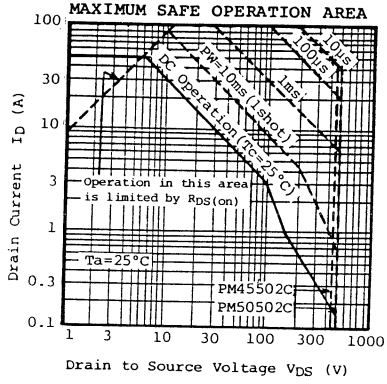
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain−Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 10mA$, $V_{GS} = 0$	500	−	−	V
Gate−Source Leak Current	I_{GSS}	$V_{GS} = \pm 16V$, $V_{DS} = 0$	−	−	±50	μA
Gate−Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = \pm 100\mu A$, $V_{DS} = 0$	±20	−	−	V
Gate Leak Current	I_{DSS}	$V_{DS} = 400V$, $V_{GS} = 0$	−	−	1	mA
Gate−Source Threshold Voltage	$V_{GS}(th)$	$I_D = 1mA$, $V_{DS} = 10V$	1.5	−	4.0	V
Drain−Source Saturation Voltage	$V_{DS(on)}$	$I_D = 25A$, $V_{GS} = 10V$*	−	2.25	3.0	V
Static Drain−Source On State Resistance	$R_{DS(on)}$	$I_D = 25A$, $V_{GS} = 10V$*	−	0.09	0.12	Ω
Forward Transfer Admittance	$\|yfs\|$	$I_D = 25A$, $V_{DS} = 10V$*	25	40	−	S
Input Capacitance	Ciss	$V_{DS} = 10v$, $V_{GS} = 0$ f = 1MHz	−	10250	−	pF
Output Capacitance	Coss		−	3600	−	pF
Reverse Transfer Capacitance	Crss		−	400	−	pF
Turn−on Delay Time	td(on)	$I_D = 25A$, $V_{GS} = 10V$ $R_L = 1.2\Omega$	−	150	−	ns
Rise Time	tr		−	700	−	ns
Turn−off Delay Time	td(off)		−	800	−	ns
Fall Time	tf		−	600	−	ns
Body−Drain Diode Forward Voltage	V_{DF}	$I_F = 25A$, $V_{GS} = 0$	−	1.2	−	V
Body−Drain Diode Reverse Recovery Time	trr	$I_F = 25A$, $V_{GS} = 0$ $di/dt = 100A/\mu s$	−	200	−	ns

*Pulse Test

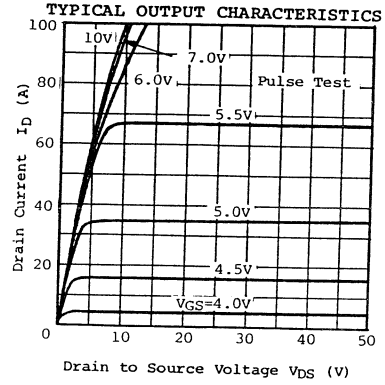
■ MECHANICAL CHARACTERISTICS

Item	Symbol	Condition	Rating	Unit
Fixing Strength	−	Mounted into main−terminal with M5 screw	15～20	kg·cm
	−	Mounted into heat sink with M6 screw	20～30	kg·cm
Weight	−	Typical value	300	g

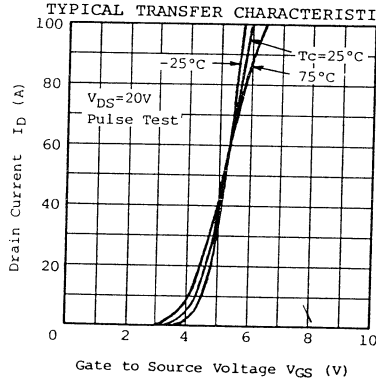
MAXIMUM SAFE OPERATION AREA



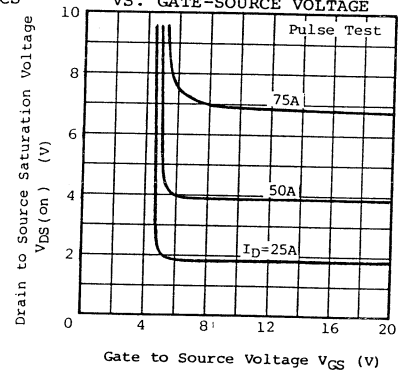
TYPICAL OUTPUT CHARACTERISTICS



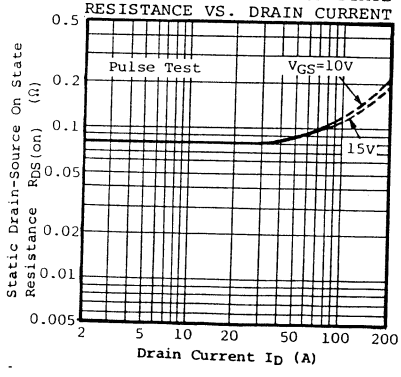
TYPICAL TRANSFER CHARACTERISTICS



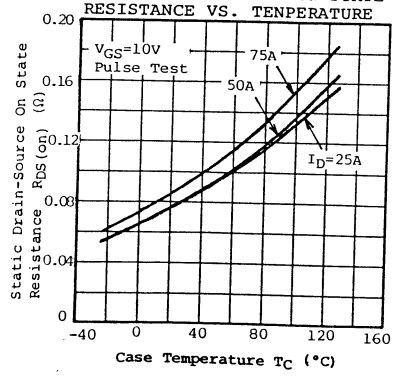
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



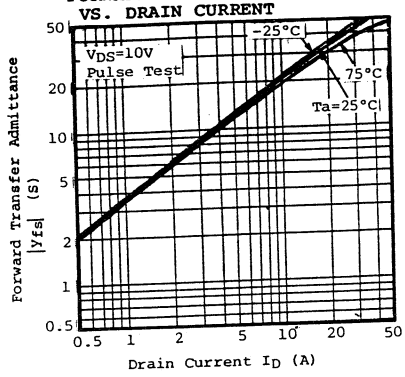
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



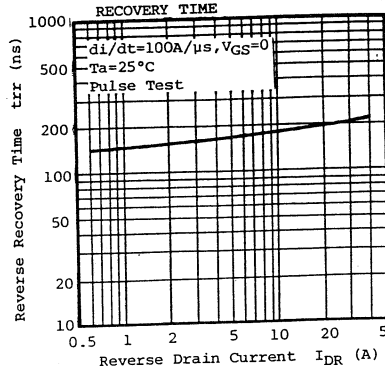
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



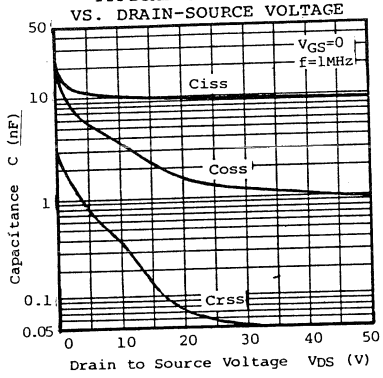
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



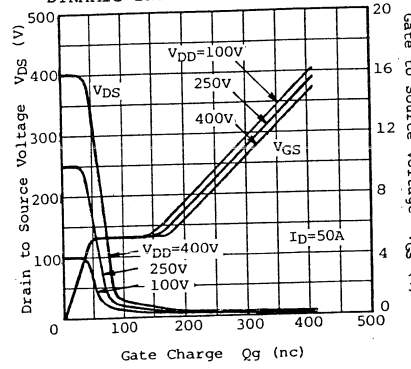
BODY-DRAIN DIODE REVERSE RECOVERY TIME



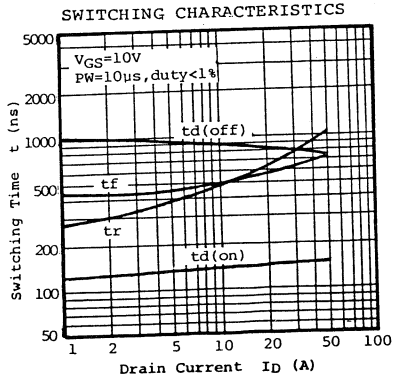
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



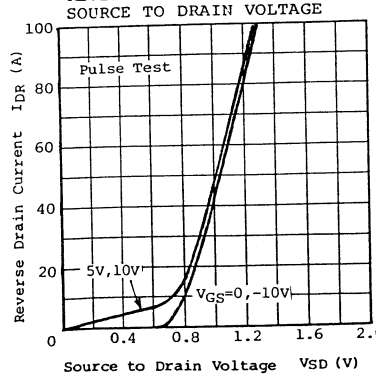
DYNAMIC INPUT CHARACTERISTICS



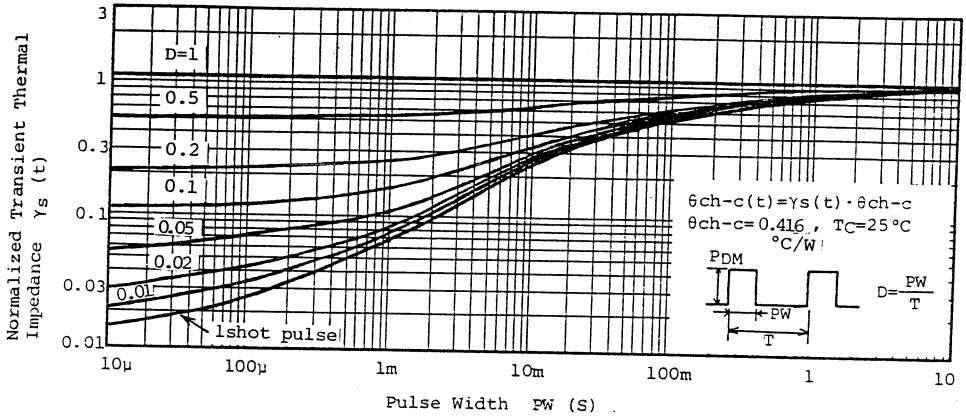
SWITCHING CHARACTERISTICS



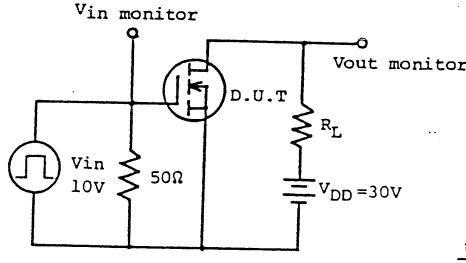
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



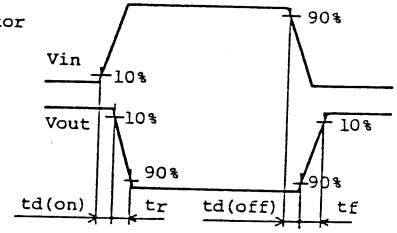
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS

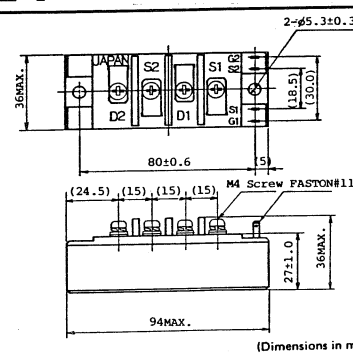


Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

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–Preliminary–

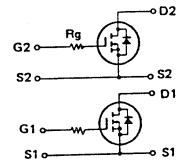
SILICON N-CHANNEL POWER MOSFET MODULE
HIGH SPEED POWER SWITCHING



(Dimensions in mm)

■ FEATURES

- ● Power MOSFET Module
  - • Low On-Resistance
  - • High Speed Switching
  - • High Efficiency, Less Driving Loss and Simple Driving Circuit
  - • No Secondary Breakdown
- ● Inherent Parallel Diode between Source and Drain
- ● Isolated Base From Terminals
- ● Suitable for Switching Regulators, DC-DC Converters and Motor Drives

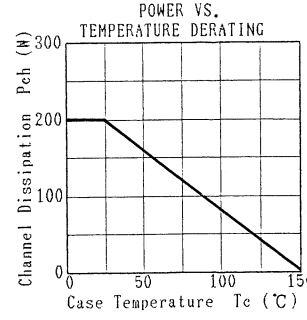


Symbol	Electrode	Terminals	Remarks
S1	Source 1	M4 Screw	Power terminals
D1	Drain 1	M4 Screw	Power terminals
S2	Source 2	M4 Screw	Power terminals
D2	Drain 2	M4 Screw	Power terminals
G1	Gate 1	#110	Signal terminals
S1	Source 1	#110	Signal terminals
G2	Gate 2	#110	Signal terminals
S2	Source 2	#110	Signal terminals

■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)
(Per FET Chip)

Item	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DSS}	450	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	30	A
Drain Peak Current	I_D(peak)	60	A
Body-Drain Diode Reverse Drain Current	I_{DR}	30	A
Body-Drain Diode Reverse Drain Peak Current	I_{DR}(peak)	60	A
Channel Dissipation	P_D*	200	W
Channel Temperature	Tch	150	℃
Storage Temperature	Tstg	−45～+125	℃
Insulation Dielectric	Visol**	2000	V

* Value at Tc=25℃
** Base to Terminals AC minute



Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

■ ELECTRICAL CHARACTERISTICS (Ta=25℃)

(Per FET chip)

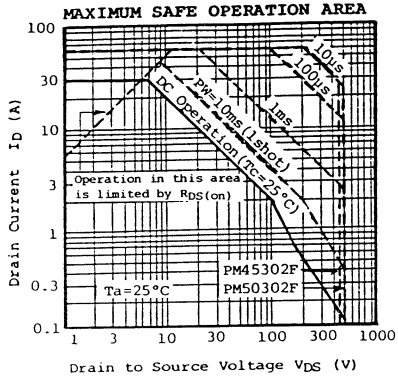
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain−Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=10mA$, $V_{GS}=0$	450	−	−	V
Gate−Source Leak Current	I_{GSS}	$V_{GS}=\pm16V$, $V_{DS}=0$	−	−	±50	μA
Gate−Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G=\pm100\mu A$, $V_{DS}=0$	±20	−	−	V
Gate Leak Current	I_{DSS}	$V_{DS}=360V$, $V_{GS}=0$	−	−	1	mA
Gate−Source Threshold Voltage	$V_{GS(th)}$	$I_D=1mA$, $V_{DS}=10V$	1.5	−	4.0	V
Drain−Source Saturation Voltage	$V_{DS(on)}$	$I_D=15A$, $V_{GS}=10V$*	−	2.0	3.0	V
Static Drain−Source On State Resistance	$R_{DS(on)}$	$I_D=15A$, $V_{GS}=10V$*	−	0.13	0.20	Ω
Forward Transfer Admittance	$\|yfs\|$	$I_D=15A$, $V_{DS}=10V$*	15	25	−	S
Input Capacitance	Ciss	$V_{DS}=10v$, $V_{GS}=0$ f=1MHz	−	6150	−	pF
Output Capacitance	Coss		−	2160	−	pF
Reverse Transfer Capacitance	Crss		−	240	−	pF
Turn−on Delay Time	td(on)	$I_D=15A$, $V_{GS}=10V$ $R_L=2\Omega$	−	100	−	ns
Rise Time	tr		−	480	−	ns
Turn−off Delay Time	td(off)		−	500	−	ns
Fall Time	tf		−	400	−	ns
Body−Drain Diode Forward Voltage	V_{DF}	$I_F=15A$, $V_{GS}=0$	−	1.2	−	V
Body−Drain Diode Reverse Recovery Time	trr	$I_F=15A$, $V_{GS}=0$ $di/dt=100A/\mu s$	−	200	−	ns

*Pulse Test

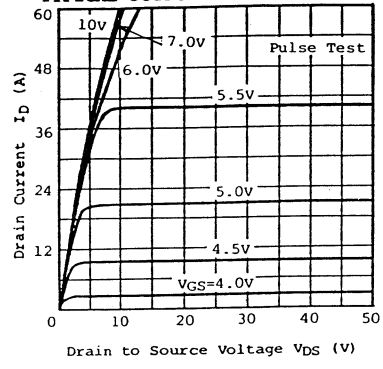
■ MECHANICAL CHARACTERISTICS

Item	Symbol	Condition	Rating	Unit
Fixing Strength	−	Mounted into main−terminal with M4 screw	15～20	kg cm
	−	Mounted into heat sink with M5 screw	15～25	kg cm
Weight	−	Typical value	220	g

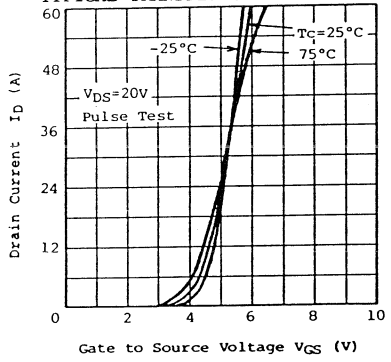
MAXIMUM SAFE OPERATION AREA



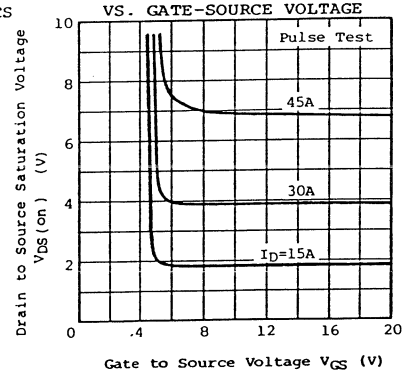
TYPICAL OUTPUT CHARACTERISTICS



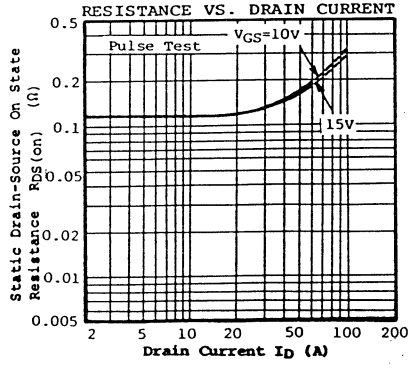
TYPICAL TRANSFER CHARACTERISTICS



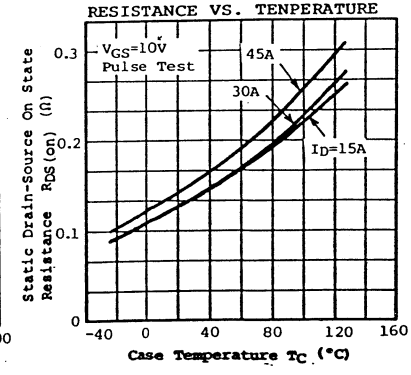
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



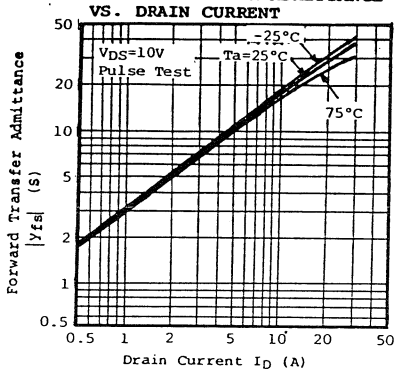
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



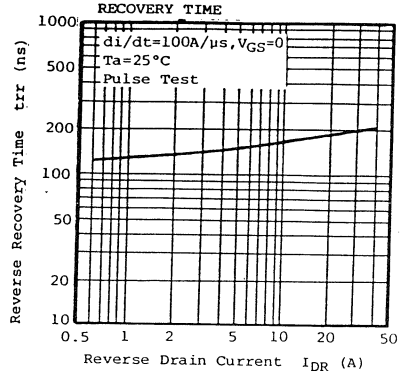
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



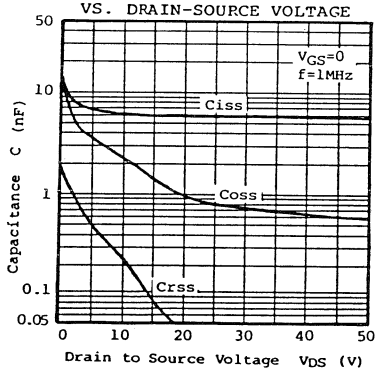
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



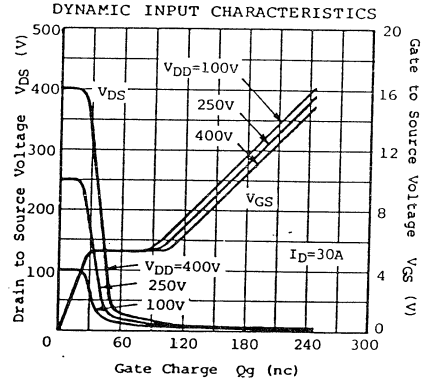
BODY-DRAIN DIODE REVERSE RECOVERY TIME



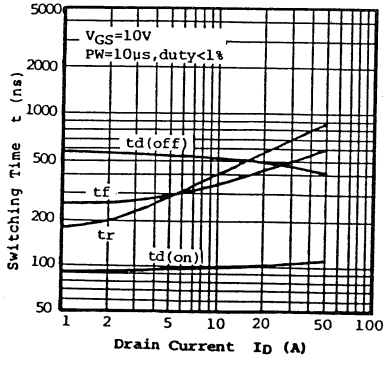
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



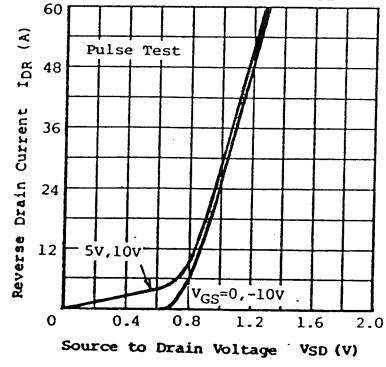
DYNAMIC INPUT CHARACTERISTICS



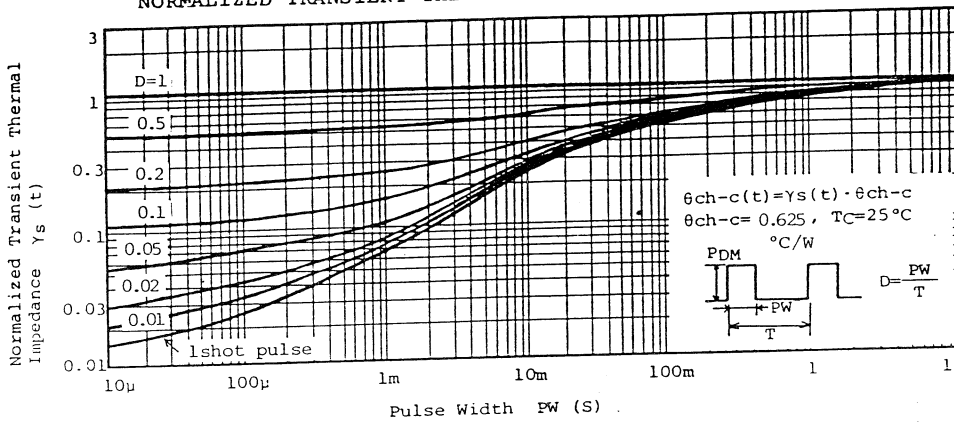
SWITCHING CHARACTERISTICS



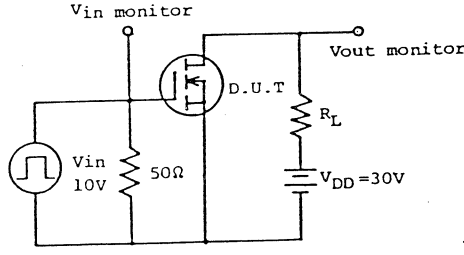
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



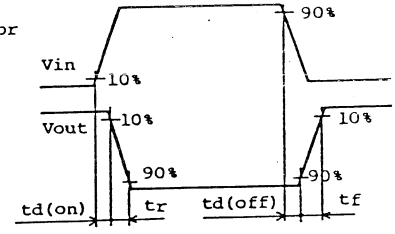
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

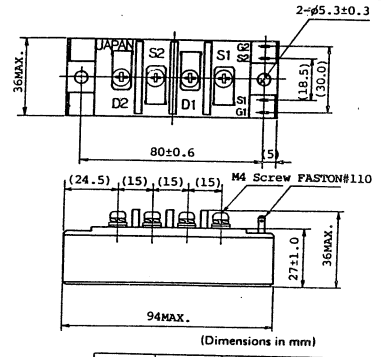
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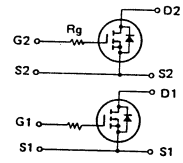
—Preliminary—

SILICON N-CHANNEL POWER MOSFET MODULE
HIGH SPEED POWER SWITCHING

■ FEATURES

- ●Power MOSFET Module
  - ・Low On-Resistance
  - ・High Speed Switching
  - ・High Efficiency, Less Driving Loss and Simple Driving Circuit
  - ・No Secondary Breakdown
- ●Inherent Parallel Diode between Source and Drain
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- ●Suitable for Switching Regulators, DC-DC Converters and Motor Drives



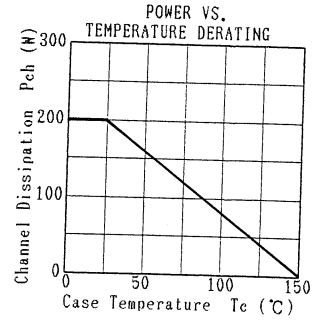


Symbol	Electrode	Terminals	Remarks
S1	Source 1	M4 Screw	Power terminals
D1	Drain 1	M4 Screw	Power terminals
S2	Source 2	M4 Screw	Power terminals
D2	Drain 2	M4 Screw	Power terminals
G1	Gate 1	#110	Signal terminals
S1	Source 1	#110	Signal terminals
G2	Gate 2	#110	Signal terminals
S2	Source 2	#110	Signal terminals

■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)
(Per FET Chip)

Item	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DSS}	500	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	30	A
Drain Peak Current	I_D(peak)	60	A
Body-Drain Diode Reverse Drain Current	I_{DR}	30	A
Body-Drain Diode Reverse Drain Peak Current	I_{DR}(peak)	60	A
Channel Dissipation	Pch*	200	W
Channel Temperature	Tch	150	℃
Storage Temperature	Tstg	−45～+125	℃
Insulation Dielectric	Visol**	2000	V

* Value at Tc=25℃
** Base to Terminals AC minute



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■ ELECTRICAL CHARACTERISTICS (Ta=25℃)

(Per FET chip)

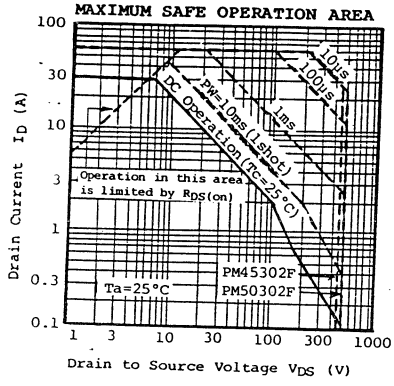
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain−Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=10mA$, $V_{GS}=0$	500	−	−	V
Gate−Source Leak Current	I_{GSS}	$V_{GS}=\pm16V$, $V_{DS}=0$	−	−	±50	μA
Gate−Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G=\pm100\mu A$, $V_{DS}=0$	±20	−	−	V
Gate Leak Current	I_{DSS}	$V_{DS}=400V$, $V_{GS}=0$	−	−	1	mA
Gate−Source Threshold Voltage	$V_{GS}(th)$	$I_D=1mA$, $V_{DS}=10V$	1.5	−	4.0	V
Drain−Source Saturation Voltage	$V_{DS(on)}$	$I_D=15A$, $V_{GS}=10V$*	−	2.25	3.0	V
Static Drain−Source On State Resistance	$R_{DS(on)}$	$I_D=15A$, $V_{GS}=10V$*	−	0.15	0.20	Ω
Forward Transfer Admittance	$\|yfs\|$	$I_D=15A$, $V_{DS}=10V$*	15	25	−	S
Input Capacitance	Ciss	$V_{DS}=10v$, $V_{GS}=0$ f=1MHz	−	6150	−	pF
Output Capacitance	Coss		−	2160	−	pF
Reverse Transfer Capacitance	Crss		−	240	−	pF
Turn−on Delay Time	td(on)	$I_D=15A$, $V_{GS}=10V$ $R_L=2\Omega$	−	100	−	ns
Rise Time	tr		−	480	−	ns
Turn−off Delay Time	td(off)		−	500	−	ns
Fall Time	tf		−	400	−	ns
Body−Drain Diode Forward Voltage	V_{DF}	$I_F=15A$, $V_{GS}=0$	−	1.2	−	V
Body−Drain Diode Reverse Recovery Time	trr	$I_F=15A$, $V_{GS}=0$ $di/dt=100A/\mu s$	−	200	−	ns

*Pulse Test

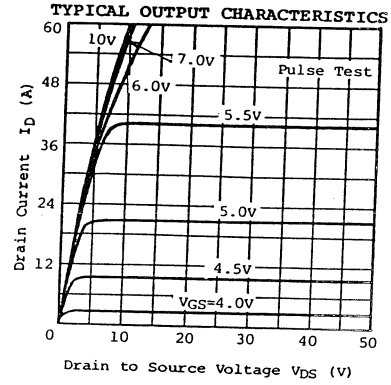
■ MECHANICAL CHARACTERISTICS

Item	Symbol	Condition	Rating	Unit
Fixing Strength	−	Mounted into main−terminal with M4 screw	15～20	kg•cm
	−	Mounted into heat sink with M5 screw	15～25	kg•cm
Weight	−	Typical value	220	g

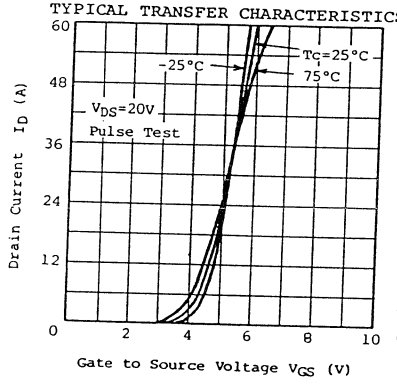
MAXIMUM SAFE OPERATION AREA



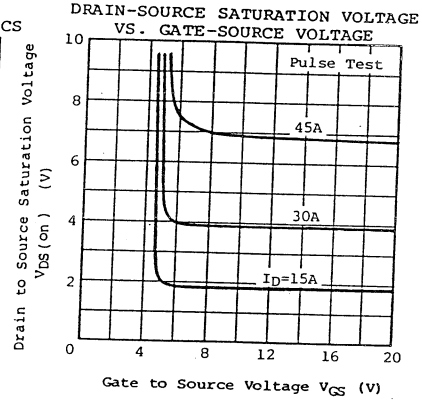
TYPICAL OUTPUT CHARACTERISTICS



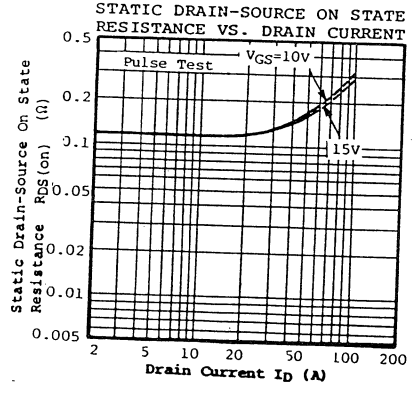
TYPICAL TRANSFER CHARACTERISTICS



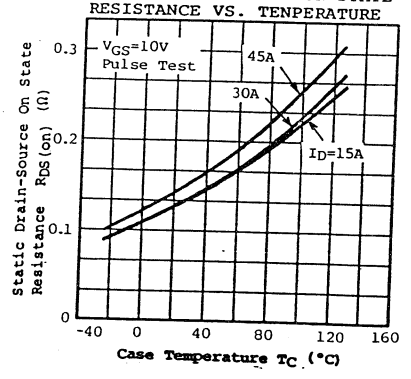
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



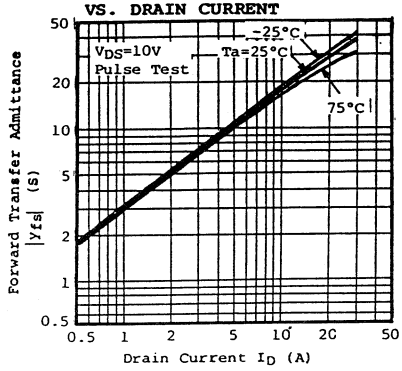
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



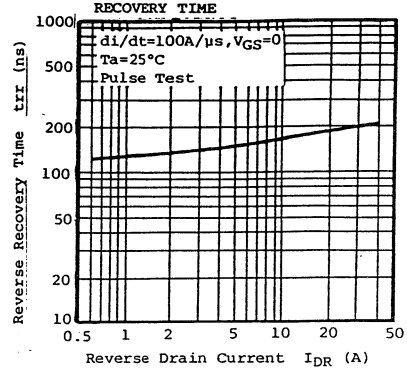
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



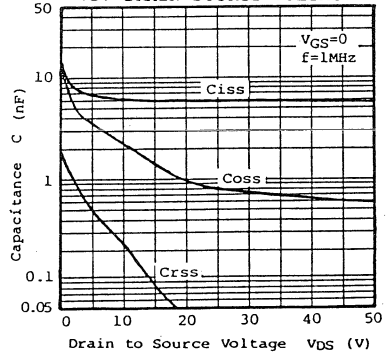
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



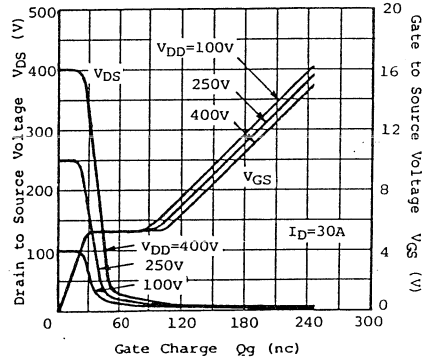
BODY-DRAIN DIODE REVERSE RECOVERY TIME



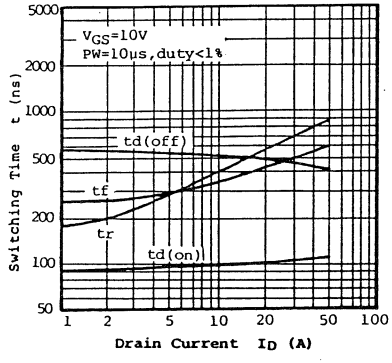
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



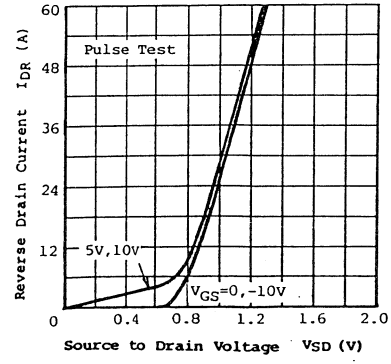
DYNAMIC INPUT CHARACTERISTICS



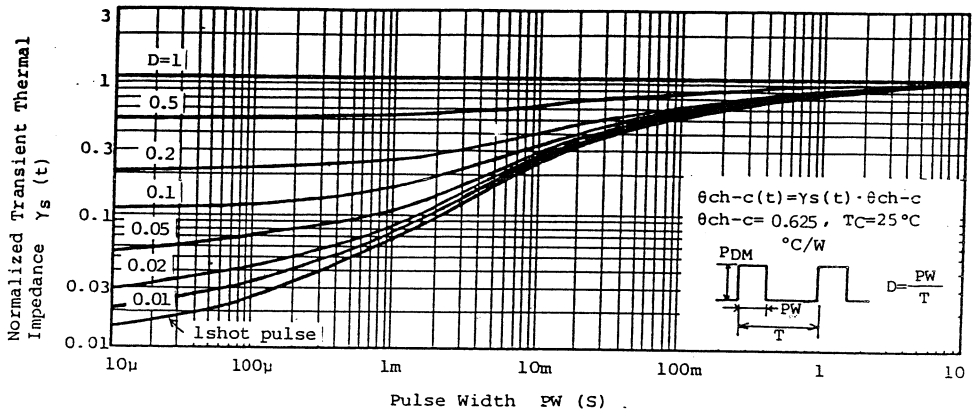
SWITCHING CHARACTERISTICS



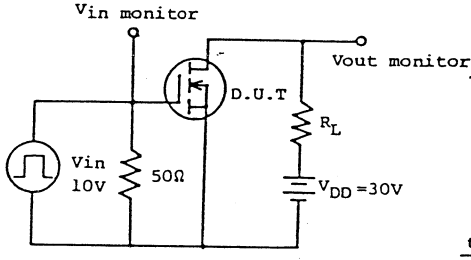
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



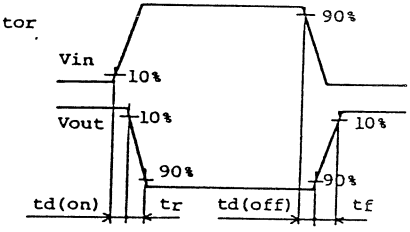
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

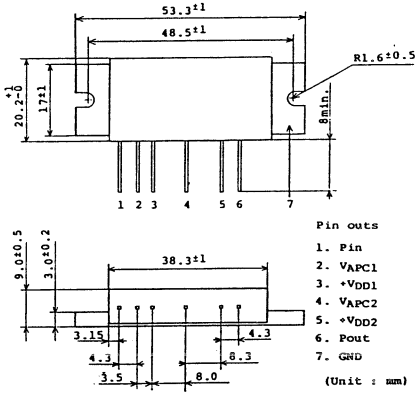
PF0008

—Preliminary—

MOSFET POWER AMPLIFIER
UHF BAND

■ FEATURES:

1. Included input and output matching circuit.
2. Easy to control output power.
3. Superior to stability at load mismatching.



■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	17	V
Maximum Circuit Current	I_D	3.0	A
APC Voltage	V_{APC}	±8	V
Maximum Input Power	Pin	30	mW
Operating Maximum Case Temperature	$T_{C(op)}$	0 ~ +80	℃
Storage Temperature	Tstg	−10 ~ +100	℃

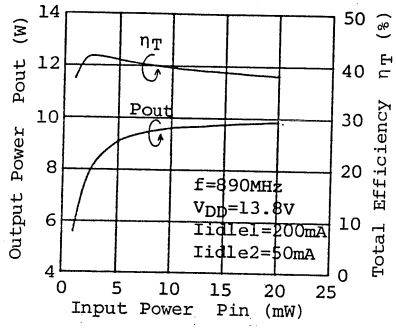
■ ELECTRICAL CHARACTERISTICS (Ta=25℃)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	$V_{DD1}=V_{DD2}=17V$, $V_{APC1}=V_{APC2}=0$	—	—	500	μA
Output Power	Pout	f=865,890MHz,	8.0	9.0	—	W
Total Efficiency	$\eta_T(1)$	Pin=10mW,	35	40	—	%
2nd Harmonic Distortion	2nd H.D.	$V_{DD1}=V_{DD2}=13.8V$,	—	−50	−30	dB
3rd Harmonic Distortion	3rd H.D.	$Iidle_1$=200mA,	—	−40	−30	dB
Input VSWR	VSWR(in)	$Iidle_2$=50mA,	—	1.5	3.0	—
Output VSWR	VSWR(out)	Zin=Zout=50Ω	—	1.5	—	—
Total Efficiency	$\eta_T(2)$	f=865,890MHz, Pin=10mW, Pout=8W(at APC Control) Zin=Zout=50Ω	35	40	—	%
Stability	—	$V_{DD1}=V_{DD2}=13.8V$, Pin=10mW, f=865MHz, Pout=8W(at APC Control), Rg=50Ω, Output VSWR=∞ All Phase, t=20sec	No Parastic Oscillation			—

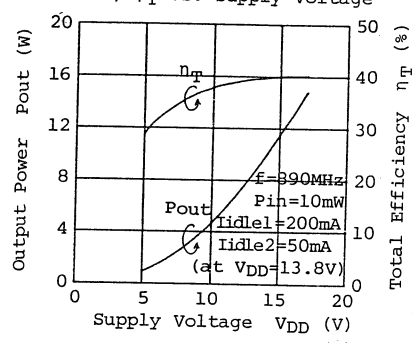
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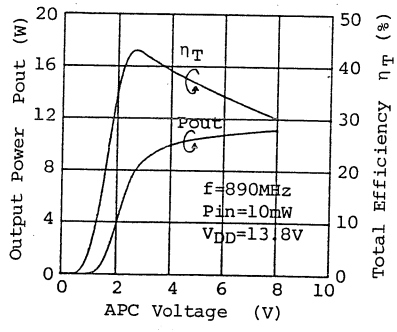
Pout, η_T vs. Input Power



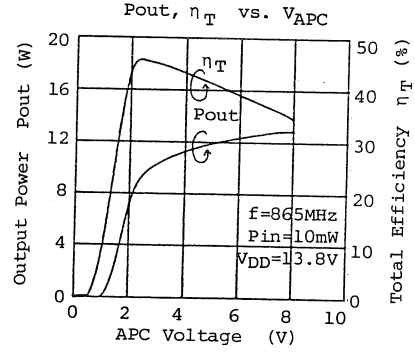
Pout, η_T vs. Supply Voltage



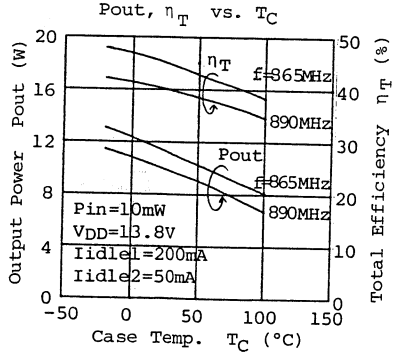
Pout, η_T vs. V_{APC}



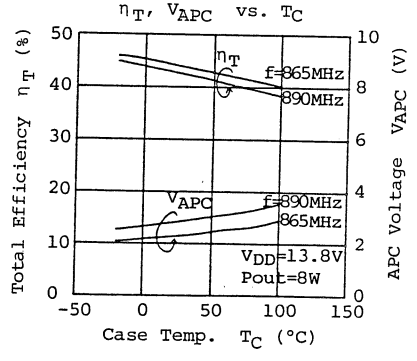
Pout, η_T vs. V_{APC}

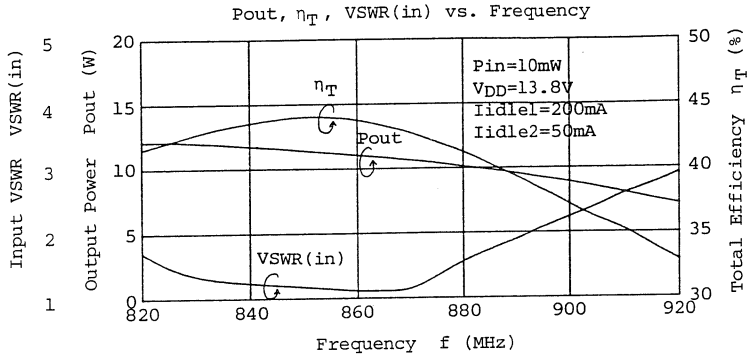


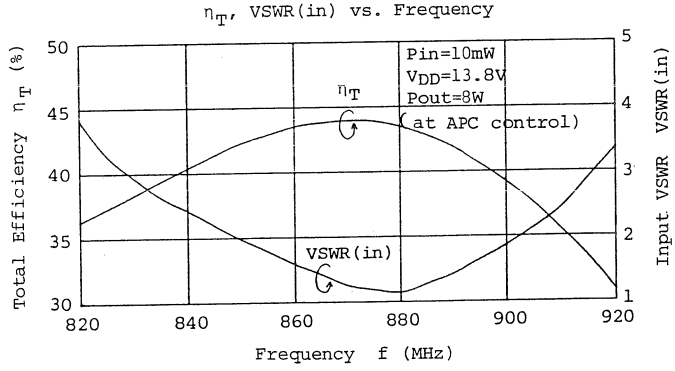
Pout, η_T vs. T_C



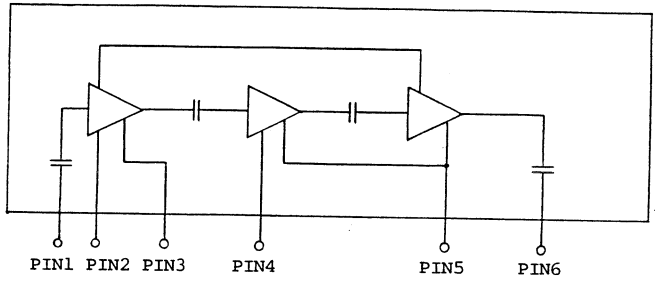
η_T, V_{APC} vs. T_C



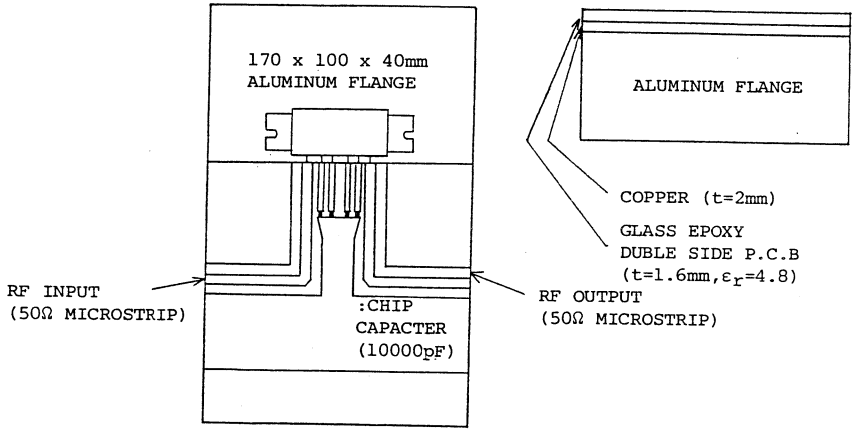

Pout, ηT , VSWR(in) vs. Frequency
Input VSWR VSWR(in)
Output Power Pout (W)
Total Efficiency ηT (%)
Pin=10mW
VDD=13.8V
Iidle1=200mA
Iidle2=50mA
ηT
Pout
VSWR(in)
Frequency f (MHz)


ηT, VSWR(in) vs. Frequency
Total Efficiency ηT (%)
Input VSWR VSWR(in)
Pin=10mW
VDD=13.8V
Pout=8W
(at APC control)
ηT
VSWR(in)
Frequency f (MHz)

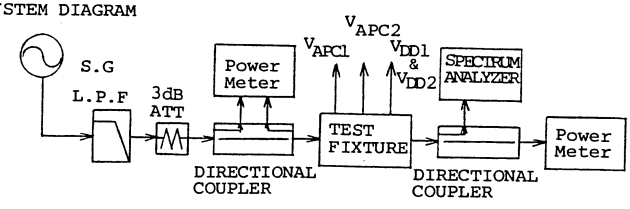
■ INTERNAL DIAGRAM



■ TEST FIXTURE



■ TEST SYSTEM DIAGRAM



NEW PRODUCT

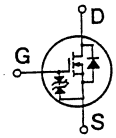
POWER MOS FET DII SERIES

2SK1199
(HS76117)

SILICON N CHANNEL MOS FET

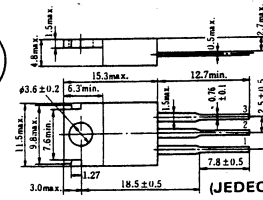
—Preliminary—

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

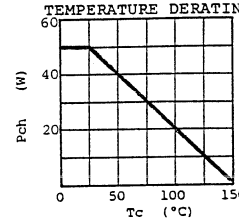
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	900	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	2	A
Drain Peak Current	$I_{D(pulse)}$*	6	A
Body-Drain Diode Reverse Drain Current	I_{DR}	2	A
Channel Dissipation	Pch**	50	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55～+150	°C

*PW≤10us, duty cycle≤1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

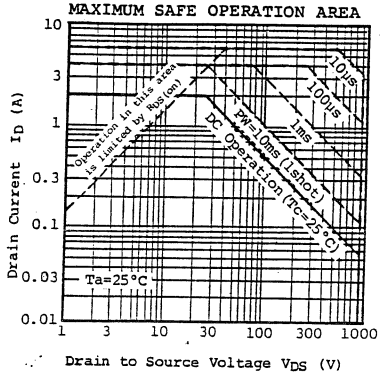
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	900	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100uA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=720V, V_{GS}=0	-	-	250	uA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=1A, V_{GS}=10V *	-	5.0	7.0	Ω
Foward Transfer Admittance	|yfs|	I_D=1A, V_{DS}=20V *	0.6	1.0	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz	-	490	-	pF
Output Capacitance	Coss		-	260	-	pF
Reverse Transfer Capacitance	Crss		-	190	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=1A, V_{GS}=10V R_L=30Ω	-	10	-	ns
Rise Time	t_r		-	60	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	65	-	ns
Fall Time	t_f		-	60	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=2A, V_{GS}=0	-	0.9	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=2A, V_{GS}=0 dIF/dt=100A/us	-	800	-	ns

*Pulse Test

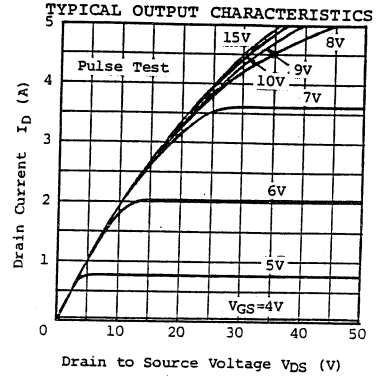
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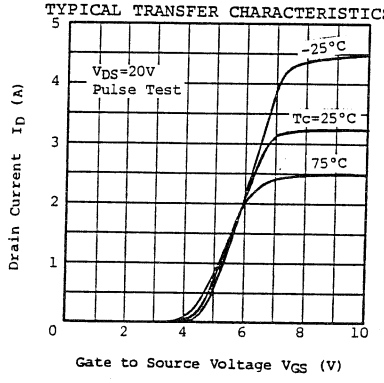
MAXIMUM SAFE OPERATION AREA



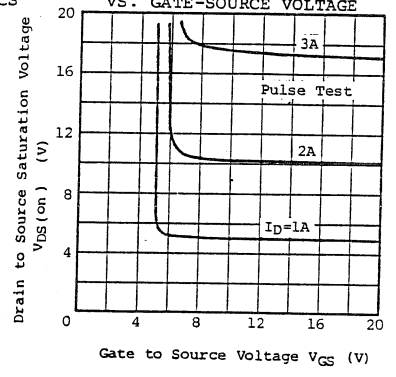
TYPICAL OUTPUT CHARACTERISTICS



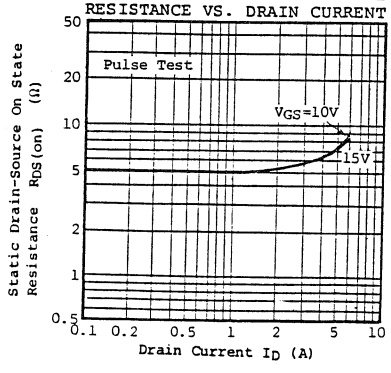
TYPICAL TRANSFER CHARACTERISTICS



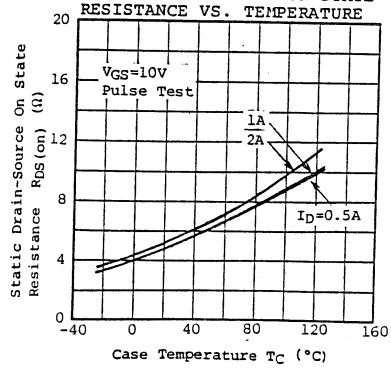
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



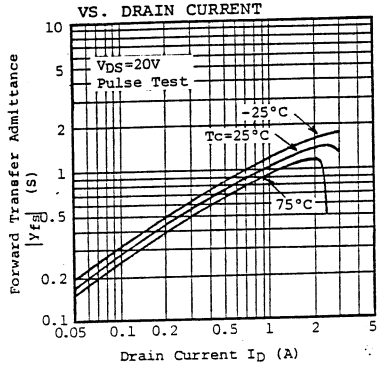
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



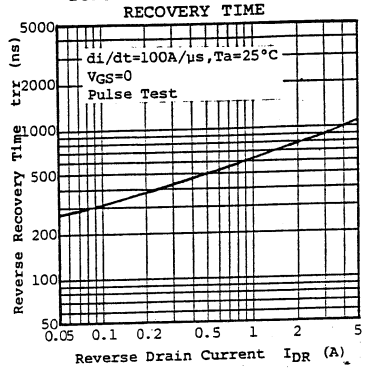
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



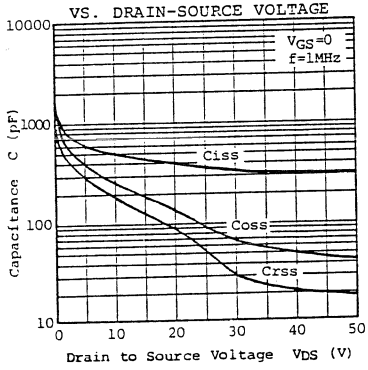
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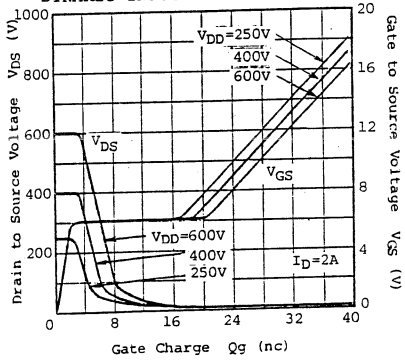
BODY-DRAIN DIODE REVERSE RECOVERY TIME



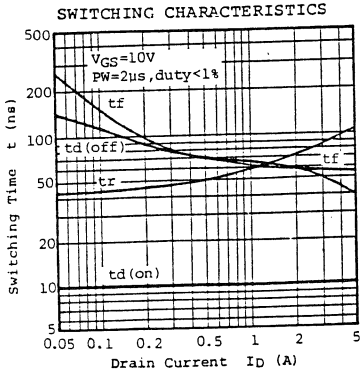
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



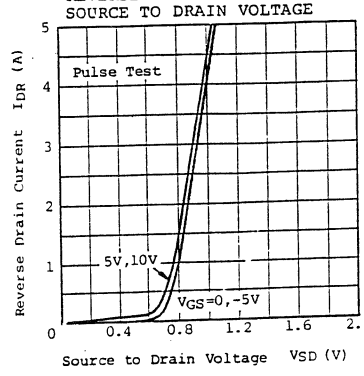
DYNAMIC INPUT CHARACTERISTICS



SWITCHING CHARACTERISTICS

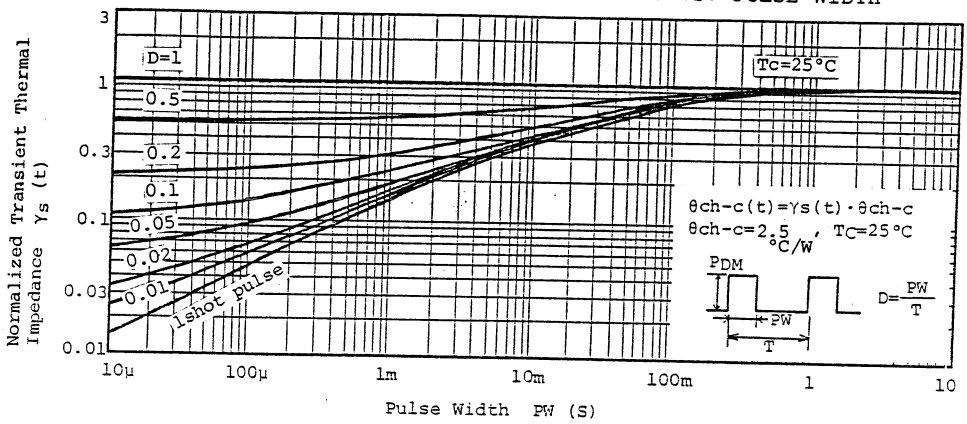


REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE

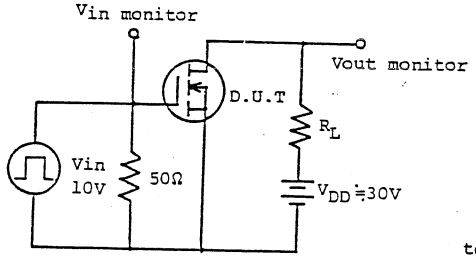


2SK1199
(HS76117)

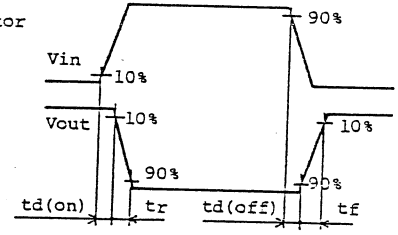
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

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HITACHI

1988.4.20
T-22-B-DS553-O

NEW PRODUCT

POWER MOS FET DII SERIES

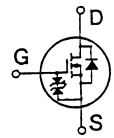
2SK1200
(HS78137)

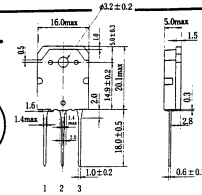
SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING

–Preliminary–

Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

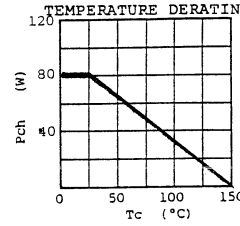
(TO-3P)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	900	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	3	A
Drain Peak Current	$I_{D(pulse)}$*	7	A
Body-Drain Diode Reverse Drain Current	I_{DR}	3	A
Channel Dissipation	Pch**	80	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 ~+150	°C

*PW≤10us, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

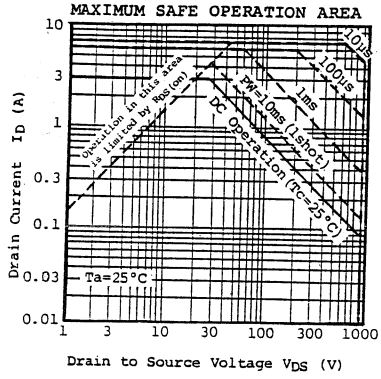
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	900	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=720V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=2A , V_{GS}=10V *	-	5.5	7.0	Ω
Foward Transfer Admittance	|yfs|	I_D=2A , V_{DS}=20V *	0.85	1.4	-	S
Input Capacitance	Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	490	-	pF
Output Capacitance	Coss		-	260	-	pF
Reverse Transfer Capacitance	Crss		-	190	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D= 2A , V_{GS}=10V R_L=15Ω	-	10	-	ns
Rise Time	t_r		-	70	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	60	-	ns
Fall Time	t_f		-	60	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F= 3A , V_{GS}=0	-	0.95	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F= 3A , V_{GS}=0 dI_F/dt=100A/μs	-	900	-	ns

*Pulse Test

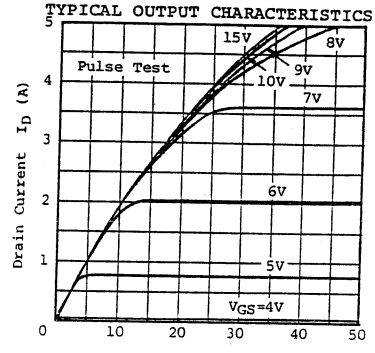
NOTICE:
The example of an applied circuit or combination with other equipment shown herein indicates characteristics and performance of semiconductor-applied products.
The company shall assume no responsibility for any problem involving a patent caused when applying the descriptions in the example.

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

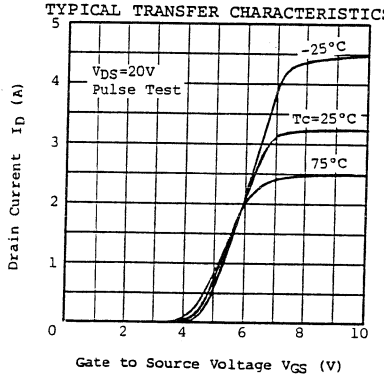
MAXIMUM SAFE OPERATION AREA



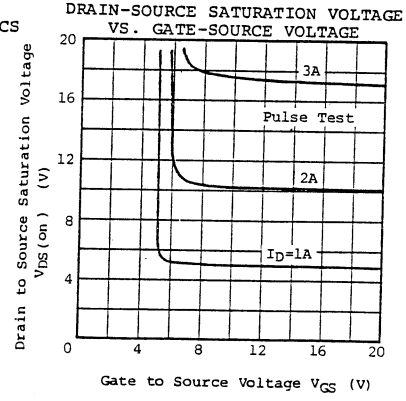
TYPICAL OUTPUT CHARACTERISTICS



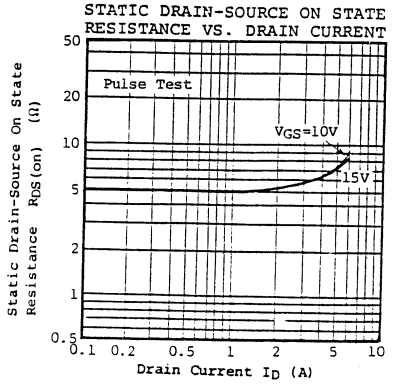
TYPICAL TRANSFER CHARACTERISTICS



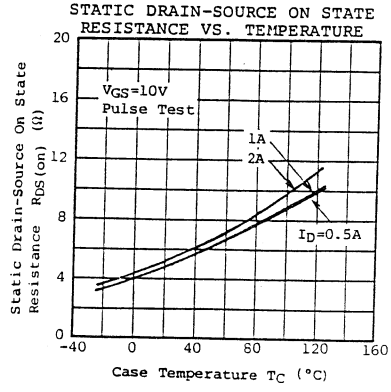
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



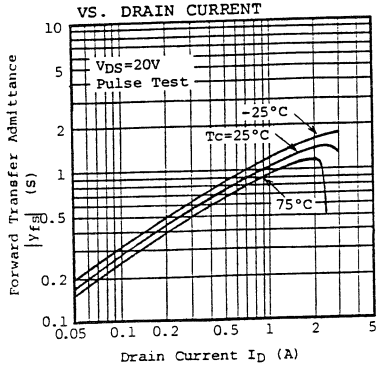
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



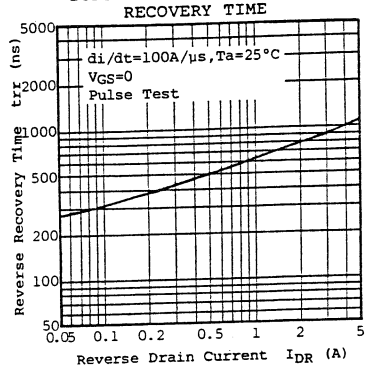
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



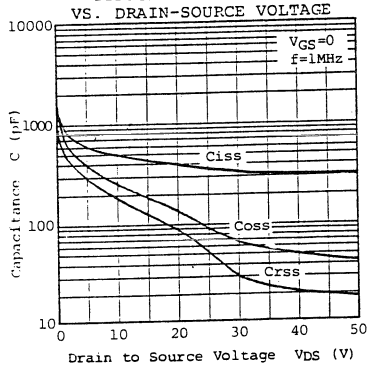
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



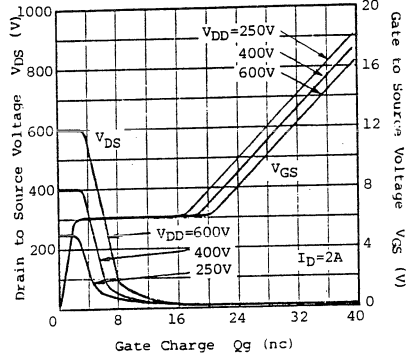
BODY-DRAIN DIODE REVERSE RECOVERY TIME



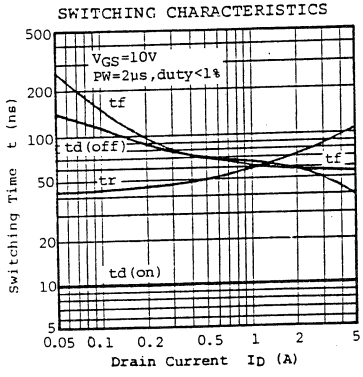
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



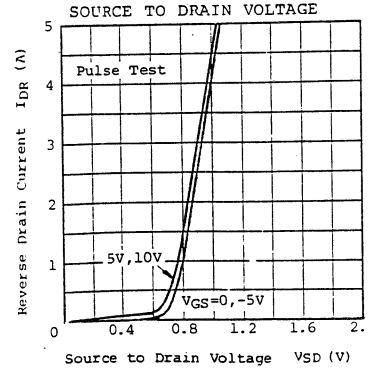
DYNAMIC INPUT CHARACTERISTICS



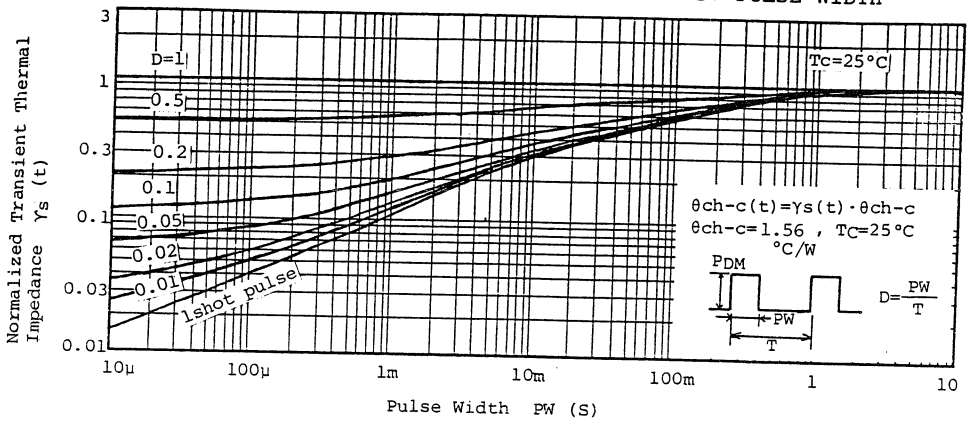
SWITCHING CHARACTERISTICS



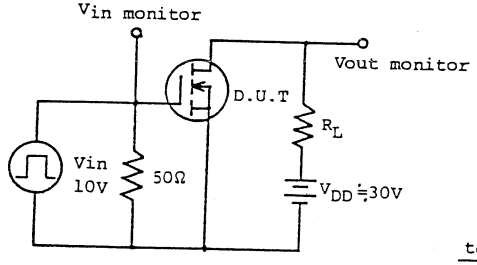
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



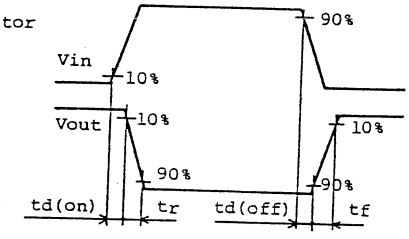
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



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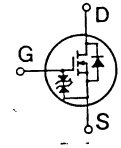
NEW PRODUCT

POWER MOS FET DII SERIES

2SK1201
(HS78149)

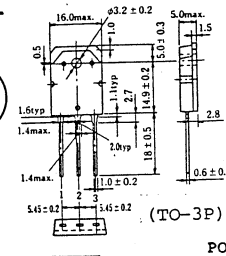
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.



(TO-3P)

—Preliminary—

1. Gate
2. Drain (Flange)
3. Source

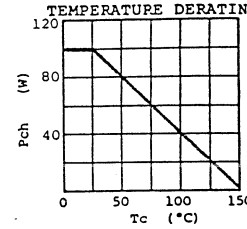
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	900	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	4	A
Drain Peak Current	$I_{D(pulse)}$*	10	A
Body-Drain Diode Reverse Drain Current	I_{DR}	4	A
Channel Dissipation	Pch**	100	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 ~ +150	°C

*PW≤10μs, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	900	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=720V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=2A, V_{GS}=10V *	-	4.0	5.5	Ω
Foward Transfer Admittance	$\|yfs\|$	I_D=2A, V_{DS}=20V *	1.1	1.7	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz	-	620	-	pF
Output Capacitance	Coss		-	350	-	pF
Reverse Transfer Capacitance	Crss		-	240	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=2A, V_{GS}=10V R_L=15Ω	-	10	-	ns
Rise Time	t_r		-	95	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	80	-	ns
Fall Time	t_f		-	75	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=4A, V_{GS}=0	-	1.0	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=4A, V_{GS}=0 dIF/dt=100A/μs	-	800	-	ns

*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

NEW PRODUCT

POWER MOS FET DII SERIES

2SK1202
(HS78139)

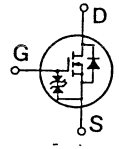
SILICON N CHANNEL MOS FET

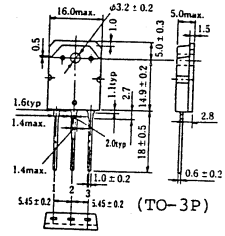
HIGH SPEED POWER SWITCHING

—Preliminary—

Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.





(TO-3P)

1. Gate
2. Drain (Flange)
3. Source

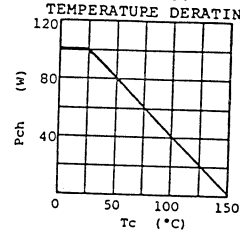
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	900	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	5	A
Drain Peak Current	$I_{D(pulse)}$*	12	A
Body-Drain Diode Reverse Drain Current	I_{DR}	5	A
Channel Dissipation	Pch**	100	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 ~ +150	°C

*PW≤10μs, duty cycle≤1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	900	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=720V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=3A, V_{GS}=10V *	-	3.0	4.0	Ω
Foward Transfer Admittance	$\|yfs\|$	I_D=3A, V_{DS}=20V *	1.5	2.4	-	S
Input Capacitance	Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	880	-	pF
Output Capacitance	Coss		-	490	-	pF
Reverse Transfer Capacitance	Crss		-	340	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=3A, V_{GS}=10V R_L=10Ω	-	15	-	ns
Rise Time	t_r		-	120	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	100	-	ns
Fall Time	t_f		-	95	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=5A, V_{GS}=0	-	1.0	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=5A, V_{GS}=0 dI_F/dt=100A/μs	-	800	-	ns

*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

HITACHI

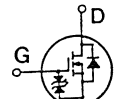
NEW PRODUCT

POWER MOS FET DII SERIES

2SK1203
(HS78141)

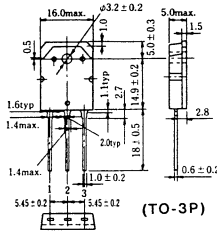
SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING

—Preliminary—



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
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(TO-3P)

1. Gate
2. Drain (Flange)
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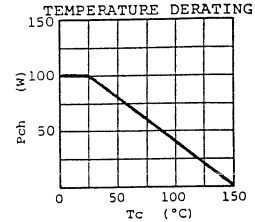
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	900	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	6	A
Drain Peak Current	$I_{D(pulse)}$*	15	A
Body-Drain Diode Reverse Drain Current	I_{DR}	6	A
Channel Dissipation	Pch**	100	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55～+150	°C

*PW≤10μs, duty cycle≤1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



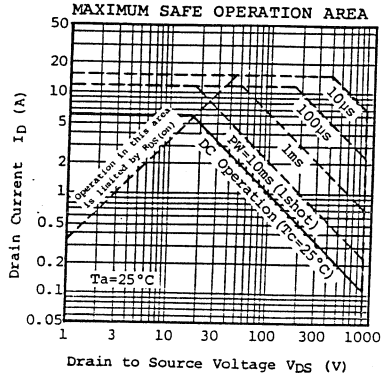
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	900	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=720V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=3A, V_{GS}=10V *	-	2.0	3.0	Ω
Foward Transfer Admittance	|yfs|	I_D=3A, V_{DS}=20V *	1.5	2.5	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz	-	1150	-	pF
Output Capacitance	Coss		-	640	-	pF
Reverse Transfer Capacitance	Crss		-	440	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=3A, V_{GS}=10V R_L=10Ω	-	15	-	ns
Rise Time	t_r		-	150	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	130	-	ns
Fall Time	t_f		-	120	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=6A, V_{GS}=0	-	1.0	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=6A, V_{GS}=0 dIF/dt=100A/μs	-	1100	-	ns

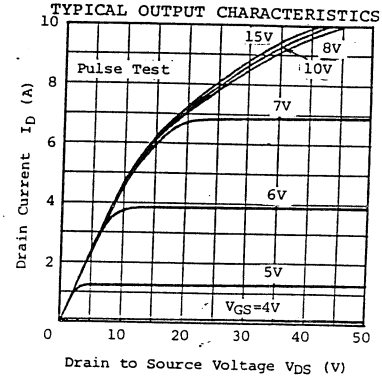
*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

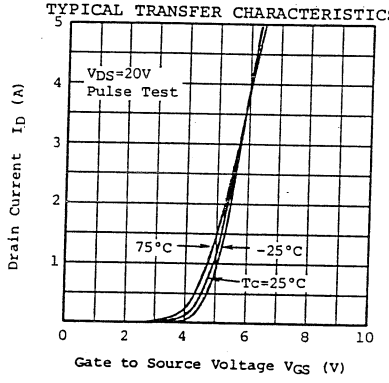
MAXIMUM SAFE OPERATION AREA



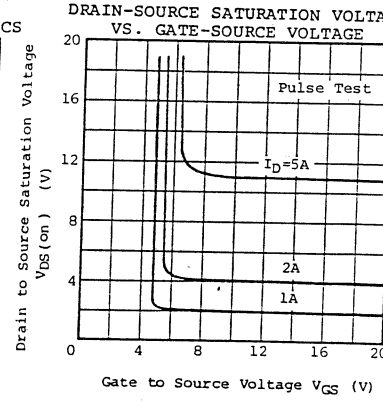
TYPICAL OUTPUT CHARACTERISTICS



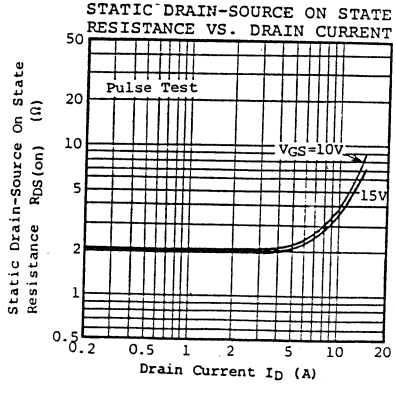
TYPICAL TRANSFER CHARACTERISTICS



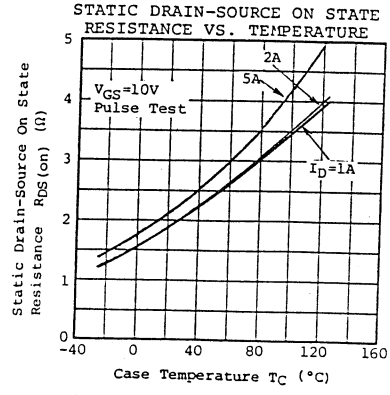
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



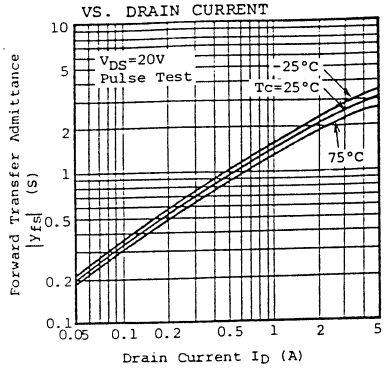
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



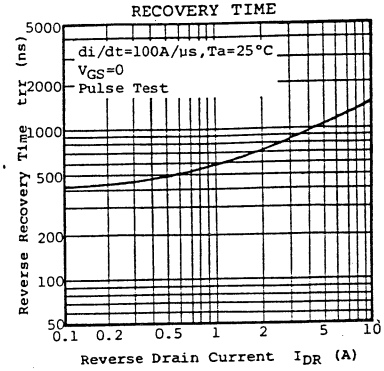
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



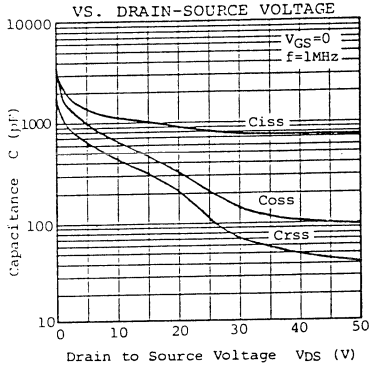
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



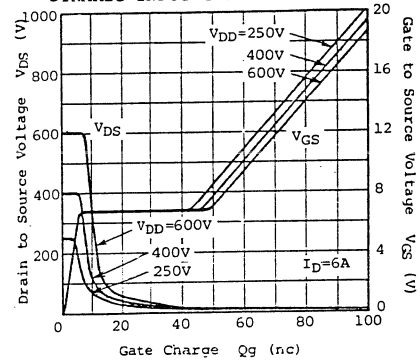
BODY-DRAIN DIODE REVERSE RECOVERY TIME



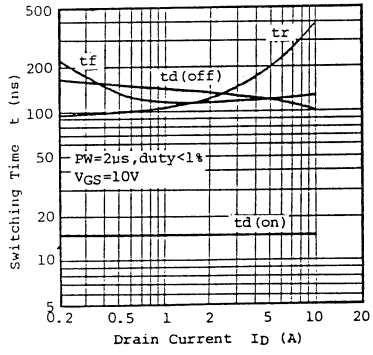
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



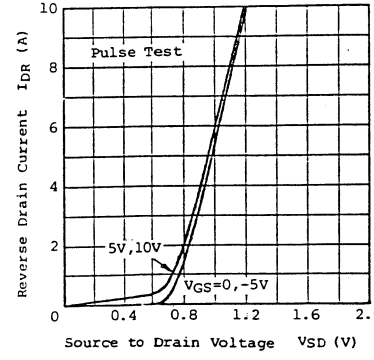
DYNAMIC INPUT CHARACTERISTICS



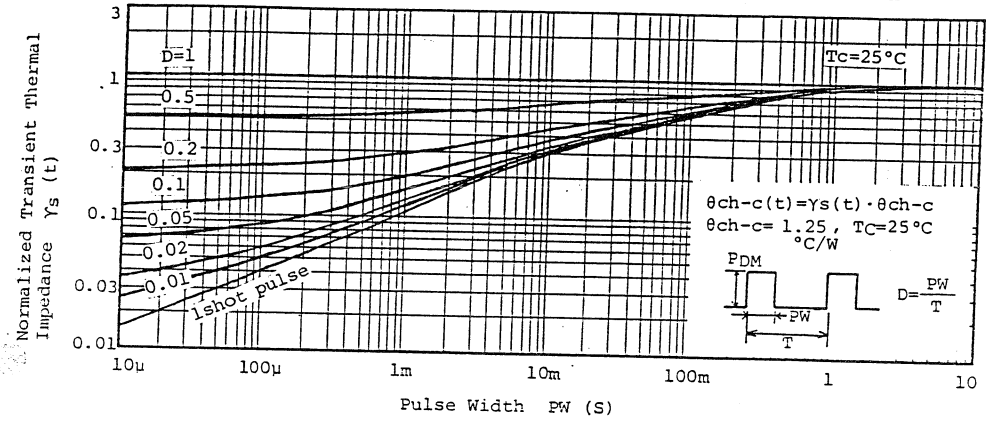
SWITCHING CHARACTERISTICS



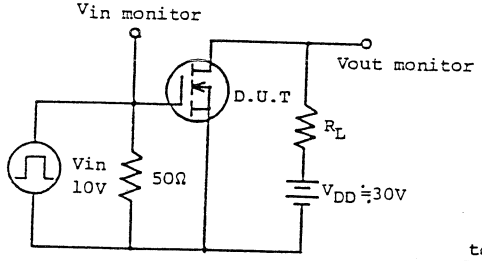
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



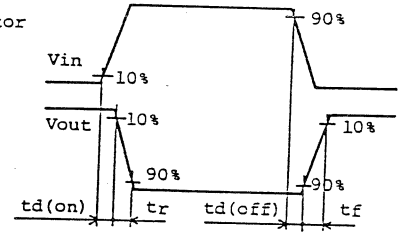
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

注1) ゲート•ソース間に内蔵のツェナーダイオードは、種々の条件下において完全にゲートの静電破壊を防止できるものではありません。このため素子を取扱う場合、人体や半田ゴテなどにアースを接続していただくようお願いいたします。

NEW PRODUCT

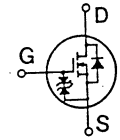
POWER MOS FET DII SERIES

2SK1204
(HS78143)

SILICON N CHANNEL MOS FET

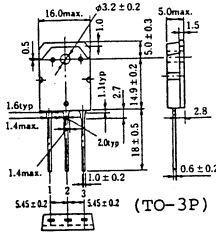
—Preliminary—

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.



(TO-3P)

1. Gate
2. Drain (Flange)
3. Source

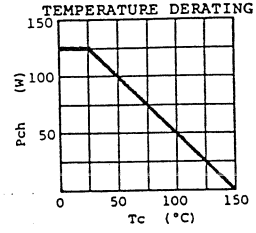
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	900	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Drain Peak Current	$I_{D(pulse)}$*	20	A
Body-Drain Diode Reverse Drain Current	I_{DR}	8	A
Channel Dissipation	Pch**	120	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 ~ +150	°C

*PW≤10μs, duty cycle≤1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	900	-	-	V
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate-Source Leak Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=720V, V_{GS}=0	-	-	250	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	4.0	V
Static Drain-Source on State Resistance	$R_{DS(on)}$	I_D=4A, V_{GS}=10V *	-	1.2	1.6	Ω
Foward Transfer Admittance	|yfs|	I_D=4A, V_{DS}=20V *	2.5	4.0	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz	-	1800	-	pF
Output Capacitance	Coss		-	1150	-	pF
Reverse Transfer Capacitance	Crss		-	730	-	pF
Turn-On Delay Time	$t_{d(on)}$	I_D=4A, V_{GS}=10V R_L=7.5Ω	-	20	-	ns
Rise Time	t_r		-	210	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	220	-	ns
Fall Time	t_f		-	210	-	ns
Body-Drain Diode Forward Voltage	V_{DF}	I_F=8A, V_{GS}=0	-	1.1	-	V
Body-Drain Diode Reverse Recovery Time	t_{rr}	I_F=8A, V_{GS}=0 dI_F/dt=100A/μs	-	1000	-	ns

*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

NEW PRODUCT

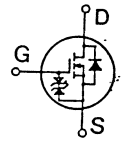
POWER MOS FET DII SERIES

2SK1151, 2SK1152
(HS72025) (HS72025A)

SILICON N CHANNEL MOS FET

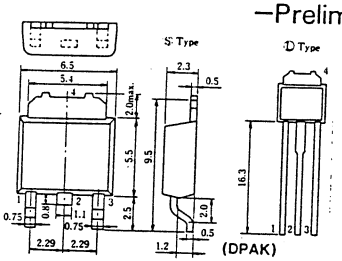
—Preliminary—

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.



1. Gate
2. Drain
3. Source
4. Drain

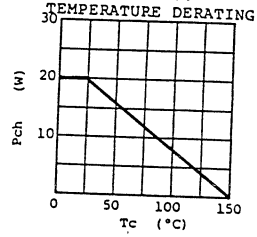
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	72025	72025A	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±30		V
Drain Current	I_D	1.5		A
Drain Peak Current	$I_{D(pulse)}$*	6		A
Body-Drain Diode Reverse Drain Current	I_{DR}	1.5		A
Channel Dissipation	Pch**	20		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	-55 ~ +150		°C

*PW≤10μs, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	72025	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	-	-	V
	72025A			500	-	-	
Gate-Source Leak Current		I_{GSS}	V_{GS}=±25V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	72025	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	100	μA
	72025A		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	3.0	V
Static Drain-Source on State Resistance	72025	$R_{DS(on)}$	I_D=1A, V_{GS}=10V *	-	3.5	5.5	Ω
	72025A			-	4.0	6.0	
Foward Transfer Admittance		$\|Yfs\|$	I_D=1A, V_{DS}=20V *	0.6	1.0	-	S
Input Capacitance		Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	160	-	pF
Output Capacitance		Coss		-	45	-	pF
Reverse Transfer Capacitance		Crss		-	8	-	pF
Turn-On Delay Time		$t_{d(on)}$	I_D=1A, V_{GS}=10V, R_L=30Ω	-	6	-	ns
Rise Time		t_r		-	20	-	ns
Turn-Off Delay Time		$t_{d(off)}$		-	25	-	ns
Fall Time		t_f		-	20	-	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=1.5A, V_{GS}=0	-	1.0	-	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=1.5A, V_{GS}=0 dIF/dt=100A/μs	-	250	-	ns

*Pulse Test

*Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

HITACHI

NEW PRODUCT

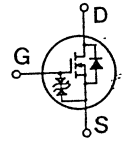
POWER MOS FET DIII SERIES

HS7025/A

—Preliminary—

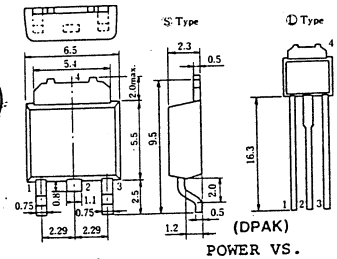
SILICON N CHANNEL MOS FET

HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.



1. Gate
2. Drain
3. Source
4. Drain

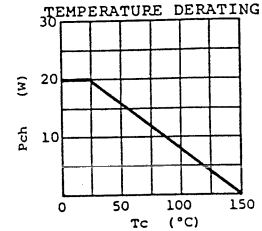
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	72025	72025A	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±30		V
Drain Current	I_D	1.5		A
Drain Peak Current	$I_{D(pulse)}$*	6		A
Body-Drain Diode Reverse Drain Current	I_{DR}	1.5		A
Channel Dissipation	Pch**	20		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	−55 ~ +150		°C

*PW≤10μs, duty cycle≤1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	72025	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	–	–	V
	72025A			500	–	–	
Gate-Source Leak Current		I_{GSS}	V_{GS}=±25V, V_{DS}=0	–	–	±10	μA
Zero Gate Voltage Drain Current	72025	I_{DSS}	V_{DS}=360V, V_{GS}=0	–	–	100	μA
	72025A		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	–	3.0	V
Static Drain-Source on State Resistance	72025	$R_{DS(on)}$	I_D=1A, V_{GS}=10V *	–	3.5	5.5	Ω
	72025A			–	4.0	6.0	
Foward Transfer Admittance		$\|yfs\|$	I_D=1A, V_{DS}=20V *	0.6	1.0	–	S
Input Capacitance		Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	–	160	–	pF
Output Capacitance		Coss		–	45	–	pF
Reverse Transfer Capacitance		Crss		–	8	–	pF
Turn-On Delay Time		$t_{d(on)}$	I_D=1A, V_{GS}=10V, R_L=30Ω	–	6	–	ns
Rise Time		t_r		–	20	–	ns
Turn-Off Delay Time		$t_{d(off)}$		–	25	–	ns
Fall Time		t_f		–	20	–	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=1.5A, V_{GS}=0	–	1.0	–	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=1.5A, V_{GS}=0 dIF/dt=100A/μs	–	250	–	ns

*Pulse Test

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

NEW PRODUCT

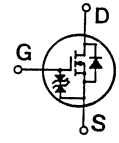
POWER MOS FET DⅢ-H SERIES

2SK1153, 2SK1154
(HS76079) (HS76079A)

SILICON N CHANNEL MOS FET

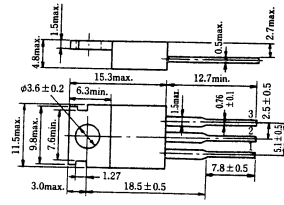
HIGH SPEED POWER SWITCHING

—Preliminary—



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

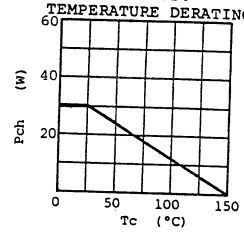
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	K1153	K1154	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±30		V
Drain Current	I_D	3		A
Drain Peak Current	$I_{D(pulse)}$*	12		A
Body-Drain Diode Reverse Drain Current	I_{DR}	3		A
Channel Dissipation	Pch**	30		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	-55～+150		°C

*PW≤10μs, duty cycle≤1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

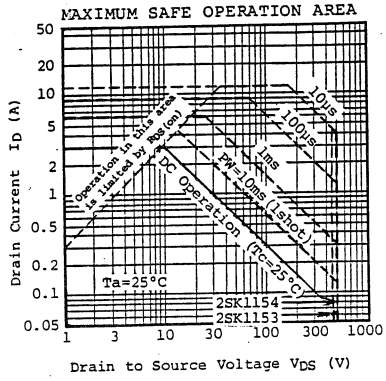
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	K1153	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	450	-	-	V
	K1154			500	-	-	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±30	-	-	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±25V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	K1153	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	250	μA
	K1154		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	2.0	-	3.0	V
Static Drain-Source on State Resistance	K1153	$R_{DS(on)}$	I_D=2A , V_{GS}=10V *	-	2.0	2.8	Ω
	K1154			-	2.2	3.0	
Foward Transfer Admittance		|yfs|	I_D=2A , V_{DS}=10V *	1.5	2.5	-	S
Input Capacitance		Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	330	-	pF
Output Capacitance		Coss		-	90	-	pF
Reverse Transfer Capacitance		Crss		-	15	-	pF
Turn-On Delay Time		$t_{d(on)}$	I_D= 2A , V_{GS}= 10V, R_L= 15Ω	-	7	-	ns
Rise Time		t_r		-	20	-	ns
Turn-Off Delay Time		$t_{d(off)}$		-	30	-	ns
Fall Time		t_f		-	20	-	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F= 3A , V_{GS}=0	-	0.9	-	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F= 3A , V_{GS}=0 dI_F/dt=100A/μs	-	300	-	ns

*Pulse Test

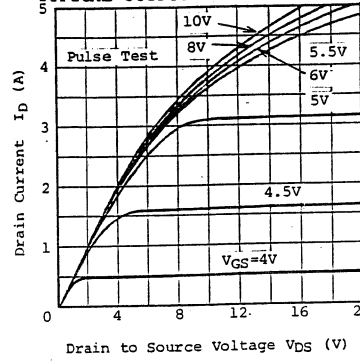
NOTICE:
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Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

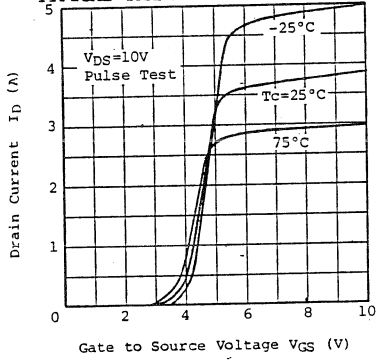
MAXIMUM SAFE OPERATION AREA



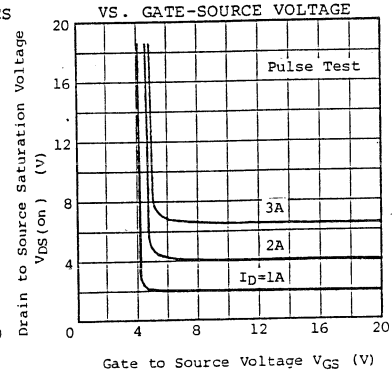
TYPICAL OUTPUT CHARACTERISTICS



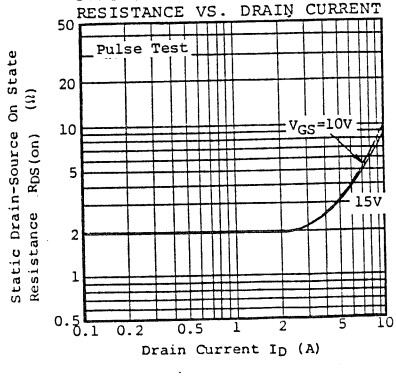
TYPICAL TRANSFER CHARACTERISTICS



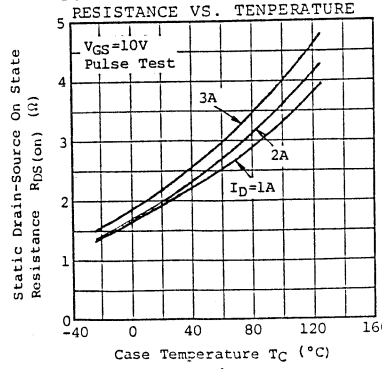
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



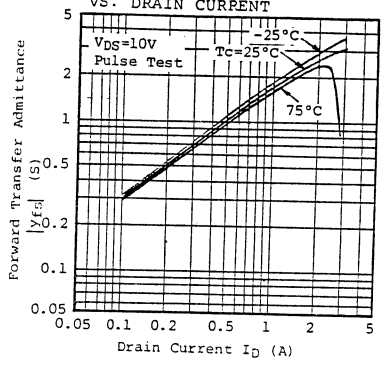
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



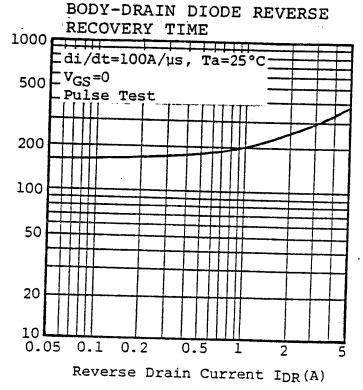
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TENPERATURE



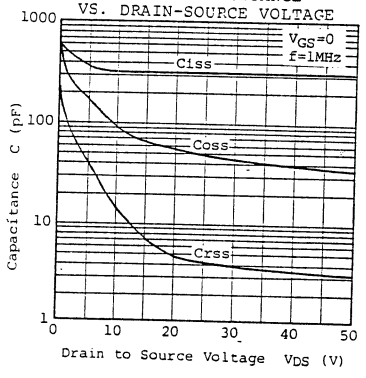
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



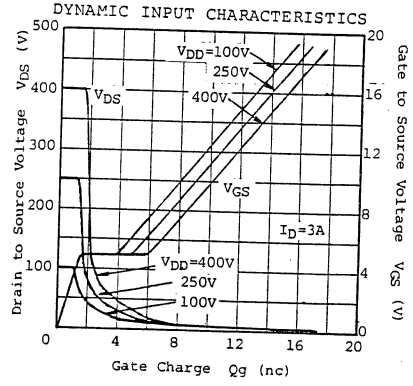
BODY-DRAIN DIODE REVERSE RECOVERY TIME



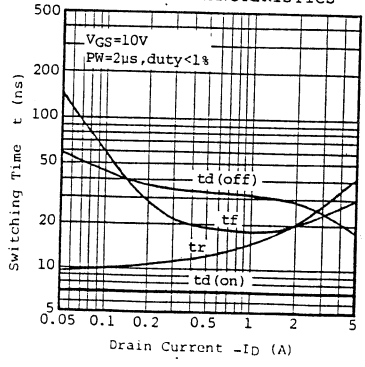
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



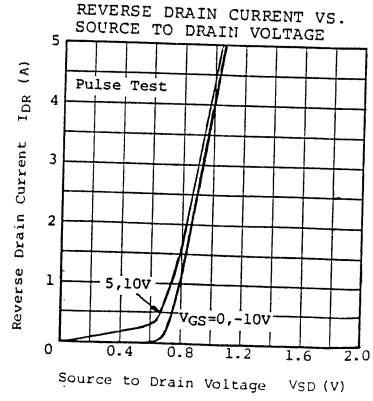
DYNAMIC INPUT CHARACTERISTICS



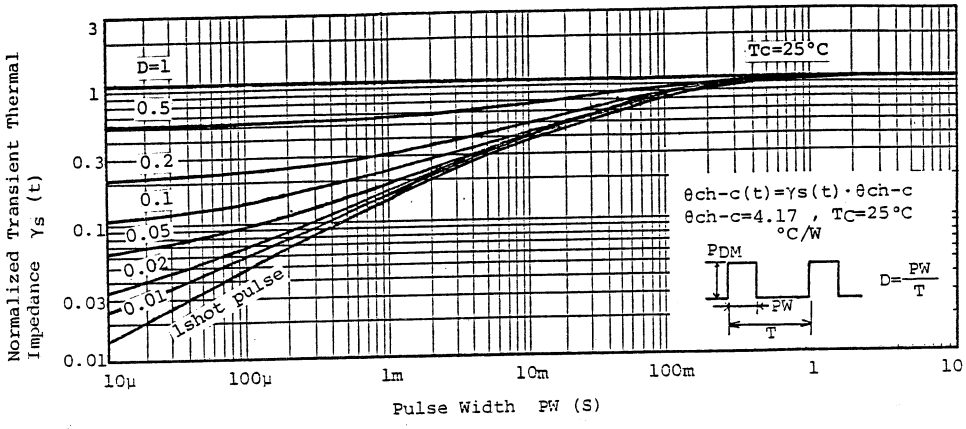
SWITCHING CHARACTERISTICS



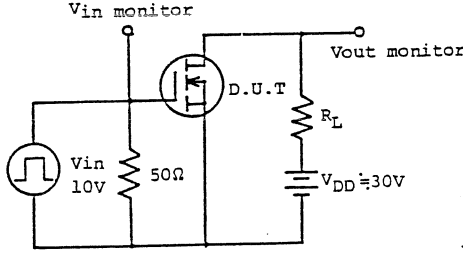
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



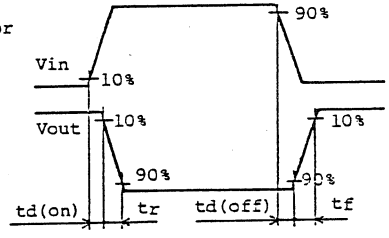
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

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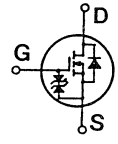
NEW PRODUCT

POWER MOS FET DⅢ-H SERIES

2SK1155, 2SK1156
(HS76091) (HS76091A)

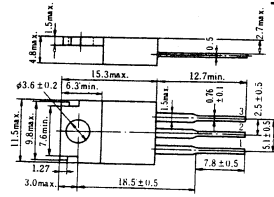
SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING

—Preliminary—



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.



1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

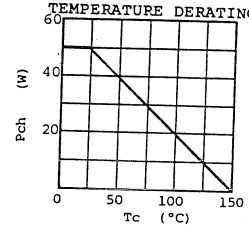
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	K1155	K1156	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±30		V
Drain Current	I_D	5		A
Drain Peak Current	$I_{D(pulse)}$*	20		A
Body-Drain Diode Reverse Drain Current	I_{DR}	5		A
Channel Dissipation	Pch**	50		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	-55 ~ +150		°C

*PW≤10μs, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	K1155	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	-	-	V
	K1156			500	-	-	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±30	-	-	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±25V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	K1155	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	250	μA
	K1156		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	3.0	V
Static Drain-Source on State Resistance	K1155	$R_{DS(on)}$	I_D=2.5A, V_{GS}=10V *	-	1.0	1.4	Ω
	K1156			-	1.2	1.5	
Foward Transfer Admittance		|yfs|	I_D=2.5A, V_{DS}=10V *	2.5	4.0	-	S
Input Capacitance		Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	640	-	pF
Output Capacitance		Coss		-	160	-	pF
Reverse Transfer Capacitance		Crss		-	20	-	pF
Turn-On Delay Time		$t_{d(on)}$	I_D=2.5A, V_{GS}=10V R_L=12Ω	-	10	-	ns
Rise Time		t_r		-	25	-	ns
Turn-Off Delay Time		$t_{d(off)}$		-	50	-	ns
Fall Time		t_f		-	30	-	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=5A, V_{GS}=0	-	0.95	-	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=5A, V_{GS}=0 dI_F/dt=100A/μs	-	300	-	ns

*Pulse Test

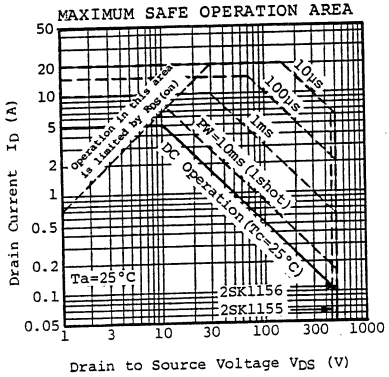
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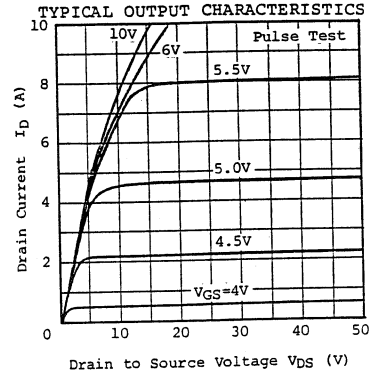
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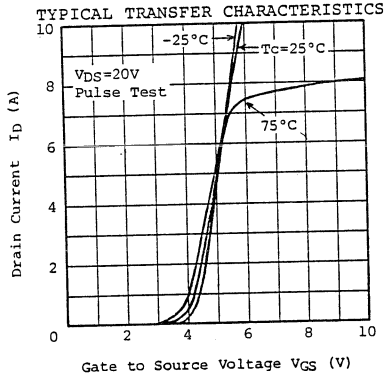
MAXIMUM SAFE OPERATION AREA



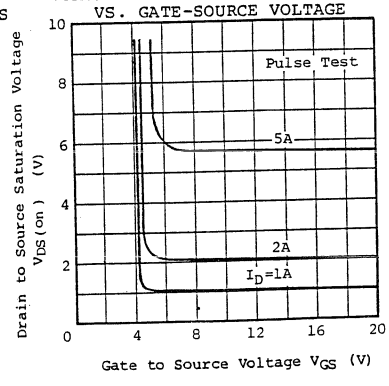
TYPICAL OUTPUT CHARACTERISTICS



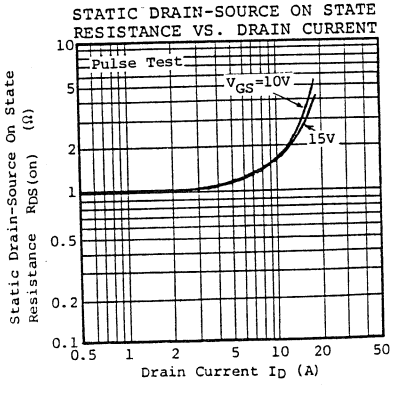
TYPICAL TRANSFER CHARACTERISTICS



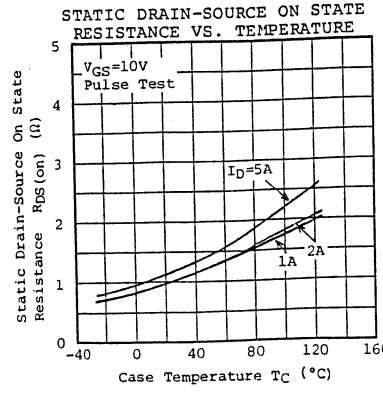
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



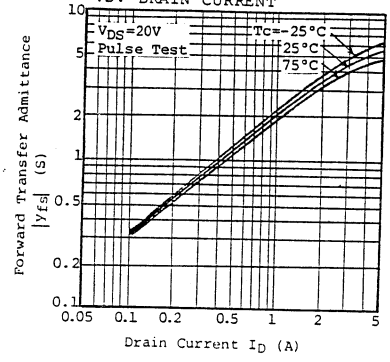
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



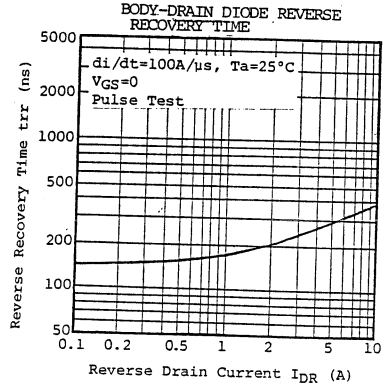
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



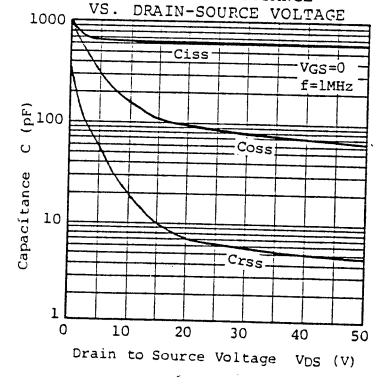
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



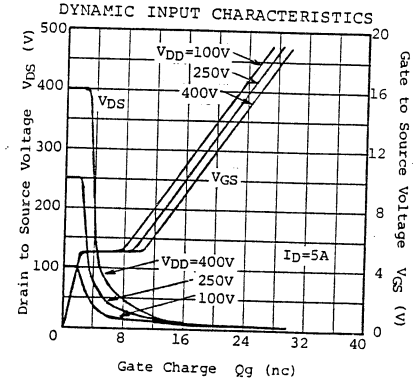
BODY-DRAIN DIODE REVERSE RECOVERY TIME



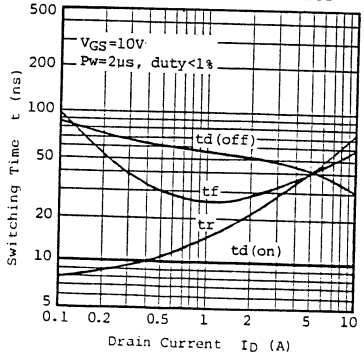
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



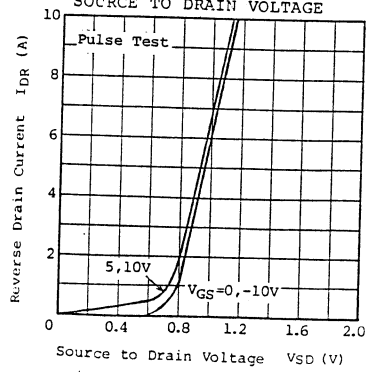
DYNAMIC INPUT CHARACTERISTICS



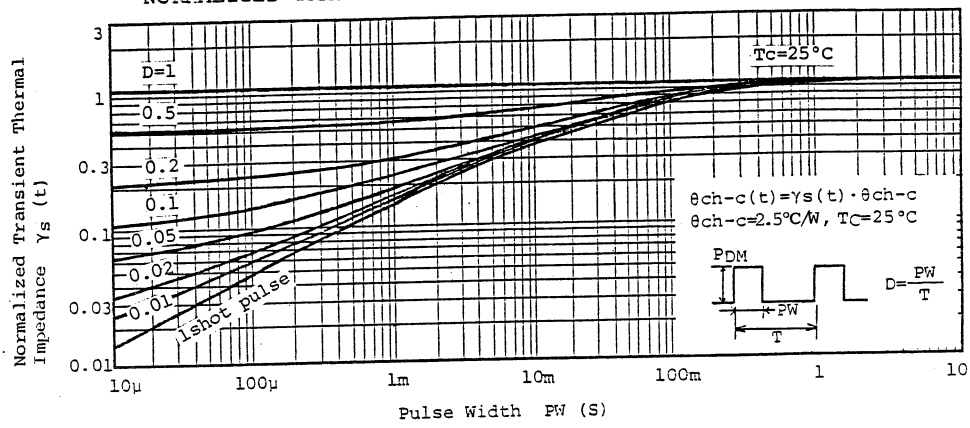
SWITCHING CHARACTERISTICS



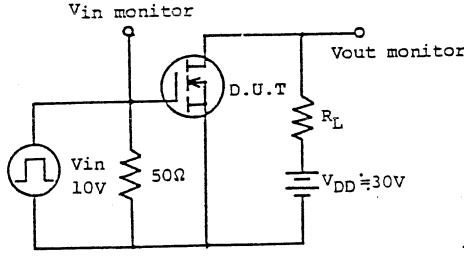
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



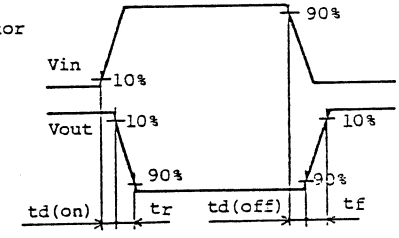
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

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NEW PRODUCT

POWER MOS FET DⅢ-H SERIES

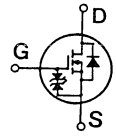
2SK1157, 2SK1158
(HS76115) (HS76115A)

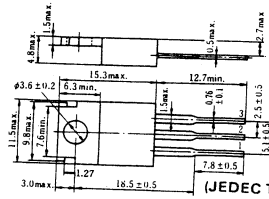
SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING

—Preliminary—

Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

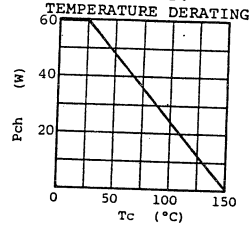
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	K1157	K1158	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±30		V
Drain Current	I_D	7		A
Drain Peak Current	$I_{D(pulse)}$*	28		A
Body-Drain Diode Reverse Drain Current	I_{DR}	7		A
Channel Dissipation	Pch**	60		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	-55～+150		°C

*PW≤10μs, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

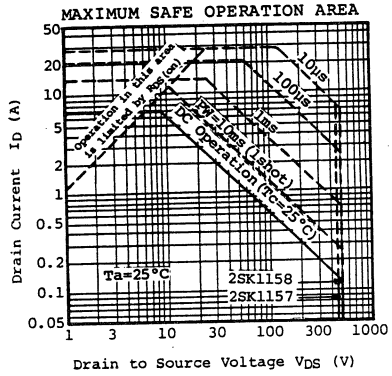
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	K1157	$V_{(BR)DSS}$	I_D= 10mA , V_{GS}=0	450	-	-	V
	K1158			500	-	-	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±30	-	-	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±25V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	K1157	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	250	μA
	K1158		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D= 1mA , V_{DS}=10V	2.0	-	3.0	V
Static Drain-Source on State Resistance	K1157	$R_{DS(on)}$	I_D= 4A , V_{GS}=10V *	-	0.6	0.8	Ω
	K1158			-	0.7	0.9	
Foward Transfer Admittance		|Yfs|	I_D=4A , V_{DS}= 10V *	4.0	6.5	-	S
Input Capacitance		Ciss	V_{DS}= 10 V, V_{GS}=0 f=1MHz	-	1050	-	pF
Output Capacitance		Coss		-	280	-	pF
Reverse Transfer Capacitance		Crss		-	40	-	pF
Turn-On Delay Time		$t_{d(on)}$	I_D= 4A , V_{GS}=10V, R_L=7.5Ω	-	15	-	ns
Rise Time		t_r		-	55	-	ns
Turn-Off Delay Time		$t_{d(off)}$		-	95	-	ns
Fall Time		t_f		-	40	-	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F= 7A , V_{GS}=0	-	0.95	-	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F= 7A , V_{GS}=0 dIF/dt=100A/μs	-	320	-	ns

*Pulse Test

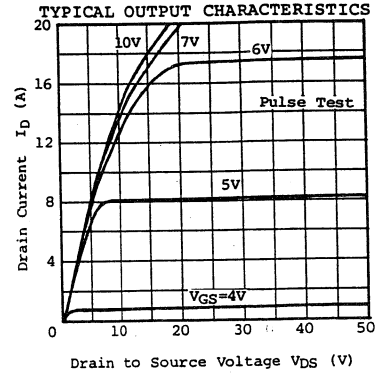
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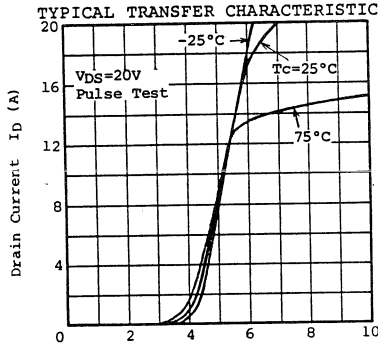
MAXIMUM SAFE OPERATION AREA



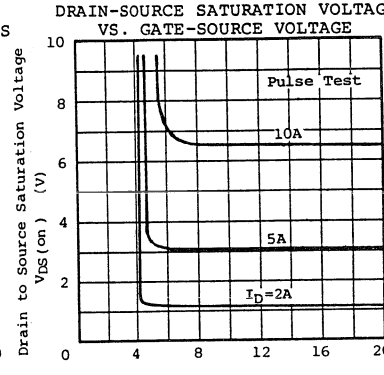
TYPICAL OUTPUT CHARACTERISTICS



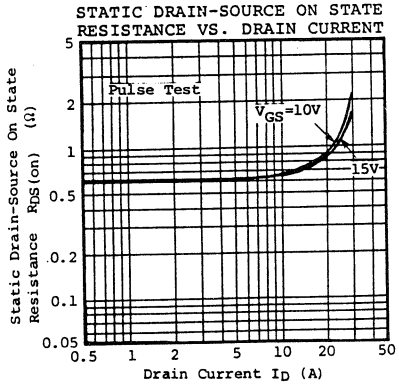
TYPICAL TRANSFER CHARACTERISTICS



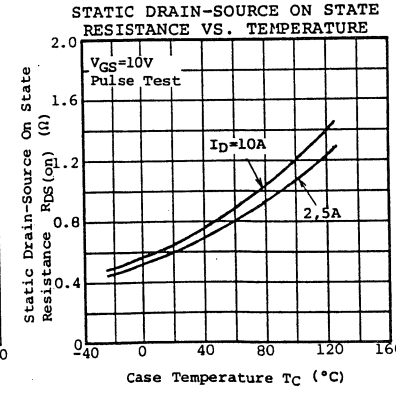
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



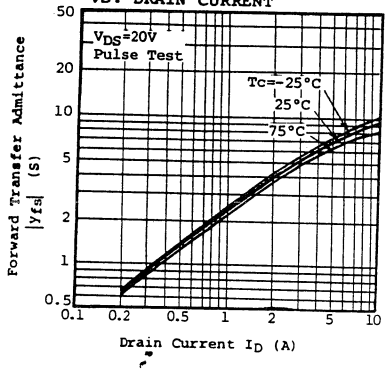
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



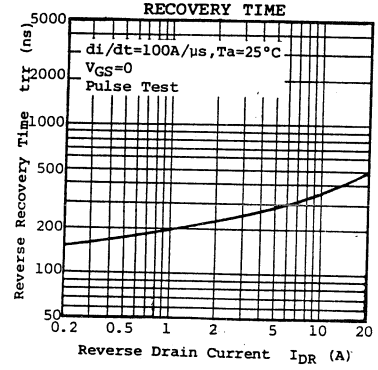
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



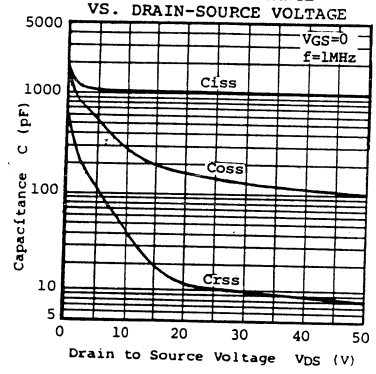
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



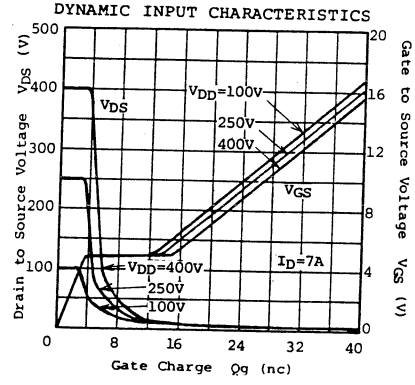
BODY-DRAIN DIODE REVERSE RECOVERY TIME



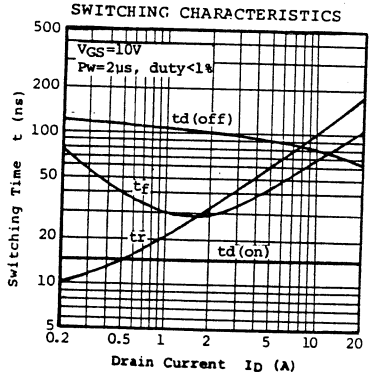
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



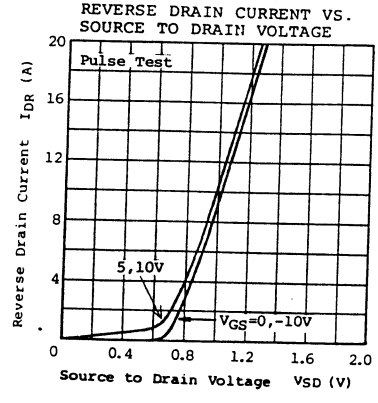
DYNAMIC INPUT CHARACTERISTICS



SWITCHING CHARACTERISTICS

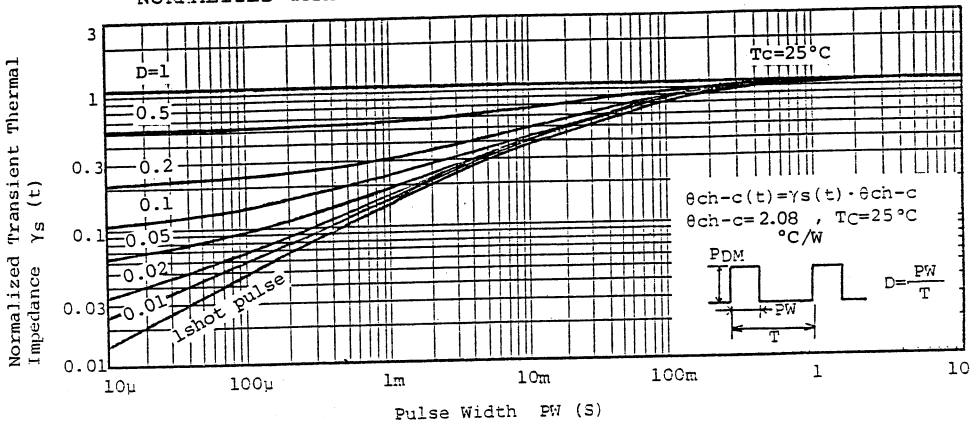


REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE

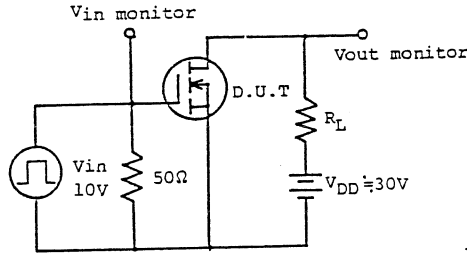


2SK1157, 2SK1158
(HS76115) (HS76115A)

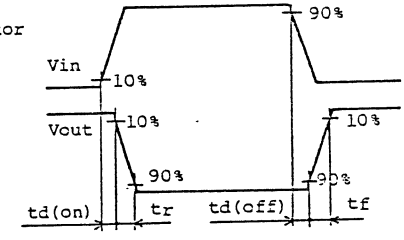
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

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NEW PRODUCT

POWER MOS FET DⅢ-H SERIES

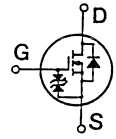
2SK1159, 2SK1160
(HS76093) (HS76093A)

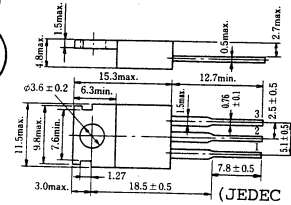
SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING

—Preliminary—

Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.





1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

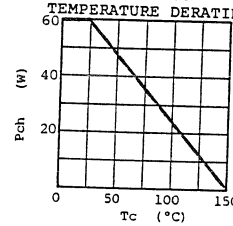
(JEDEC TO220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	K1159	K1160	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±30		V
Drain Current	I_D	8		A
Drain Peak Current	$I_{D(pulse)}$*	32		A
Body-Drain Diode Reverse Drain Current	I_{DR}	8		A
Channel Dissipation	Pch**	60		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	-55～+150		°C

*PW≤10us, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

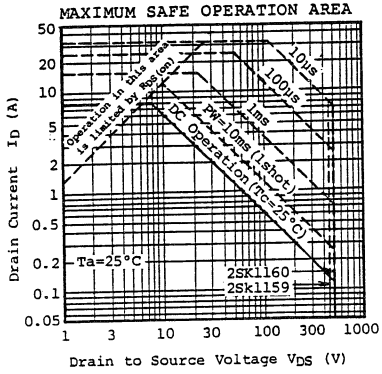
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	K1159	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	-	-	V
	K1160			500	-	-	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±30	-	-	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±25V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	K1159	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	250	μA
	K1160		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	3.0	V
Static Drain-Source on State Resistance	K1159	$R_{DS(on)}$	I_D=4A, V_{GS}=10V *	-	0.55	0.7	Ω
	K1160			-	0.60	0.8	
Foward Transfer Admittance		|Yfs|	I_D=4A, V_{DS}=10V *	4.5	7.5	-	S
Input Capacitance		Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	1150	-	pF
Output Capacitance		Coss		-	340	-	pF
Reverse Transfer Capacitance		Crss		-	55	-	pF
Turn-On Delay Time		td(on)	I_D=4A, V_{GS}=10V, R_L=7.5Ω	-	17	-	ns
Rise Time		tr		-	55	-	ns
Turn-Off Delay Time		td(off)		-	100	-	ns
Fall Time		tf		-	45	-	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=7A, V_{GS}=0	-	0.9	-	V
Body-Drain Diode Reverse Recovery Time		trr	I_F=7A, V_{GS}=0 dIF/dt=100A/μs	-	350	-	ns

*Pulse Test

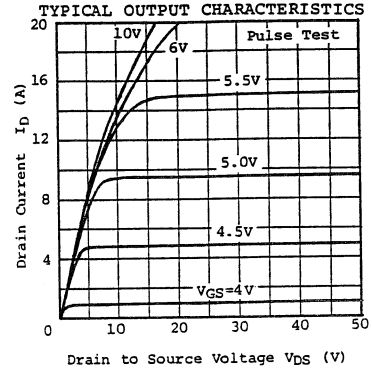
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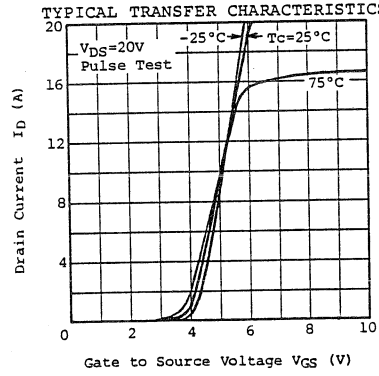
MAXIMUM SAFE OPERATION AREA



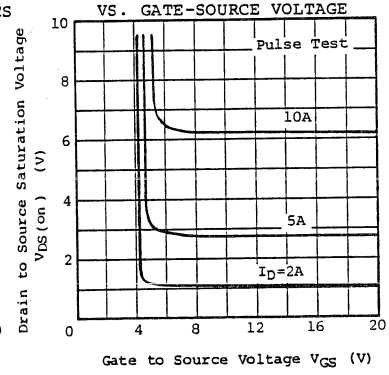
TYPICAL OUTPUT CHARACTERISTICS



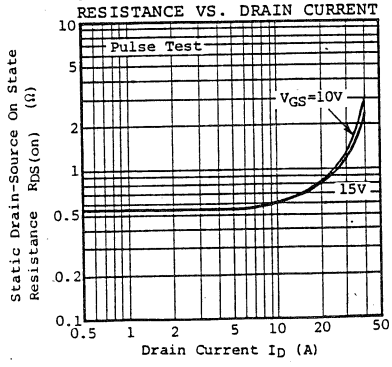
TYPICAL TRANSFER CHARACTERISTICS



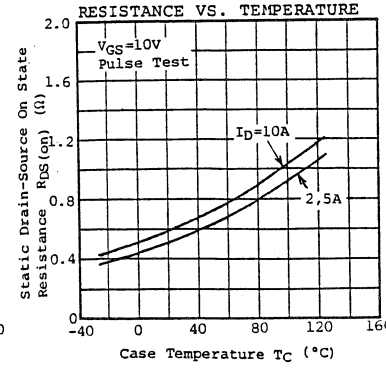
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



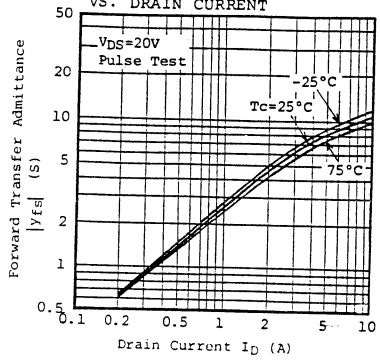
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



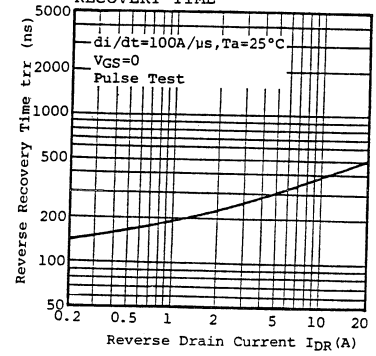
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



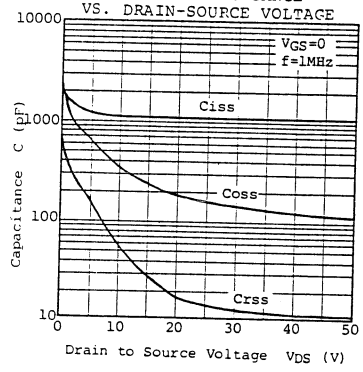
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



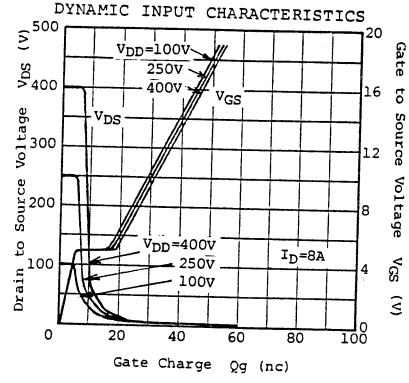
BODY-DRAIN DIODE REVERSE RECOVERY TIME



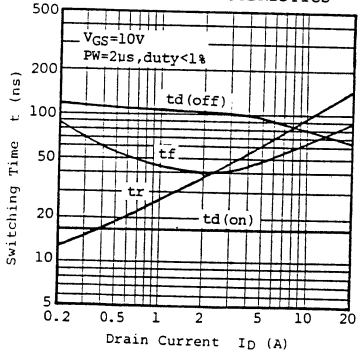
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



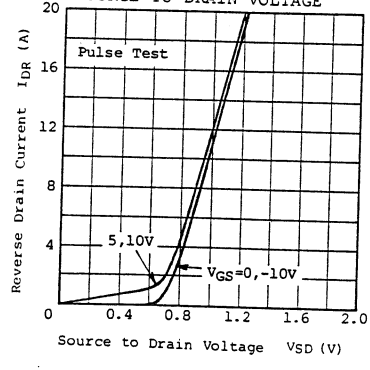
DYNAMIC INPUT CHARACTERISTICS



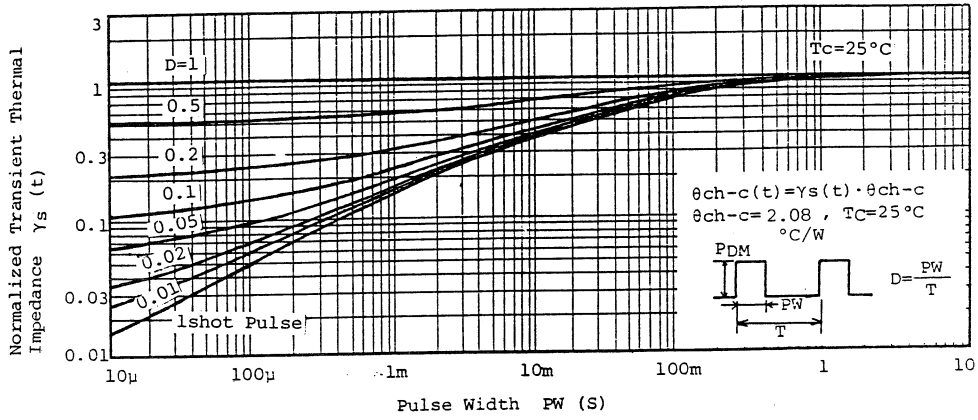
SWITCHING CHARACTERISTICS



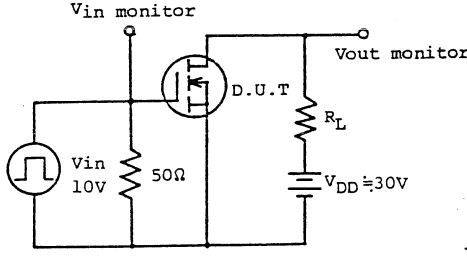
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



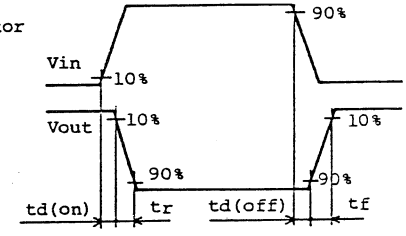
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

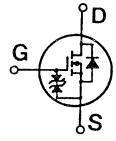
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NEW PRODUCT

POWER MOS FET DⅢ-H SERIES

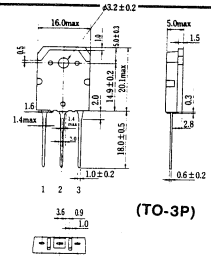
2SK1161, 2SK1162
(HS78131) (HS78131A)

SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.



(TO-3P)

—Preliminary—

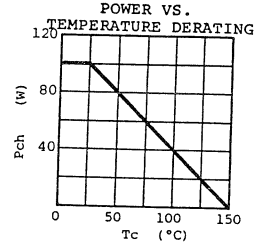
1. Gate
2. Drain (Flange)
3. Source

(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	K1161	K1162	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±30		V
Drain Current	I_D	10		A
Drain Peak Current	$I_{D(pulse)}$*	30		A
Body-Drain Diode Reverse Drain Current	I_{DR}	10		A
Channel Dissipation	Pch**	100		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	-55 ~ +150		°C

*PW≤10μs, duty cycle≤1% **Value at Tc=25°C



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

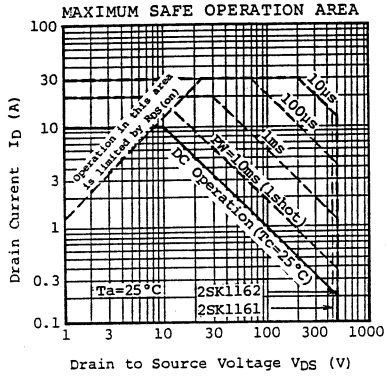
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	K1161	$V_{(BR)DSS}$	I_D= 10mA , V_{GS}=0	450	-	-	V
	K1162			500	-	-	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±30	-	-	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±25V , V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	K1161	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	250	μA
	K1162		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	2.0	-	3.0	V
Static Drain-Source on State Resistance	K1161	$R_{DS(on)}$	I_D= 5A , V_{GS}=10V *	-	0.6	0.8	Ω
	K1162			-	0.7	0.9	
Foward Transfer Admittance		|yfs|	I_D=5A , V_{DS}=10V *	4.0	7.0	-	S
Input Capacitance		Ciss	V_{DS}= 10 V, V_{GS}=0 f=1MHz	-	1050	-	pF
Output Capacitance		Coss		-	280	-	pF
Reverse Transfer Capacitance		Crss		-	40	-	pF
Turn-On Delay Time		$t_{d(on)}$	I_D= 5A , V_{GS}= 10V, R_L= 6Ω	-	15	-	ns
Rise Time		t_r		-	60	-	ns
Turn-Off Delay Time		$t_{d(off)}$		-	90	-	ns
Fall Time		t_f		-	45	-	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F= 10A , V_{GS}=0	-	1.0	-	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F= 10A , V_{GS}=0 dIF/dt=100A/μs	-	350	-	ns

*Pulse Test

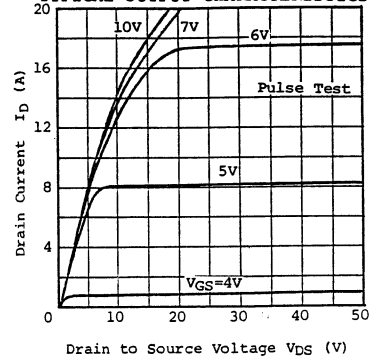
NOTICE:
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Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

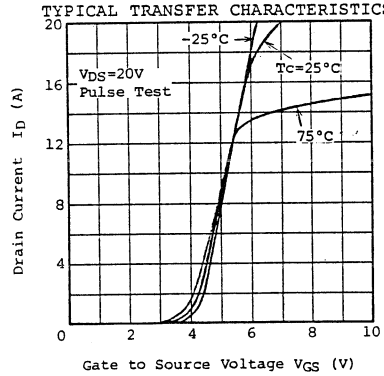
MAXIMUM SAFE OPERATION AREA



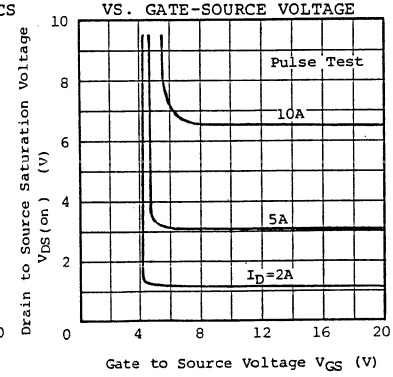
TYPICAL OUTPUT CHARACTERISTICS



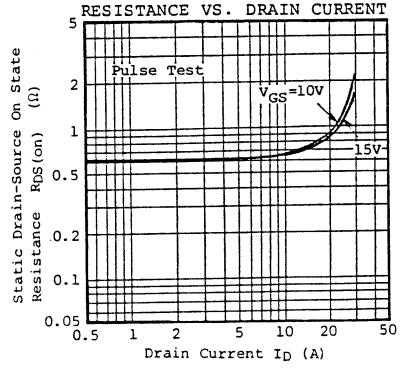
TYPICAL TRANSFER CHARACTERISTICS



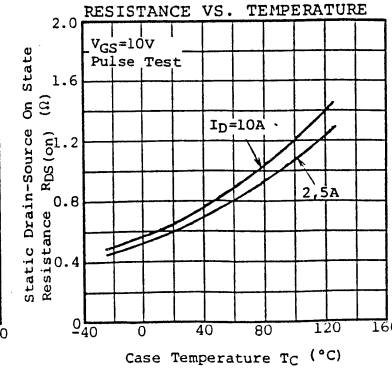
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



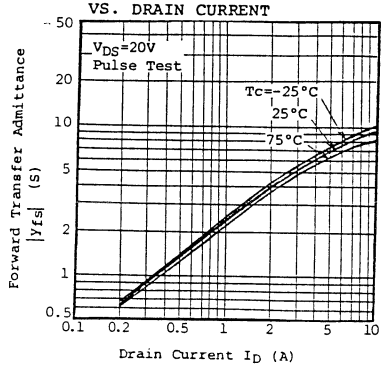
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



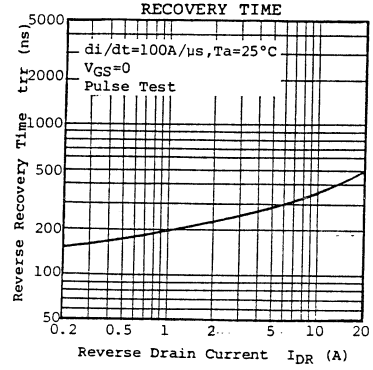
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



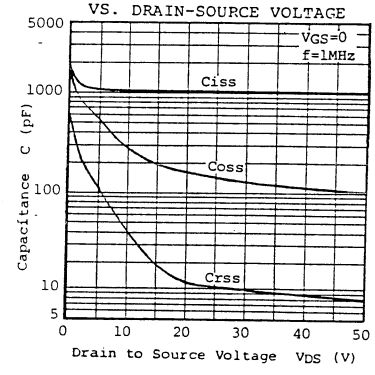
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



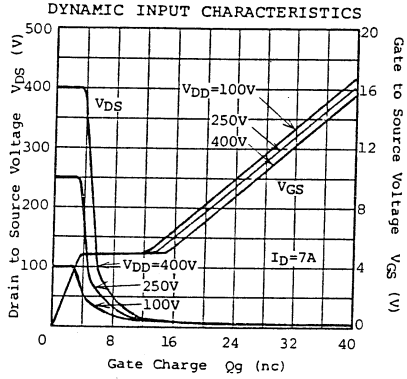
BODY-DRAIN DIODE REVERSE RECOVERY TIME



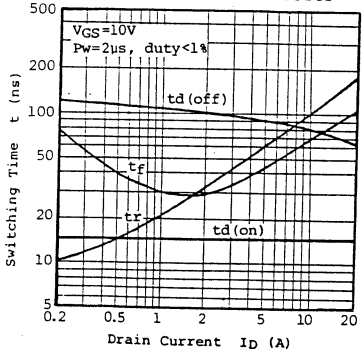
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



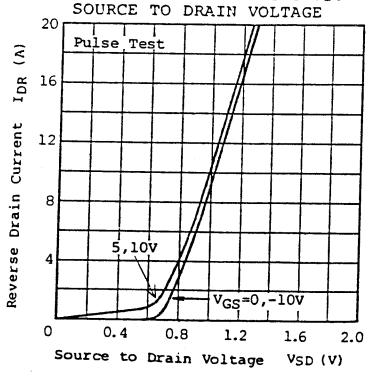
DYNAMIC INPUT CHARACTERISTICS



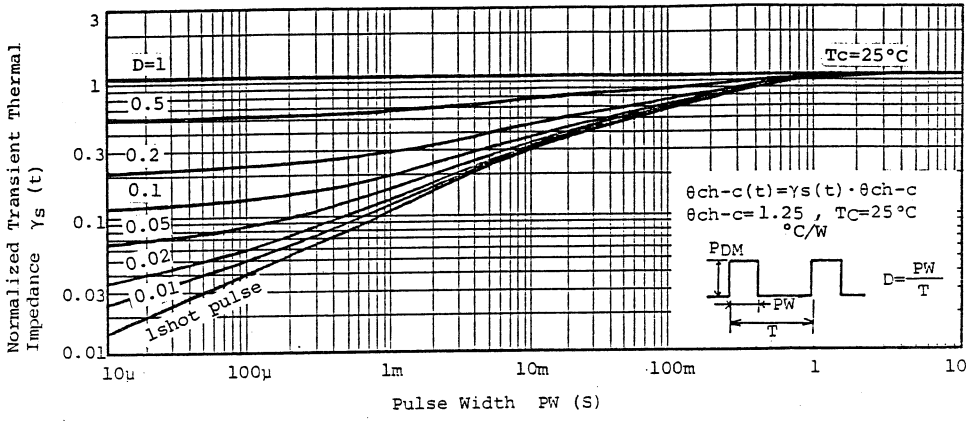
SWITCHING CHARACTERISTICS



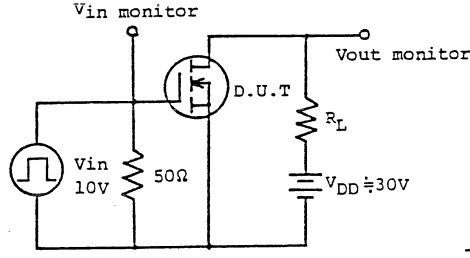
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



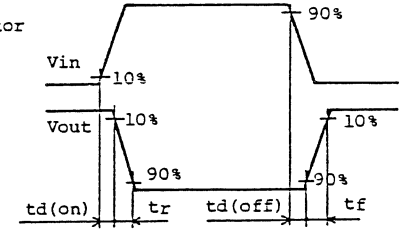
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

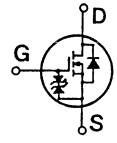
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NEW PRODUCT

POWER MOS FET DⅢ-H SERIES

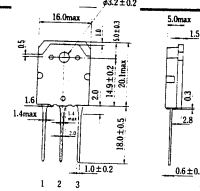
2SK1163, 2SK1164
(HS78097) (HS78097A)

SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.



(TO-3P)

—Preliminary—

1. Gate
2. Drain (Flange)
3. Source

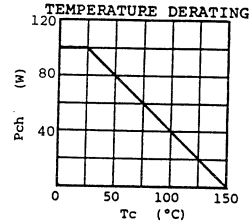
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	K1163	K1164	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±30		V
Drain Current	I_D	11		A
Drain Peak Current	$I_{D(pulse)}$*	40		A
Body-Drain Diode Reverse Drain Current	I_{DR}	11		A
Channel Dissipation	Pch**	100		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	-55～+150		°C

*PW≦10us, duty cycle≦1%　　**Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	K1163	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	-	-	V
	K1164			500	-	-	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±30	-	-	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±25V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	K1163	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	250	μA
	K1164		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	3.0	V
Static Drain-Source on State Resistance	K1163	$R_{DS(on)}$	I_D=5A, V_{GS}=10V *	-	0.55	0.7	Ω
	K1164			-	0.60	0.8	
Foward Transfer Admittance		|yfs|	I_D=5A, V_{DS}=10V *	5.0	8.0	-	S
Input Capacitance		Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz	-	1150	-	pF
Output Capacitance		Coss		-	340	-	pF
Reverse Transfer Capacitance		Crss		-	55	-	pF
Turn-On Delay Time		$t_{d(on)}$	I_D=5A, V_{GS}=10V, R_L=6Ω	-	17	-	ns
Rise Time		t_r		-	60	-	ns
Turn-Off Delay Time		$t_{d(off)}$		-	95	-	ns
Fall Time		t_f		-	50	-	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=11A, V_{GS}=0	-	1.0	-	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=11A, V_{GS}=0 dIF/dt=100A/μs	-	400	-	ns

*Pulse Test

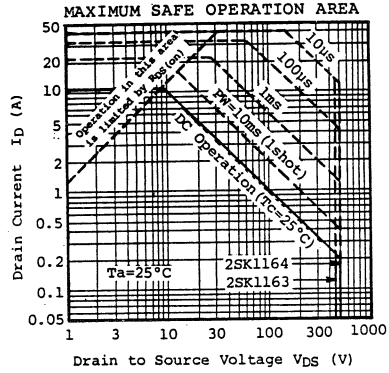
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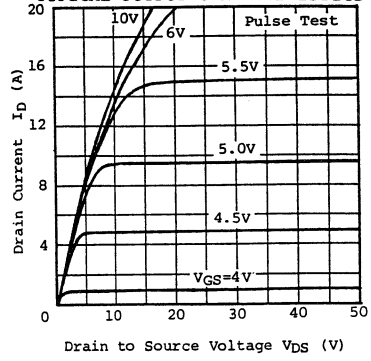
HITACHI

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T-22-B-DS540-O

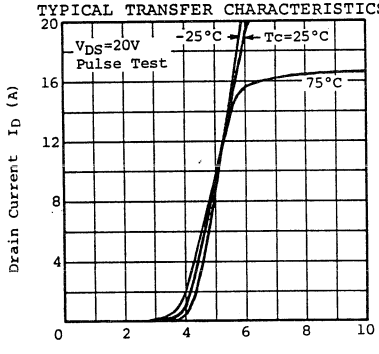
MAXIMUM SAFE OPERATION AREA



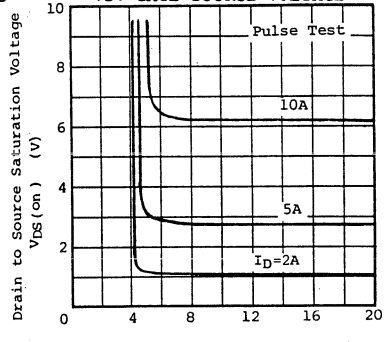
TYPICAL OUTPUT CHARACTERISTICS



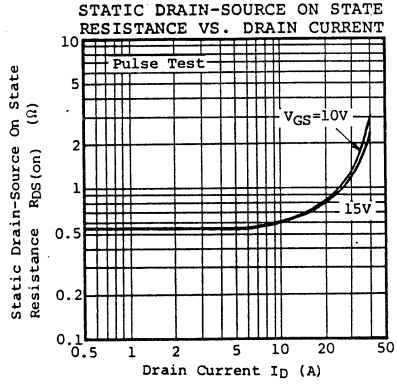
TYPICAL TRANSFER CHARACTERISTICS



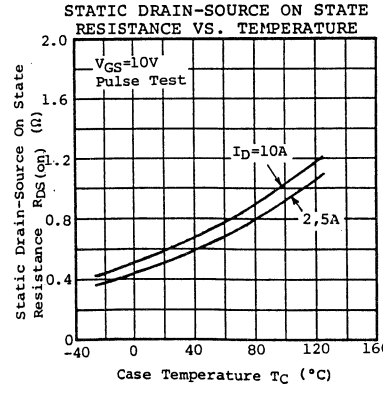
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



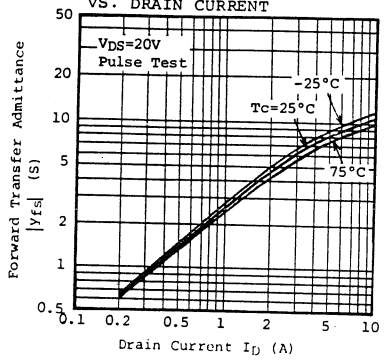
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



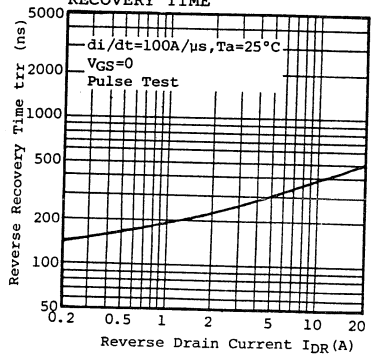
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



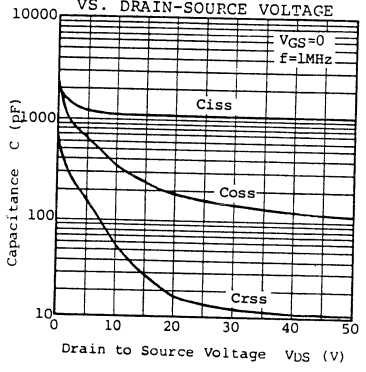
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



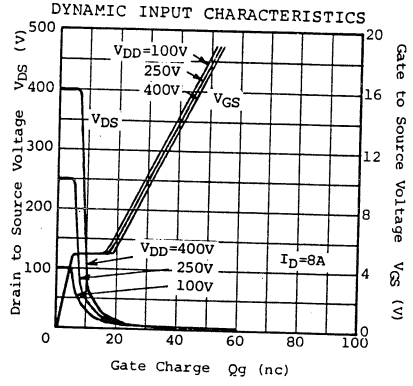
BODY-DRAIN DIODE REVERSE RECOVERY TIME



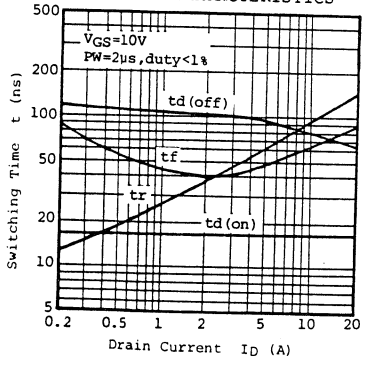
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



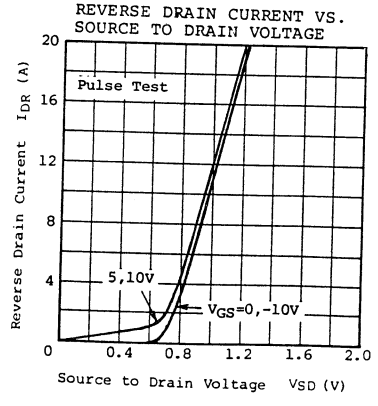
DYNAMIC INPUT CHARACTERISTICS



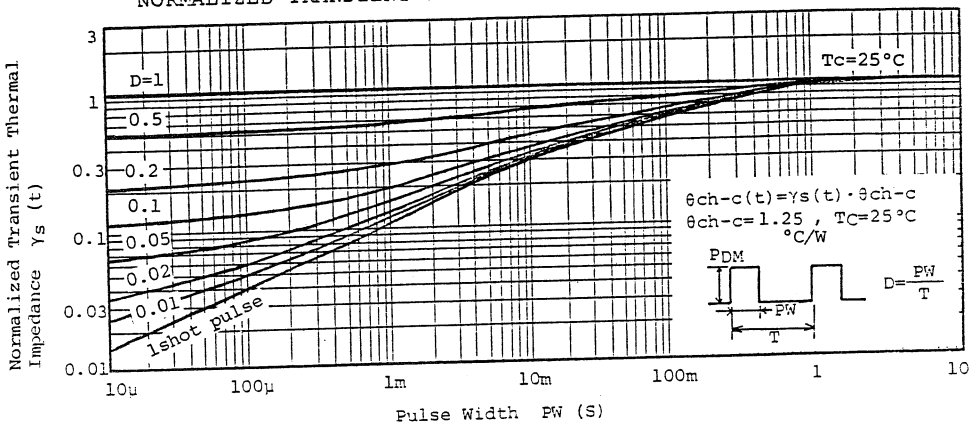
SWITCHING CHARACTERISTICS



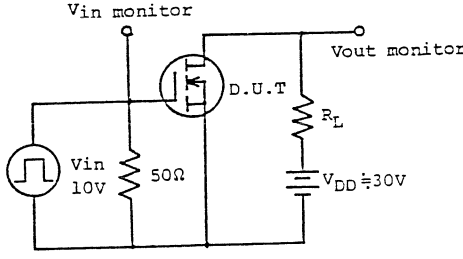
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



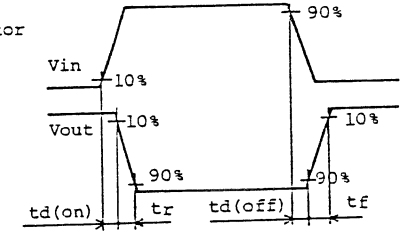
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

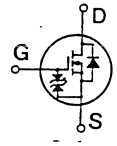
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NEW PRODUCT

POWER MOS FET DⅢ-H SERIES

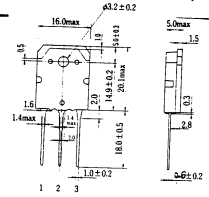
2SK1165, 2SK1166
(HS78099) (HS78099A)

SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.



(TO-3P)

(Dimensions in mm)

Preliminary

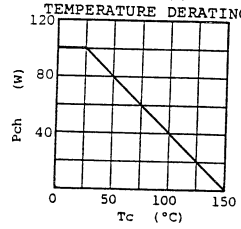
1. Gate
2. Drain (Flange)
3. Source

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	K1165	K1166	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±30		V
Drain Current	I_D	12		A
Drain Peak Current	$I_{D(pulse)}$*	48		A
Body-Drain Diode Reverse Drain Current	I_{DR}	12		A
Channel Dissipation	Pch**	100		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	−55 ~ +150		°C

*PW≤10us, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

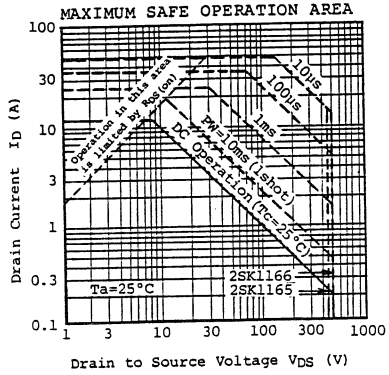
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	K1165	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	-	-	V
	K1166			500	-	-	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±30	-	-	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±25V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	K1165	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	250	μA
	K1166		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	3.0	V
Static Drain-Source on State Resistance	K1165	$R_{DS(on)}$	I_D=6A, V_{GS}=10V *	-	0.40	0.55	Ω
	K1166			-	0.45	0.60	
Foward Transfer Admittance		|yfs|	I_D=6A, V_{DS}=10V *	6.0	10	-	S
Input Capacitance		Ciss	V_{DS}=10V, V_{GS}=0 f=1MHz	-	1450	-	pF
Output Capacitance		Coss		-	410	-	pF
Reverse Transfer Capacitance		Crss		-	55	-	pF
Turn-On Delay Time		$t_{d(on)}$	I_D=6A, V_{GS}=10V R_L=5Ω	-	20	-	ns
Rise Time		t_r		-	70	-	ns
Turn-Off Delay Time		$t_{d(off)}$		-	120	-	ns
Fall Time		t_f		-	60	-	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=12A, V_{GS}=0	-	1.0	-	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=12A, V_{GS}=0 dIF/dt=100A/μs	-	450	-	ns

*Pulse Test

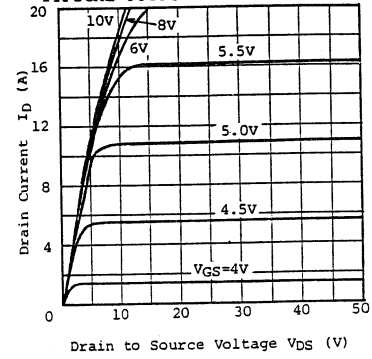
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Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

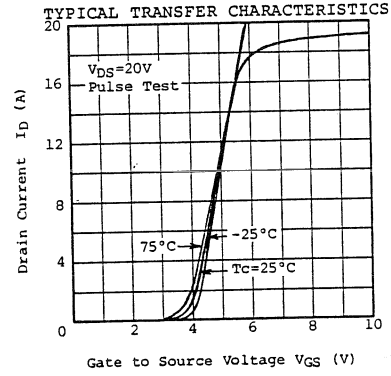
MAXIMUM SAFE OPERATION AREA



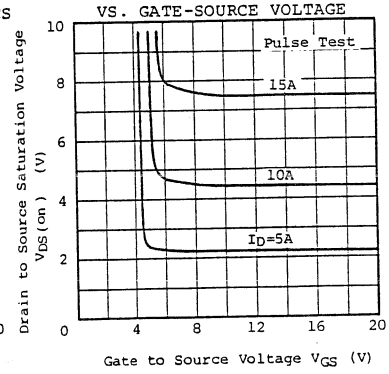
TYPICAL OUTPUT CHARACTERISTICS



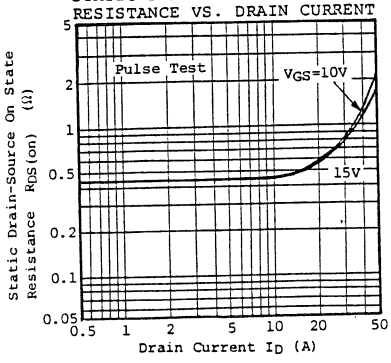
TYPICAL TRANSFER CHARACTERISTICS



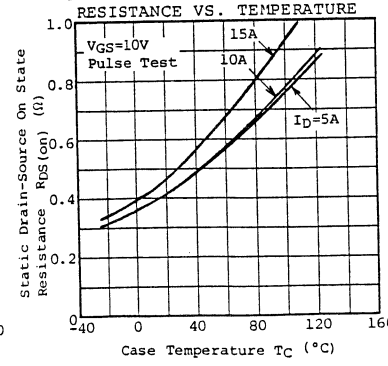
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



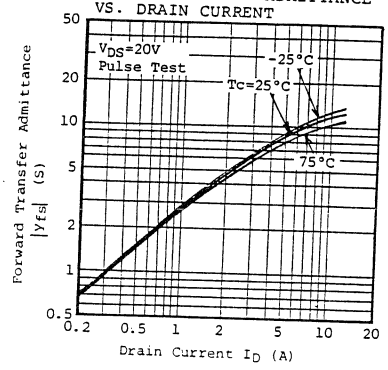
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



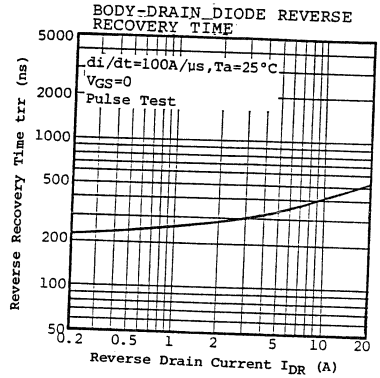
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



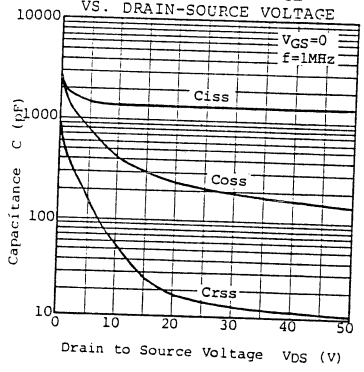
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



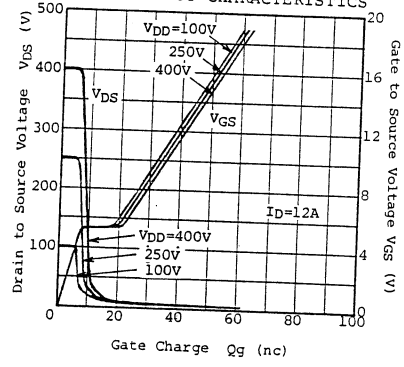
BODY-DRAIN DIODE REVERSE RECOVERY TIME



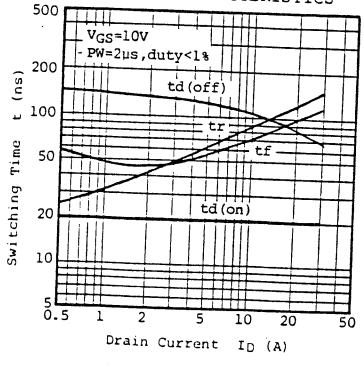
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



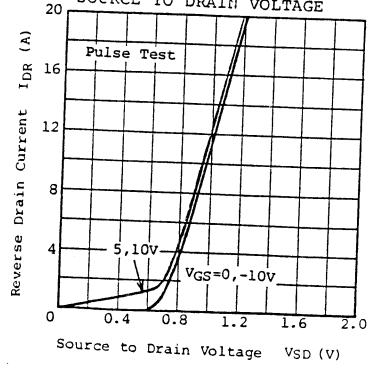
DYNAMIC INPUT CHARACTERISTICS



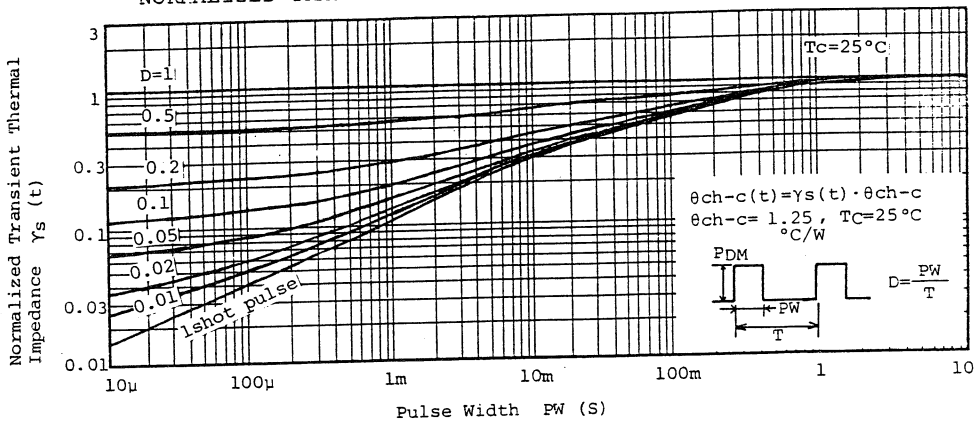
SWITCHING CHARACTERISTICS



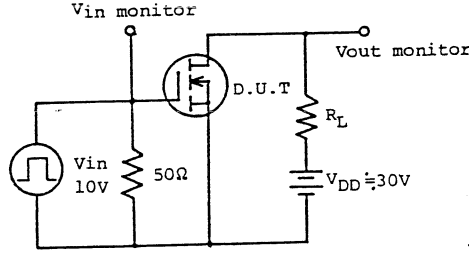
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



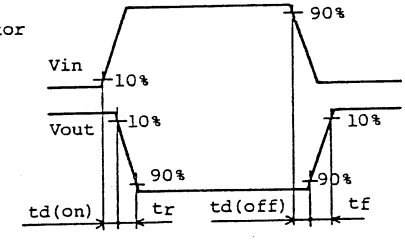
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

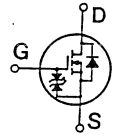
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NEW PRODUCT

POWER MOS FET DⅢ-H SERIES

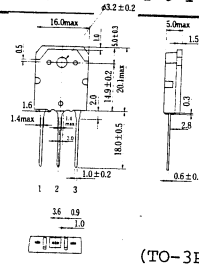
2SK1167, 2SK1168
(HS78101) (HS78101A)

SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING



Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.



(TO-3P)

—Preliminary—

1. Gate
2. Drain (Flange)
3. Source

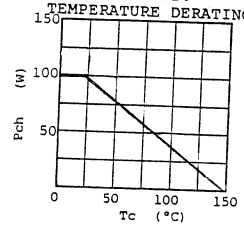
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	K1167	K1168	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±30		V
Drain Current	I_D	15		A
Drain Peak Current	$I_{D(pulse)}$*	60		A
Body-Drain Diode Reverse Drain Current	I_{DR}	15		A
Channel Dissipation	Pch**	100		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	-55 ~ +150		°C

*PW≤10us, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	K1167	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	-	-	V
	K1168			500	-	-	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±30	-	-	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±25V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	K1167	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	250	μA
	K1168		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	3.0	V
Static Drain-Source on State Resistance	K1167	$R_{DS(on)}$	I_D=8A, V_{GS}=10V *	-	0.25	0.36	Ω
	K1168			-	0.30	0.40	
Foward Transfer Admittance		|Yfs|	I_D=8A, V_{DS}=10V *	8	13	-	S
Input Capacitance		Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	2050	-	pF
Output Capacitance		Coss		-	600	-	pF
Reverse Transfer Capacitance		Crss		-	75	-	pF
Turn-On Delay Time		$t_{d(on)}$	I_D=8A, V_{GS}=10V R_L=3.75Ω	-	30	-	ns
Rise Time		t_r		-	110	-	ns
Turn-Off Delay Time		$t_{d(off)}$		-	150	-	ns
Fall Time		t_f		-	70	-	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=15A, V_{GS}=0	-	1.0	-	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=15A, V_{GS}=0 dIF/dt=100A/μs	-	500	-	ns

*Pulse Test

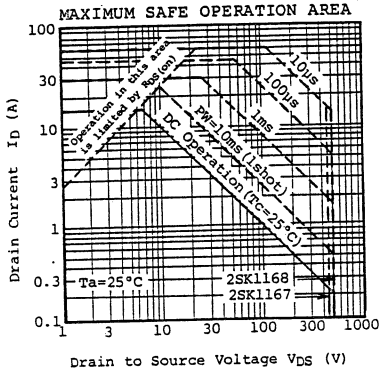
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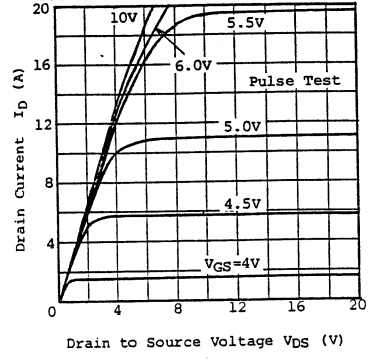
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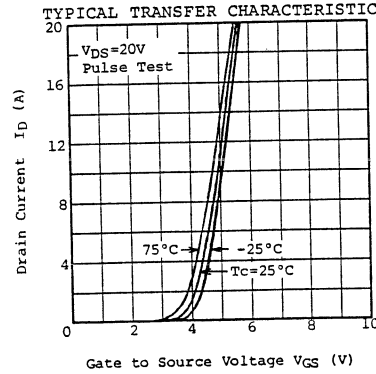
MAXIMUM SAFE OPERATION AREA



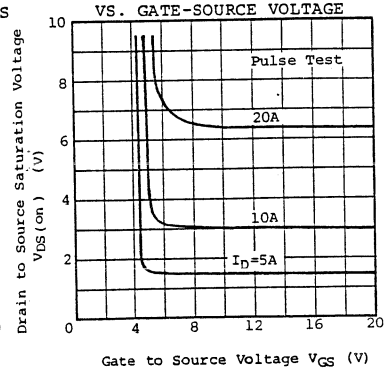
TYPICAL OUTPUT CHARACTERISTICS



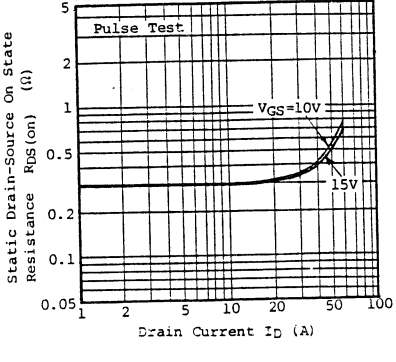
TYPICAL TRANSFER CHARACTERISTICS



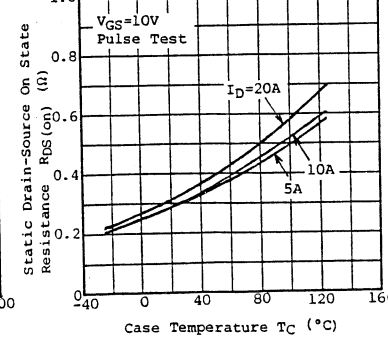
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



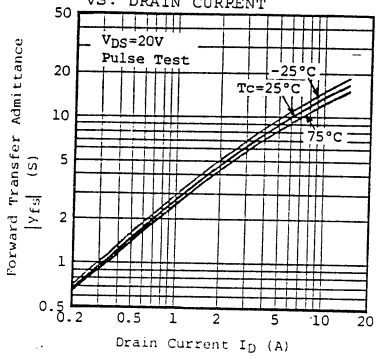
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



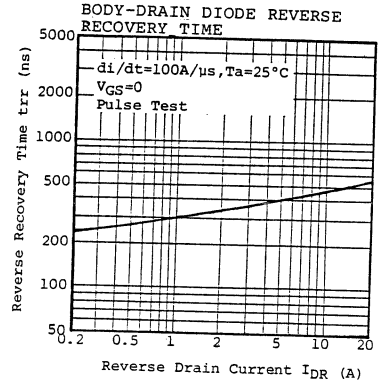
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



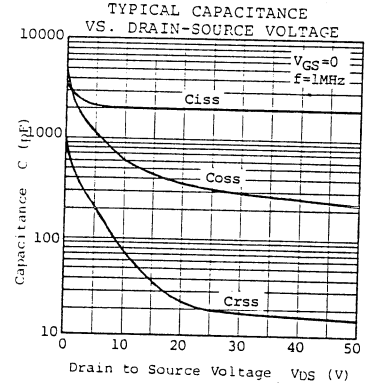
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



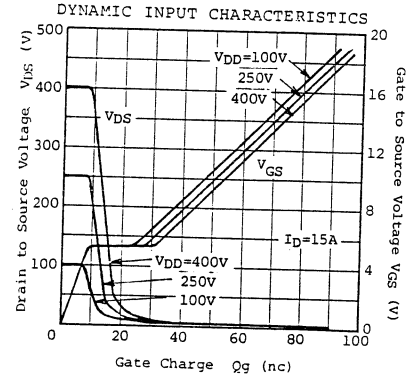
BODY-DRAIN DIODE REVERSE RECOVERY TIME



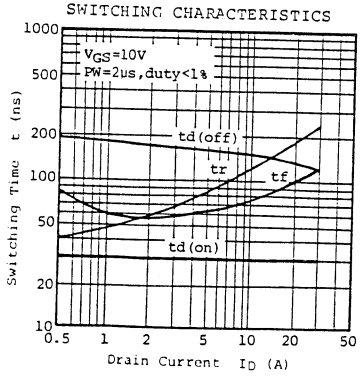
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



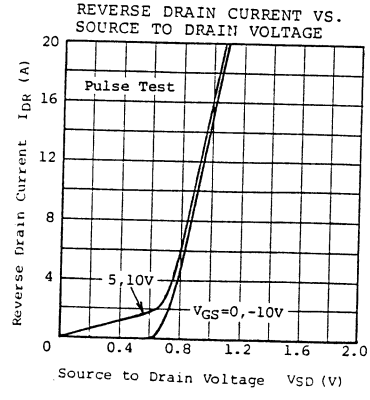
DYNAMIC INPUT CHARACTERISTICS



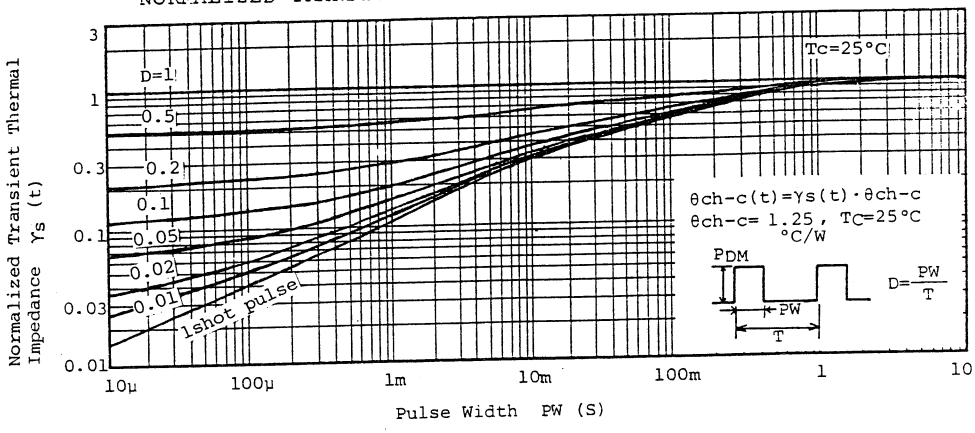
SWITCHING CHARACTERISTICS



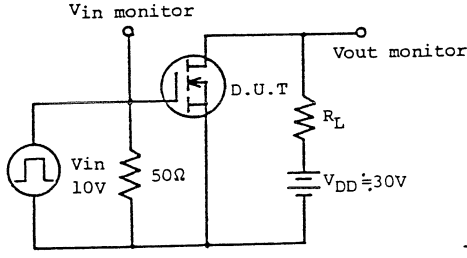
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



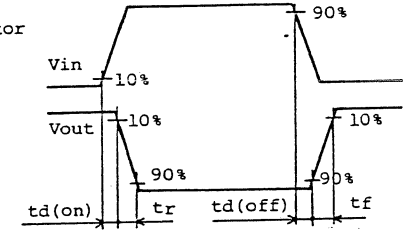
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

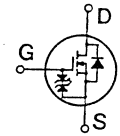
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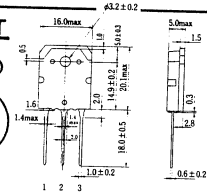
NEW PRODUCT

POWER MOS FET DⅢ-H SERIES

2SK1169, 2SK1170
(HS78103) (HS78103A)

SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING





(TO-3P)

—Preliminary—

Features;

- Low On-Resistance.
- High Speed Switching.
- Low Drive Current.
- No Secondary Breakdown.
- Suitable for Switching Regulator, DC-DC Converter.

1. Gate
2. Drain (Flange)
3. Source

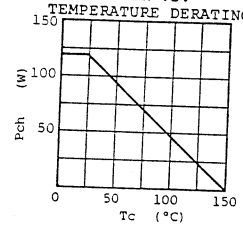
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	K1169	K1170	Unit
Drain-Source Voltage	V_{DSS}	450	500	V
Gate-Source Voltage	V_{GSS}	±30		V
Drain Current	I_D	20		A
Drain Peak Current	$I_{D(pulse)}$*	80		A
Body-Drain Diode Reverse Drain Current	I_{DR}	20		A
Channel Dissipation	Pch**	120		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	-55~+150		°C

*PW≤10μs, duty cycle≤1% **Value at Tc=25°C

POWER VS. TEMPERATURE DERATING



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

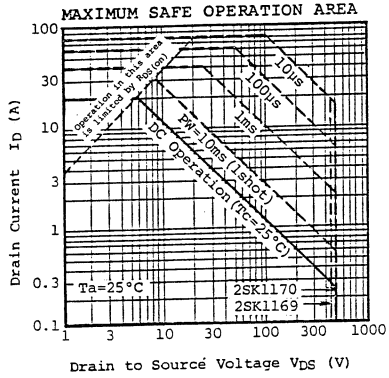
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	K1169	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	-	-	V
	K1170			500	-	-	
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±30	-	-	V
Gate-Source Leak Current		I_{GSS}	V_{GS}=±25V, V_{DS}=0	-	-	±10	μA
Zero Gate Voltage Drain Current	K1169	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	250	μA
	K1170		V_{DS}=400V, V_{GS}=0				
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	2.0	-	3.0	V
Static Drain-Source on State Resistance	K1169	$R_{DS(on)}$	I_D=10A, V_{GS}=10V *	-	0.20	0.25	Ω
	K1170			-	0.22	0.27	
Foward Transfer Admittance		|Yfs|	I_D=10A, V_{DS}=10V *	10	16	-	S
Input Capacitance		Ciss	V_{DS}=10 V, V_{GS}=0 f=1MHz	-	2800	-	pF
Output Capacitance		Coss		-	780	-	pF
Reverse Transfer Capacitance		Crss		-	90	-	pF
Turn-On Delay Time		$t_{d(on)}$	I_D=10A, V_{GS}=10V R_L=3Ω	-	32	-	ns
Rise Time		t_r		-	115	-	ns
Turn-Off Delay Time		$t_{d(off)}$		-	200	-	ns
Fall Time		t_f		-	90	-	ns
Body-Drain Diode Forward Voltage		V_{DF}	I_F=20A, V_{GS}=0	-	1.0	-	V
Body-Drain Diode Reverse Recovery Time		t_{rr}	I_F=20A, V_{GS}=0 dI_F/dt=100A/μs	-	500	-	ns

*Pulse Test

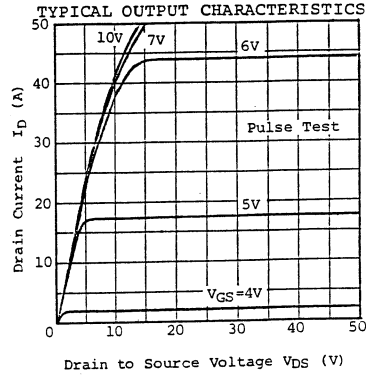
NOTICE:
The example of an applied circuit or combination with other equipment shown herein indicates characteristics and performance of semiconductor-applied products.
The company shall assume no responsibility for any problem involving a patent caused when applying the descriptions in the example.

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

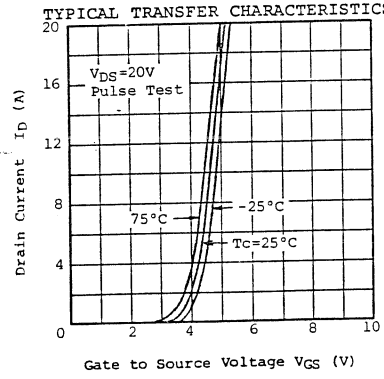
MAXIMUM SAFE OPERATION AREA



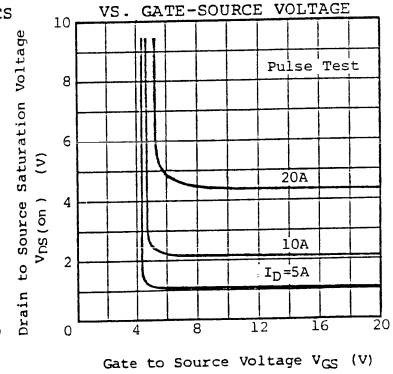
TYPICAL OUTPUT CHARACTERISTICS



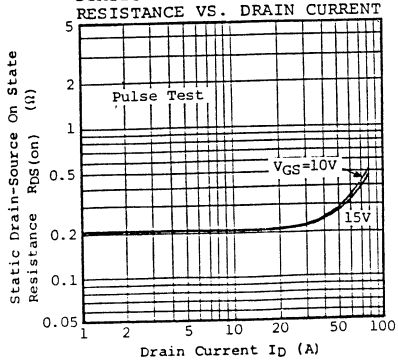
TYPICAL TRANSFER CHARACTERISTICS



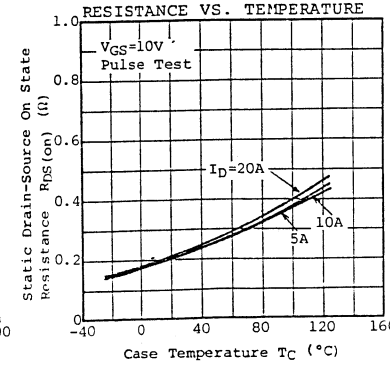
DRAIN-SOURCE SATURATION VOLTAGE VS. GATE-SOURCE VOLTAGE



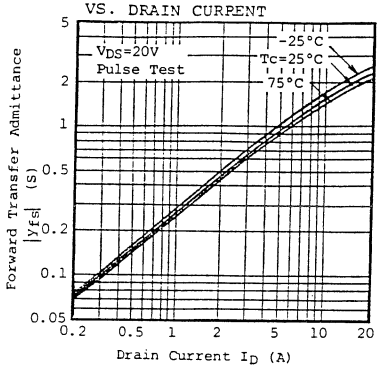
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. DRAIN CURRENT



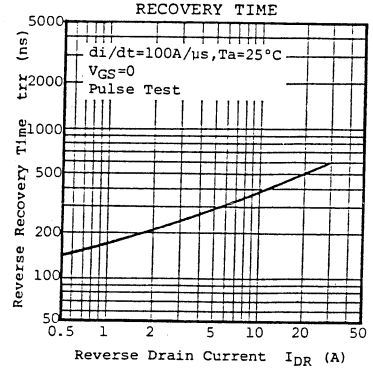
STATIC DRAIN-SOURCE ON STATE RESISTANCE VS. TEMPERATURE



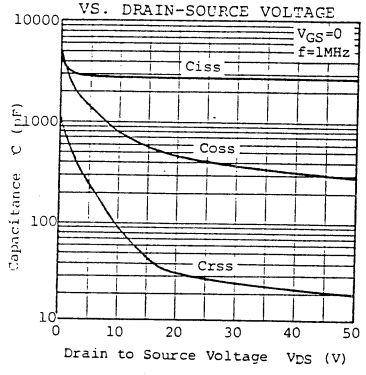
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



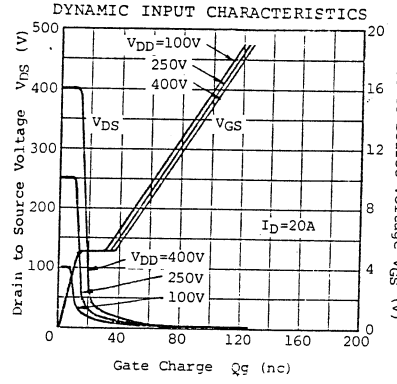
BODY-DRAIN DIODE REVERSE RECOVERY TIME



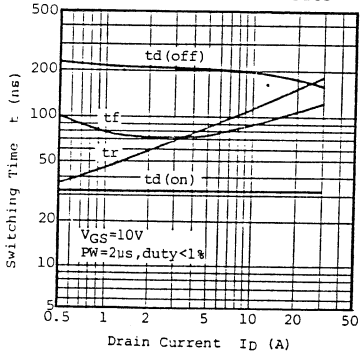
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE



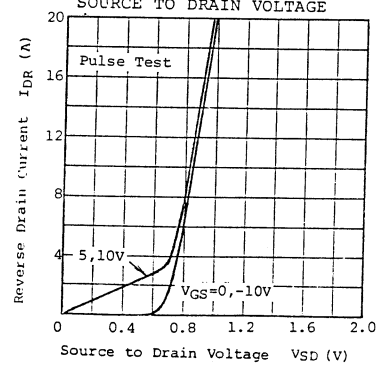
DYNAMIC INPUT CHARACTERISTICS



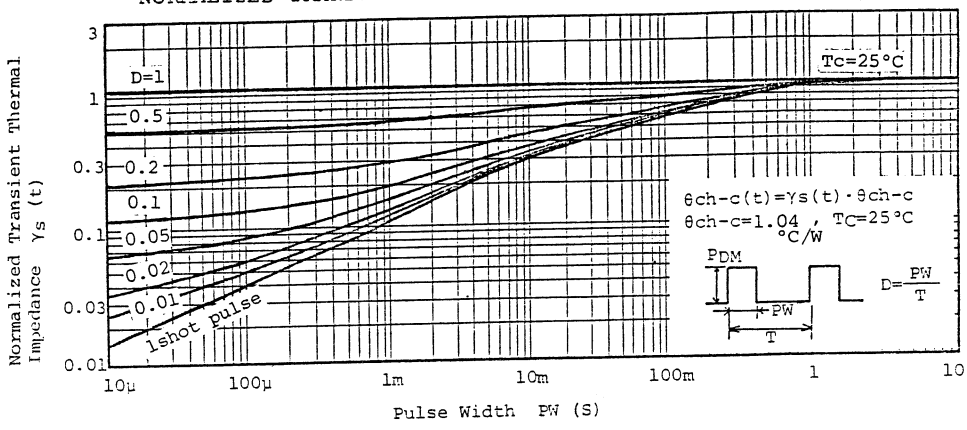
SWITCHING CHARACTERISTICS



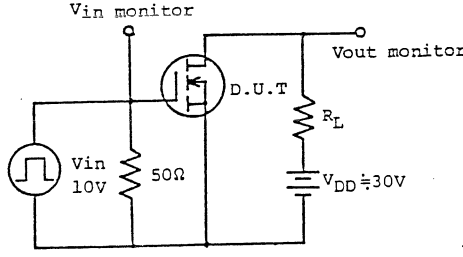
REVERSE DRAIN CURRENT VS. SOURCE TO DRAIN VOLTAGE



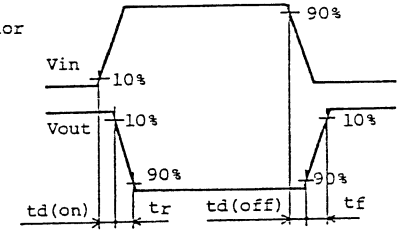
NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS



Note 1) ZENER DIODES EQUIPPED BETWEEN GATE AND SOURCE CANNOT PREVENT ELECTRO-STATIC DAMAGE IN ALL CIRCUMSTANCES. TO PROTECT DEVICES FROM ELECTRO-STATIC DAMAGE, GROUNDING SOLDERING IRON AND MEASUREMENT EQUIPMENT, AND USING GROUND STRAP ARE EFFECTIVE.

注1) ゲート•ソース間に内蔵のツェナーダイオードは、種々の条件下において完全にゲートの静電破壊を防止できるものではありません。このため素子を取扱う場合、人体や半田ゴテなどにアースを接続していただくようお願いいたします。

NEW PRODUCT

POWER MOS FET ARRAY

HF9913
(4AK15)

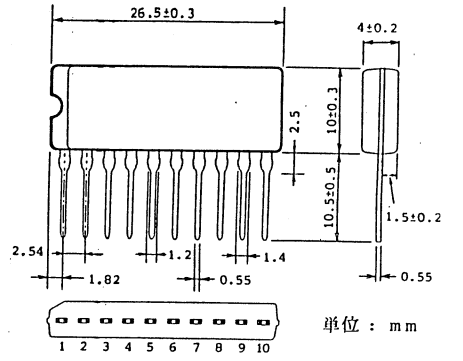
シリコン Nチャネル パワーMOS FET アレイ
高速度電力スイッチング

—Product Preview—

特長

- 低オン抵抗
  $R_{DS(on)} \leqq 0.07\Omega$, $V_{GS}=10V$, $I_D=8A$
  $R_{DS(on)} \leqq 0.095\Omega$, $V_{GS}=4V$, $I_D=8A$
- 低電圧駆動
  4V駆動が可能なため、5V系電源(マイコン, TTL)から直接ドライブできます。
- 駆動電力が小さい。(パワーMOS FET 搭載)
- スイッチング速度が速い。
- リード端子間隔が2.54mm(0.1インチ)のためプリント基板実装が容易です。
- マルチチップパワーMOS FETをシングルインラインの小形パッケージに搭載しているため、高密度実装が可能です。

外形図



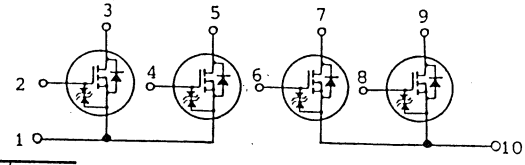
単位：mm

用途

- モータ, ソレノイド, ランプの駆動用などに最適です。

単体相当品種 ; 2SK971, 2SK977, 2SK1094

内部等価回路



電極接続

2, 4, 6, 8 ; ゲート (Gate)
3, 5, 7, 9 ; ドレイン(Drain)
1, 10 ; ソース (Source)

■絶対最大定格(Ta=25℃)

項目	記号	定格	単位
ドレイン・ソース電圧	V_{DSS}	60	V
ゲート・ソース電圧	V_{GSS}	±20	V
ドレイン電流	I_D	8	A/unit
ドレインピーク電流	$I_{D(pulse)}$*	32	A/unit
逆ドレイン電流	I_{DR}	8	A/unit
チャネル損失	Pch**	28	W
チャネル損失	Pch	3.5	W
チャネル温度	Tch	150	℃
保存温度	Tstg	-55～+150	℃

*PW≦10μs, duty cycle≦1%　**Tc=25℃

Product Preview : This document contains information on a product under development. Hitachi reserves the right to change or discontinue the product without notice.
開発中の製品のデータシートです。この製品は予告なく変更、廃止されることがあります。

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.
新製品のデータシートです。掲載内容は、予告なく変更されることがあります。

HITACHI

'88-01-25

■電気的特性(Ta＝25℃)　　* Pulse Test

項目	記号	測定条件	min.	typ.	max.	単位
ドレイン・ソース破壊電圧	$V_{(BR)DSS}$	I_D＝10mA, V_{GS}＝0	60	—	—	V
ゲート・ソース破壊電圧	$V_{(BR)GSS}$	I_G＝±100μA, V_{DS}＝0	±20	—	—	V
ゲート・ソース漏れ電流	I_{GSS}	V_{GS}＝±16V, V_{DS}＝0	—	—	±10	μA
ドレイン・ソースリーク電流	I_{DSS}	V_{DS}＝50V, V_{GS}＝0	—	—	250	μA
ゲート・ソース遮断電圧	$V_{GS(off)}$	I_D＝1mA, V_{DS}＝10V	1.0	—	2.0	V
ドレイン・ソースオン抵抗	$R_{DS(on)}$	I_D＝8A, V_{GS}＝10V *	—	0.055	0.07	Ω
		I_D＝8A, V_{GS}＝4V *	—	0.075	0.095	Ω
順伝達アドミタンス	$\|yfs\|$	I_D＝8A, V_{DS}＝10V *	7	12	—	S
入力容量	Ciss	V_{DS}＝10V, V_{GS}＝0	—	860	—	pF
出力容量	Coss	f＝1MHz	—	450	—	pF
逆伝達容量	Crss		—	140	—	pF
ターンオン遅延時間	td(on)		—	10	—	ns
上昇時間	tr	I_D＝8A, V_{GS}＝10V	—	70	—	ns
ターンオフ遅延時間	td(off)	R_L＝3.75Ω	—	180	—	ns
下降時間	tf		—	120	—	ns
ボディドレインダイオード順方向電圧	V_{DF}	I_F＝8A, V_{GS}＝0	—	1.05	—	V
ボディドレインダイオード逆回復時間	trr	I_F＝8A, V_{GS}＝0 dI_F/dt＝50A/μs	—	110	—	ns

NEW PRODUCT

POWER MOS FET ARRAY

HF9915
(4AH16)

シリコン Nチャネル パワーMOS FET アレイ
高速度電力スイッチング

—Product Preview—

特長

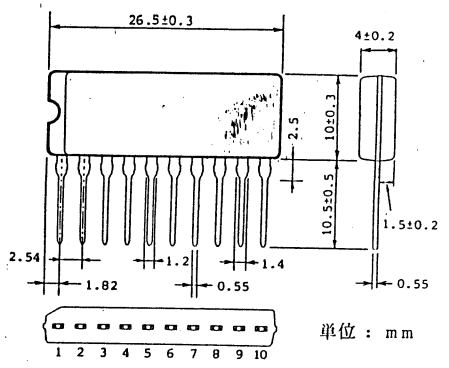
- 低オン抵抗
  $R_{DS(on)} \leqq 0.18\,\Omega$, $V_{GS}=10V$, $I_D=5A$
  $R_{DS(on)} \leqq 0.25\,\Omega$, $V_{GS}=4V$, $I_D=5A$
- 低電圧駆動
  4V駆動が可能なため、5V系電源(マイコン, TTL)から直接ドライブできます。
- 駆動電力が小さい。(パワーMOS FET 搭載)
- スイッチング速度が速い。
- リード端子間隔が2.54mm(0.1インチ)のためプリント基板実装が容易です。
- マルチチップパワーMOS FETをシングルインラインの小形パッケージに搭載しているため、高密度実装が可能です。

用途

- モータ, ソレノイド, ランプの駆動用などに最適です。

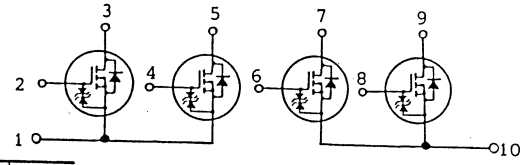
単体相当品種 ; 2SK970, 2SK976, 2SK1093
2SK974Ⓐ, 2SK974Ⓢ

外形図



単位 : mm

内部等価回路



電極接続

2, 4, 6, 8 ; ゲート (Gate)
3, 5, 7, 9 ; ドレイン(Drain)
1, 10 ; ソース (Source)

■絶対最大定格(Ta=25℃)

項目	記号	定格	単位
ドレイン・ソース電圧	V_{DSS}	60	V
ゲート・ソース電圧	V_{GSS}	±20	V
ドレイン電流	I_D	5	A/unit
ドレインピーク電流	$I_{D(pulse)}$*	20	A/unit
逆ドレイン電流	I_{DR}	5	A/unit
チャネル損失	Pch**	28	W
チャネル損失	Pch	3.5	W
チャネル温度	Tch	150	℃
保存温度	Tstg	-55～+150	℃

*PW≦10μs, duty cycle≦1% **Tc=25℃

Product Preview : This document contains information on a product under development. Hitachi reserves the right to change or discontinue the product without notice.
開発中の製品のデータシートです。この製品は予告なく変更、廃止されることがあります。

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.
新製品のデータシートです。掲載内容は、予告なく変更されることがあります。

HITACHI

'88-01-25

■電気的特性(Ta＝25℃)　　* Pulse Test

項　目	記号	測定条件	min.	typ.	max.	単位
ドレイン・ソース破壊電圧	$V_{(BR)DSS}$	I_D＝10mA, V_{GS}＝0	60	—	—	V
ゲート・ソース破壊電圧	$V_{(BR)GSS}$	I_G＝±100μA, V_{DS}＝0	±20	—	—	V
ゲート・ソース漏れ電流	I_{GSS}	V_{GS}＝±16V, V_{DS}＝0	—	—	±10	μA
ドレイン・ソースリーク電流	I_{DSS}	V_{DS}＝50V, V_{GS}＝0	—	—	100	μA
ゲート・ソース遮断電圧	$V_{GS(off)}$	I_D＝1mA, V_{DS}＝10V	1.0	—	2.0	V
ドレイン・ソースオン抵抗	$R_{DS(on)}$	I_D＝5A, V_{GS}＝10V *	—	0.12	0.18	Ω
		I_D＝5A, V_{GS}＝4V *	—	0.17	0.25	Ω
順伝達アドミタンス	$\|yfs\|$	I_D＝5A, V_{DS}＝10V *	3.5	6.0	—	S
入力容量	Ciss	V_{DS}＝10V, V_{GS}＝0	—	400	—	pF
出力容量	Coss	f＝1MHz	—	220	—	pF
逆伝達容量	Crss		—	60	—	pF
ターンオン遅延時間	td(on)		—	5	—	ns
上昇時間	tr	I_D＝5A, V_{GS}＝10V	—	55	—	ns
ターンオフ遅延時間	td(off)	R_L＝6Ω	—	140	—	ns
下降時間	tf		—	90	—	ns
ボディドレインダイオード順方向電圧	V_{DF}	I_F＝5A, V_{GS}＝0	—	1.0	—	V
ボディドレインダイオード逆回復時間	trr	I_F＝5A, V_{GS}＝0 dI_F/dt＝50A/μs	—	100	—	ns

NEW PRODUCT

POWER MOS FET ARRAY

HF9917

シリコン Nチャネル パワーMOS FET アレイ
高速度電力スイッチング

—Product Preview—

特長

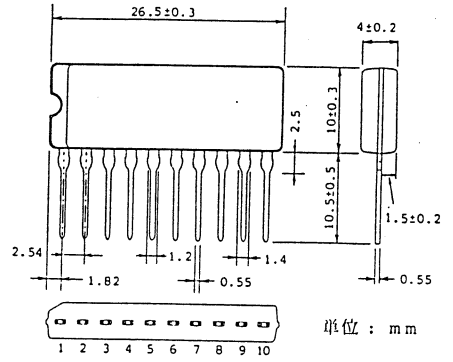
- 低オン抵抗
  $R_{DS(on)} \leqq 0.35\,\Omega$, $V_{GS}=10V$, $I_D=1A$
  $R_{DS(on)} \leqq 0.50\,\Omega$, $V_{GS}=4V$, $I_D=1A$
- 低電圧駆動
  4V駆動が可能なため、5V系電源(マイコン, TTL)から直接ドライブできます。
- 駆動電力が小さい。(パワーMOS FET 搭載)
- スイッチング速度が速い。
- リード端子間隔が2.54mm(0.1インチ)のためプリント基板実装が容易です。
- マルチチップパワーMOS FETをシングルインラインの小形パッケージに搭載しているため、高密度実装が可能です。

用途

- モータ, ソレノイド, ランプの駆動用などに最適です。

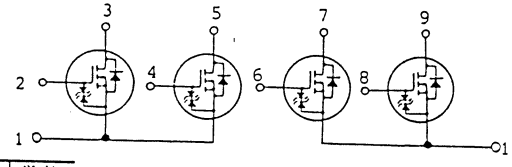
単体相当品種 ; 2SK973Ⓛ, 2SK973Ⓢ

外形図



単位 : mm

内部等価回路



電極接続

2, 4, 6, 8 ; ゲート (Gate)
3, 5, 7, 9 ; ドレイン(Drain)
1, 10 ; ソース (Source)

■絶対最大定格($T_a=25℃$)

項目	記号	定格	単位
ドレイン・ソース電圧	V_{DSS}	60	V
ゲート・ソース電圧	V_{GSS}	±20	V
ドレイン電流	I_D	2.5	A/unit
ドレインピーク電流	$I_{D(pulse)}$*	10	A/unit
逆ドレイン電流	I_{DR}	2.5	A/unit
チャネル損失	Pch**	28	W
チャネル損失	Pch	3.5	W
チャネル温度	Tch	150	℃
保存温度	Tstg	−55～+150	℃

*PW≦10μs, duty cycle≦1%　**Tc=25℃

Product Preview : This document contains information on a product under development. Hitachi reserves the right to change or discontinue the product without notice.
開発中の製品のデータシートです。この製品は予告なく変更、廃止されることがあります。

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.
新製品のデータシートです。掲載内容は、予告なく変更されることがあります。

HITACHI

'88-01-25

■電気的特性(Ta＝25℃)　　* Pulse Test

項目	記号	測定条件	min.	typ.	max.	単位
ドレイン・ソース破壊電圧	$V_{(BR)DSS}$	I_D＝10mA, V_{GS}＝0	60	—	—	V
ゲート・ソース破壊電圧	$V_{(BR)GSS}$	I_G＝±100μA, V_{DS}＝0	±20	—	—	V
ゲート・ソース漏れ電流	I_{GSS}	V_{GS}＝±16V, V_{DS}＝0	—	—	±10	μA
ドレイン・ソースリーク電流	I_{DSS}	V_{DS}＝50V, V_{GS}＝0	—	—	100	μA
ゲート・ソース遮断電圧	$V_{GS(off)}$	I_D＝1mA, V_{DS}＝10V	1.0	—	2.0	V
ドレイン・ソースオン抵抗	$R_{DS(on)}$	I_D＝1A, V_{GS}＝10V *	—	0.25	0.35	Ω
		I_D＝1A, V_{GS}＝4V *	—	0.40	0.50	Ω
順伝達アドミタンス	$\|yfs\|$	I_D＝1A, V_{DS}＝10V *	1.2	2.0	—	S
入力容量	Ciss	V_{DS}＝10V, V_{GS}＝0	—	240	—	pF
出力容量	Coss	f＝1MHz	—	115	—	pF
逆伝達容量	Crss		—	35	—	pF
ターンオン遅延時間	td(on)		—	4	—	ns
上昇時間	tr	I_D＝1A, V_{GS}＝10V	—	15	—	ns
ターンオフ遅延時間	td(off)	R_L＝30Ω	—	80	—	ns
下降時間	tf		—	40	—	ns
ボディドレインダイオード順方向電圧	V_{DF}	I_F＝2A, V_{GS}＝0	—	1.0	—	V
ボディドレインダイオード逆回復時間	trr	I_F＝2A, V_{GS}＝0 dI_F/dt＝50A/μs	—	70	—	ns

NEW PRODUCT

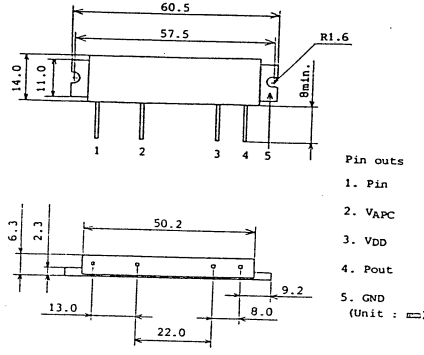
PF0010

MOSFET POWER AMPLIFIER
UHF BAND

—Preliminary—

FEATURES:

1. Included input and output matching circuit.
2. Easy to control output power.
3. Superior to stability at load mismatching.



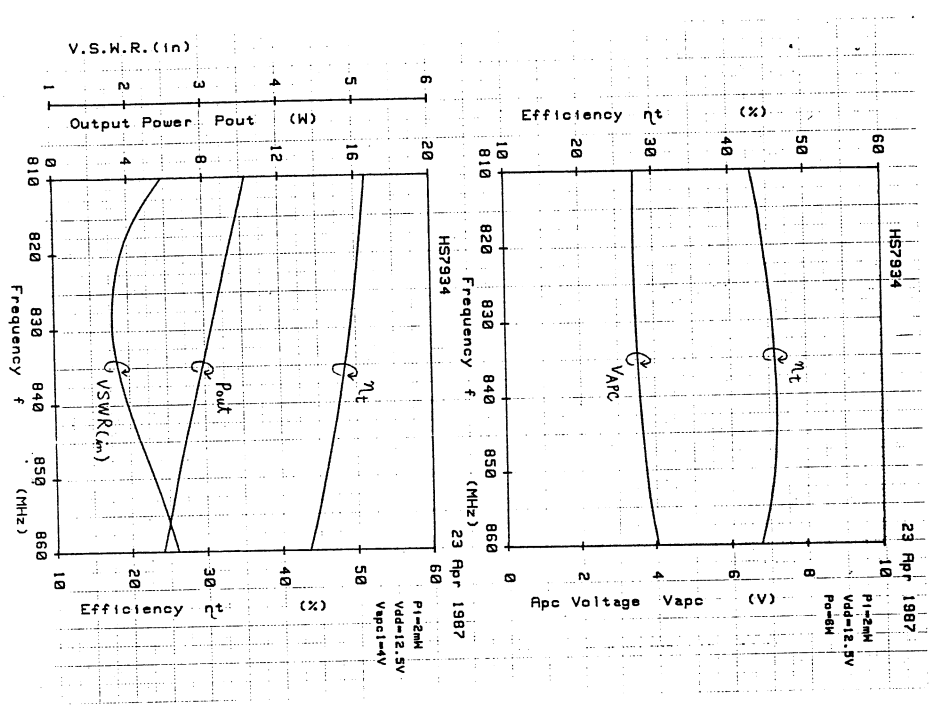
ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

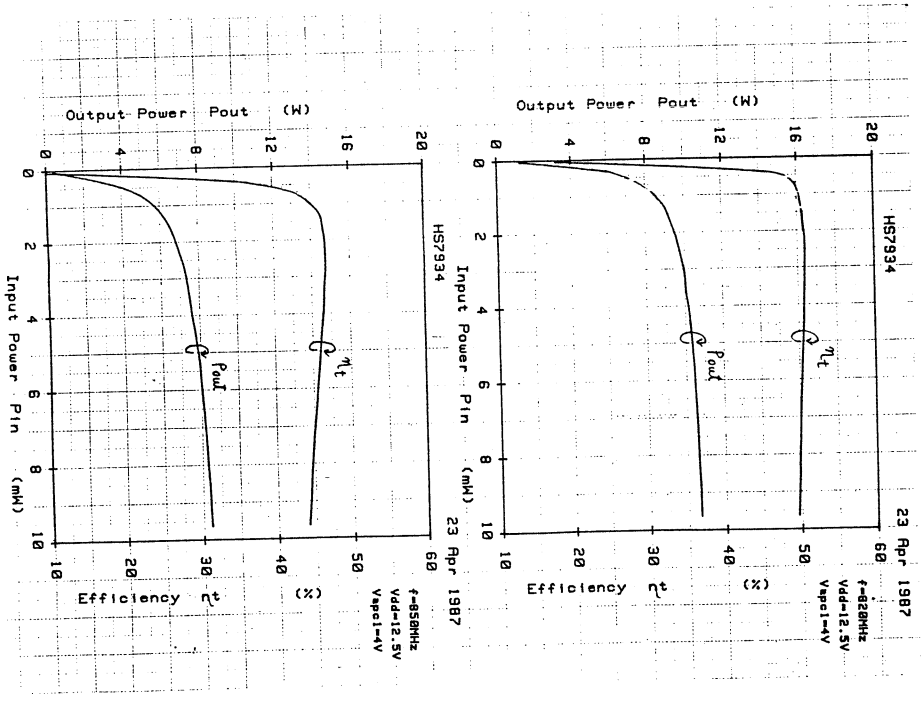
Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	17	V
Maximum Circuit Current	I_D	3.0	A
APC Voltage	V_{APC}	8	V
Maximum Input Power	Pin	20	mW
Operating Maximum Case Temperature	$T_{C(op)}$	−40 ~ +100	℃
Storage Temperature	Tstg	−45 ~ +125	℃

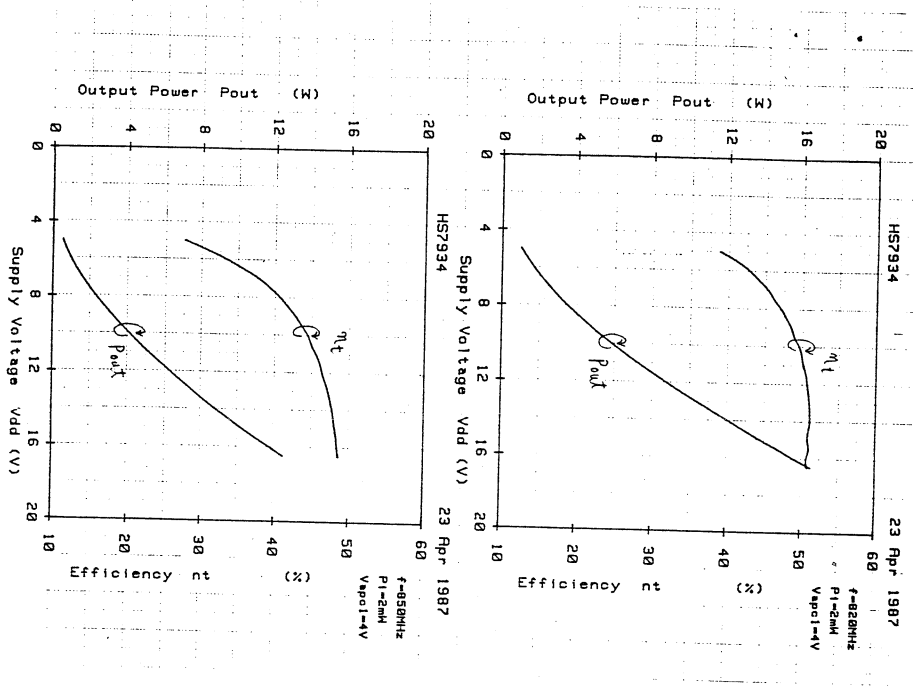
ELECTRICAL CHARACTERISTICS (Ta=25℃)

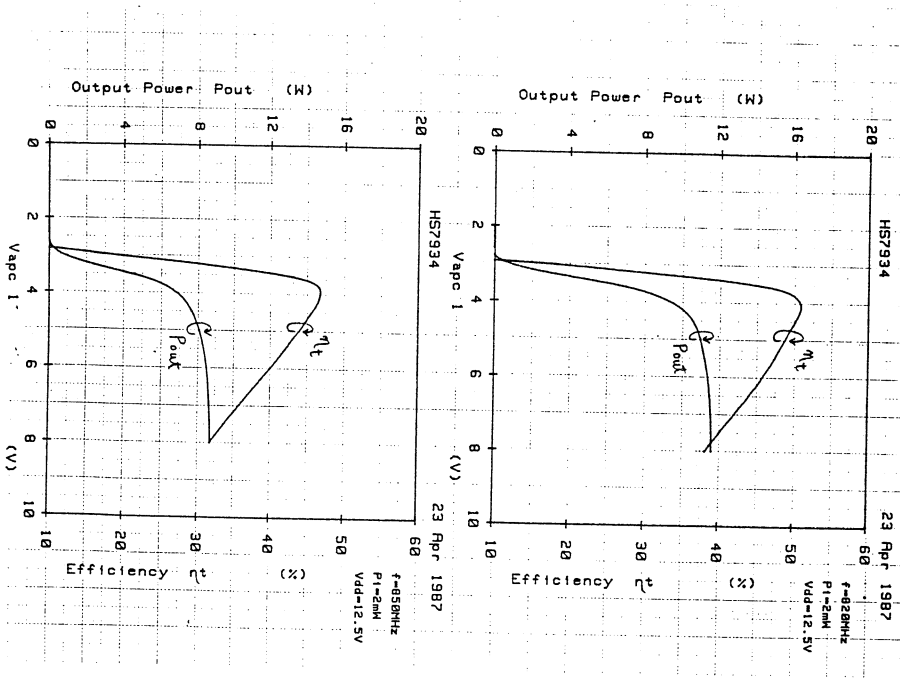
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	$V_{DD1}=V_{DD2}=17V$, $V_{APC}=0$	—	—	500	μA
Total Efficiency	η_T	f=820,850MHz, Pin=2mW, V_{DD}=12.5V, Pout=6W(at APC Control) Zin=Zout=50Ω	35	40	—	%
2nd Harmonic Distortion	2nd H.D.		—	−50	−30	dB
3rd Harmonic Distortion	3rd H.D.		—	−50	−30	dB
Input VSWR	VSWR(in)		—	1.5	3.0	—
Output VSWR	VSWR(out)		—	1.5	—	—
Stability	—	V_{DD}=12.5V, Pin=2mW, f=820MHz, Pout=6W(at APC Control), Rg=50Ω, Output VSWR=∞ All Phase, t=20sec	No Parastic Oscillation			—

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.


V.S.W.R.(in)
Output Power Pout (W)
Frequency f (MHz)
VSWR(in)
Pout
ηt
Efficiency ηt (%)
HS7934
23 Apr 1987
Pi=2mW
Vdd=12.5V
Vapc1=4V
Apc Voltage Vapc (V)
VAPC
Po=6W


Output Power Pout (W)
Input Power Pin (mW)
Pout
ηt
Efficiency ηt (%)
HS7934
23 Apr 1987
f=820MHz
f=850MHz
Vdd=12.5V
Vapc1=4V


HS7934
23 Apr 1987
Output Power Pout (W)
Efficiency ηt (%)
Supply Voltage Vdd (V)
Pout
ηt
f=820MHz
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HS7934
23 Apr 1987
Output Power Pout (W)
Efficiency ηt (%)
Vapc 1 (V)
Pout
ηt
f=820MHz
Pi=2mW
Vdd=12.5V
f=850MHz
Pi=2mW
Vdd=12.5V

NEW PRODUCT

PF0011
(HS7938)

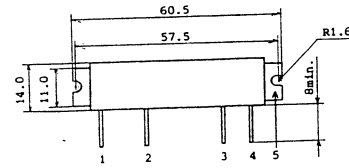
MOSFET POWER AMPLIFIER

UHF BAND

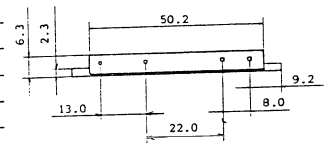
—Preliminary—

■ FEATURES:

1. Included input and output matching circuit.
2. Easy to control output power.
3. Superior to stability at load mismatching.



Pin outs
1. Pin
2. V_{APC}
3. V_{DD}
4. Pout
5. GND
(Unit : mm)



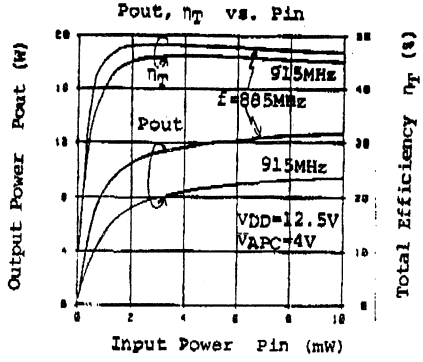
■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

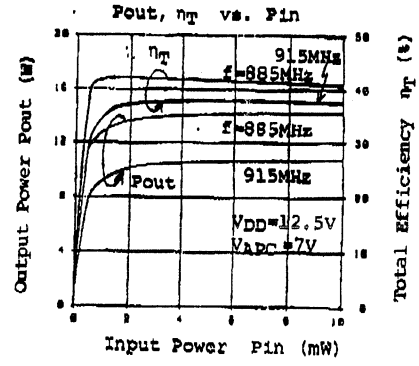
Item	Symbol	Rating	Unit
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Maximum Input Power	Pin	20	mW
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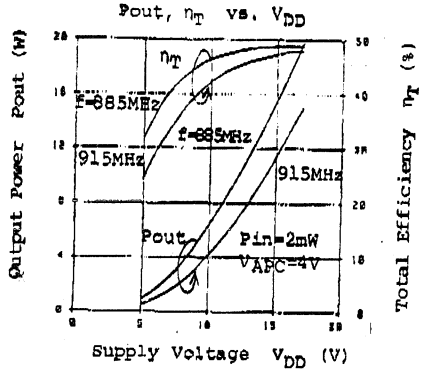
■ ELECTRICAL CHARACTERISTICS (Ta=25℃)

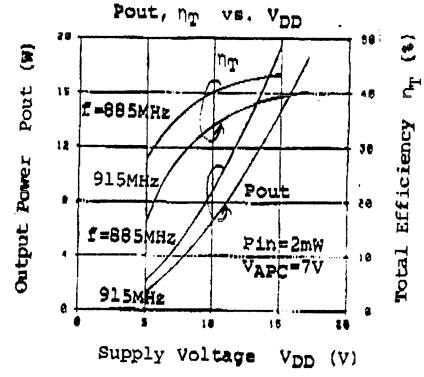
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	$V_{DD1}=V_{DD2}=17V$, $V_{APC}=0$	—	—	500	μA
Total Efficiency	η_T	f=890,915MHz, Pin=2mW, V_{DD}=12.5V, Pout=6W(at APC Control) Zin=Zout=50Ω	35	40	—	%
2nd Harmonic Distortion	2nd H.D.		—	−50	−30	dB
3rd Harmonic Distortion	3rd H.D.		—	−50	−30	dB
Input VSWR	VSWR(in)		—	1.5	3.0	—
Output VSWR	VSWR(out)		—	1.5	—	—
Output Power	Pout	f=890,915MHz, Pin=2mW, V_{DD}=7V, $V_{APC}\leqq 7V$, Zin=Zout=50Ω	1.0	—	—	W
Stability	—	V_{DD}=12.5V, Pin=2mW, f=890MHz, Pout=6W(at APC Control), Rg=50Ω, Output VSWR=∞ All Phase, t=20sec	No Parastic Oscillation			—

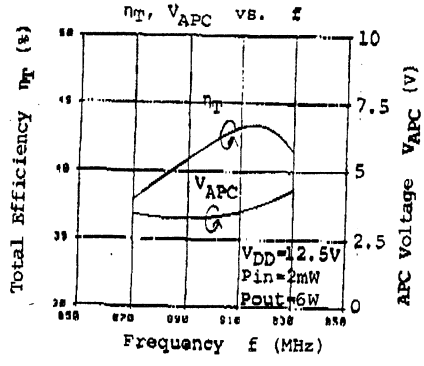
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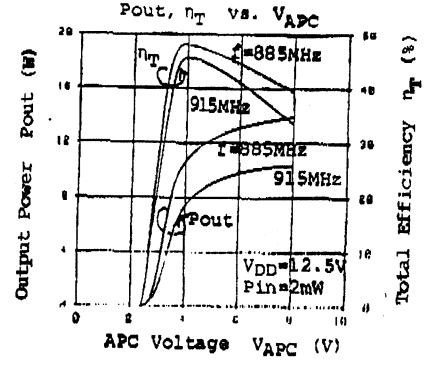

Pout, η_T vs. Pin
Output Power Pout (W)
Total Efficiency η_T (%)
η_T
915MHz
f=885MHz
Pout
915MHz
VDD=12.5V
VAPC=4V
Input Power Pin (mW)

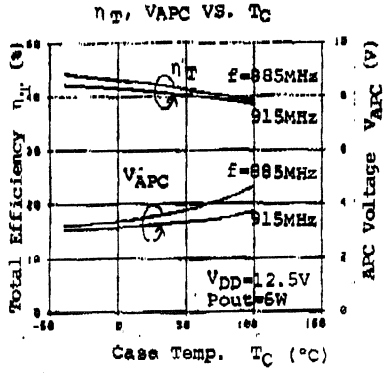

Pout, η_T vs. Pin
Output Power Pout (W)
Total Efficiency η_T (%)
η_T
915MHz
f=885MHz
f=885MHz
Pout
915MHz
VDD=12.5V
VAPC=7V
Input Power Pin (mW)


Pout, η_T vs. V_{DD}
Output Power Pout (W)
Total Efficiency η_T (%)
η_T
f=885MHz
915MHz
f=885MHz
915MHz
Pout
Pin=2mW
VAPC=4V
Supply Voltage V_{DD} (V)

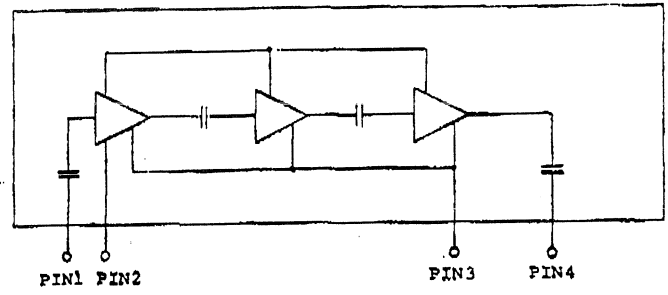

Pout, η_T vs. V_{DD}
Output Power Pout (W)
Total Efficiency η_T (%)
η_T
f=885MHz
915MHz
Pout
f=885MHz
Pin=2mW
VAPC=7V
915MHz
Supply Voltage V_{DD} (V)


η_T, V_{APC} vs. f
Total Efficiency η_T (%)
APC Voltage V_{APC} (V)
10
7.5
5
2.5
0
η_T
V_{APC}
VDD=12.5V
Pin=2mW
Pout=6W
Frequency f (MHz)

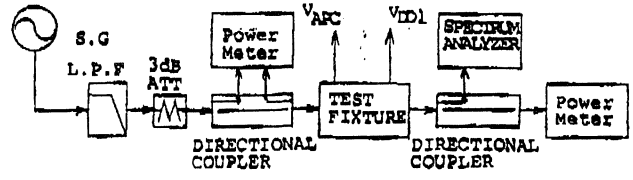

Pout, η_T vs. V_{APC}
Output Power Pout (W)
Total Efficiency η_T (%)
η_T
f=885MHz
915MHz
f=885MHz
915MHz
Pout
VDD=12.5V
Pin=2mW
APC Voltage V_{APC} (V)



■ INTERNAL DIAGRAM



■ TEST SYSTEM DIAGRAM



POWER-MOS FET APPLICATION NOTE

INDEX

APPLICATION HINTS 451

1. Audio Power Amplifier 451

1.1 Linear Power Amplifier 451
1.2 PWM (Pulse Width Modulation) Amplifier 457

2. High Speed Power Switching 463

2.1 Switching Regulator 463
2.2 High Speed Drive Circuit 477

3. High Frequency Power Amplifier 480

3.1 1kW Medium Wave Broadcasting Transmitter 481
3.2 600W Short Wave Broadcasting Transmitter 483
3.3 VHF High Power Amplifier Circuit 484

4. Motor Control 492

5. Analog Switch 500

6. Character Display 503

6.1 Features 503
6.2 Application Notes 505

7. Ultrasonic Equipment 507

8. Others 508

NOTICE
The example of an applied circuit or combination with other equipment shown herein indicates characteristics and performance of a semiconductor-applied products. The Company shall assume no responsibility for any problem involving a patent caused when applying the descriptions in the example.

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1 Audio Power Amplifier

1.1 Linear Power Amplifier

(1) Design of output stage (Design of power supply voltage V_{DD})

Fig. 4-1 shows an equivalent circuit of the output stage. R_{ON} is a drain-to-source equivalent resistance when the power MOS FET is on, and according to the 2SK134/2SJ49 spec, it is;

$$R_{ON} = \frac{V_{DS(sat)}}{I_D} = \frac{12}{7} = 1.71\,\Omega$$

The peak current I_p flowing through load R_L=8Ω at Po=100W is calculated from mean current I,

$$P_O = I^2 R_L$$

$$I_p = \sqrt{2} \cdot I = \sqrt{\frac{2P_o}{R_L}}$$

$$= \sqrt{\frac{200}{8}} = 5\ A$$

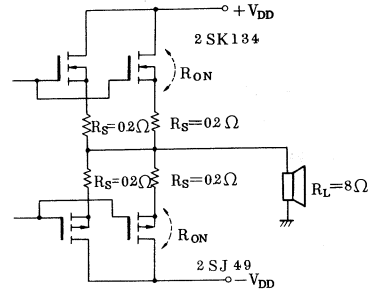


Fig. 4-1 Equivalent Circuit of the Output Stage

Therefore, if the transformer regulation is estimated at 20% and the AC line regulation at ±15%, then the power supply voltage V_{DD} is given as;

$$V_{DD} = 1.2 \times 1.15 \left\{ R_L + \frac{(R_{ON} + R_s)}{2} \right\} I_p$$

$$\fallingdotseq 61.8\ V$$

In Fig. 4-3, the power supply of power stage is common with that of voltage amplifier stage, so the voltage is set at ±65V including the gate-to-source ON voltage at Po=100W.

In the case of D series 2SK343/2SJ99, the R_{ON} value is very small (0.5Ω), the supply voltage required for the same output (100W) is only 57.6V. This enables us to make the transformer capacity and the cooling fin smaller, resulting in cost reduction.

(2) Design of voltage amplifier stage

A power MOS FET can be driven by a low driving power. Fundamentally, only power for charging and discharging the gate-to-source capacitance is needed by the output stage, so that a class B driver stage is not required. The driving power varies with input frequency. At 100W output and 100kHz frequency, it would be very small as follows.

$$Pin = f \cdot Ciss \cdot V_{GS}{}^2 = 100 \times 10^3 \times 900 \times 10^{-12} \times 6^2 = 3.24\,mW$$

Therefore, an output stage power MOS FET can be driven directly from a class A predriver (voltage amplifier stage) used in a bipolar transistor amplifier. By eliminating the class B driver, the quantity of components can be reduced, and impairment of the amplifier's performance by the driver itself can be avoided. Moreover, the number of poles in the transfer function (open loop gain vs. frequency characteristics) decreases, and the stagger can easily be increased. Consequently, the stability against oscillation is improved. Transistors for the voltage amplifier stage are required to have a high breakdown voltage, low Cob (collector output capacitance) and high f_T (gain-bandwidth product).

(3) Open loop voltage gain

The transconductance $|y_{fs}|$ of power MOS FETs is as large as 1.0 ∿ 2.5S typ. Yet it is only a fraction of that of bipolar transistors. For example, $|y_{fs}|$ of bipolar transistors at I_C (collector current)= 1.0A, is very large, as follows;

$$|y_{fe}| = \frac{1}{r_e} = \frac{I_E}{KT/q} = \frac{1\,A}{26\,mV} \fallingdotseq 38\,S$$

where re: Emitter equivalent resistance
K: Boltzmann constant
T: Absolute temperature
q: Electron charge
I_E: Emitter bias current

When the power device is used in the source follower (In bipolar transistor circuit; it's called emitter follower), the relationship between input and output is;

$$\frac{\text{output}}{\text{input}} \fallingdotseq \frac{R_L}{R_L + 1/|y_{fs}|}$$

(See Fig. 4-2)

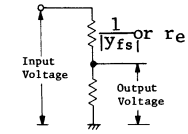


Fig. 4-2 Source Follower Input & Output

Only the nonlinear component of this equation, $1/|y_{fs}|$, causes distortion, so that a larger $|y_{fs}|$ is of lower distortion. In other words, since a power MOS FET amplifier has a distortion about 20dB larger than a bipolar transistor amplifier, it is necessary to design for larger open loop gain and larger negative feedback than in a bipolar transistor circuit.

(4) Considerations for parasitic oscillation

Because power MOS FETs have excellent high-frequency characteristics, they are liable to cause oscillation, even in a simple circuit.

For an analysis of stability in a source follower circuit, see paragraph 5.9 of Power MOS FET Data Book (MAR, 1985). Here, we would like to show some precautions in fabrication.

- Minimize the wiring between the printed circuit board and the power MOS FETs. Direct connection is recommended.
- Provide one-point grounding for the amplifier printed circuit, power supply, and speaker terminals. Make the wiring of power supply line and ground line as big as possible.
- The output coupling coil L has the effect of reducing distortion in the high frequency range. It also prevents oscillation which might occur when the output is loaded by capacitance. Its value should be determined experimentally.
- Printed circuit layout should flow topographically from input to output.

(5) Line up

Table 4-1 Line-up of Devices in Audio Amplifier

Output Power		Input Stage			Driver Stage				Output Stage	
			Bipolar		FET (V_{DSX})		Bipolar (V_{CEO})		FET (V_{DSX})	
Single Pushpull	Parallel Pushpull	FET	NPN	PNP	N Channel	P Channel	NPN	PNP	N Channel	P Channel
50~60	—	2SK190 2SK186	2SC1775 2SC2855	2SA872 2SA1190	2SK213 (140V)	2SJ76 (−140V)	2SD756 (120V)	2SB716 (−120V)	2SK133 (120V)	2SJ48 (−120V)
60~80	100~120				2SK214 (160V)	2SJ77 (−160V)	2SD756A (140V)	2SB716A (−140V)	2SK134 (140V) 2SK413 (140V)	2SJ49 (−140V) 2SJ118 (−140V)
—	120~140	—			2SK215 (180V)	2SJ78 (−180V)	2SD668A (160V)	2SB648A (−160V)	2SK135 (160V) 2SK414 (160V)	2SJ50 (−160V) 2SJ119 (−160V)
80~100	—				2SK216 (200V)	2SJ79 (−200V)	2SD758 (200V)	2SB718 (−200V)	2SK175 (180V)	2SJ55 (−180V)
—	140~200	—	2SC1775A 2SC2856	2SA872A 2SA1191	—	—			2SK400 (200V) 2SK176 (200V)	2SJ114 (−200V) 2SJ56 (−200V)

Underline is D Series (Drain Case Type)

(6) Application Circuit

● 100W Output THD≒0.01%, f=100kHz

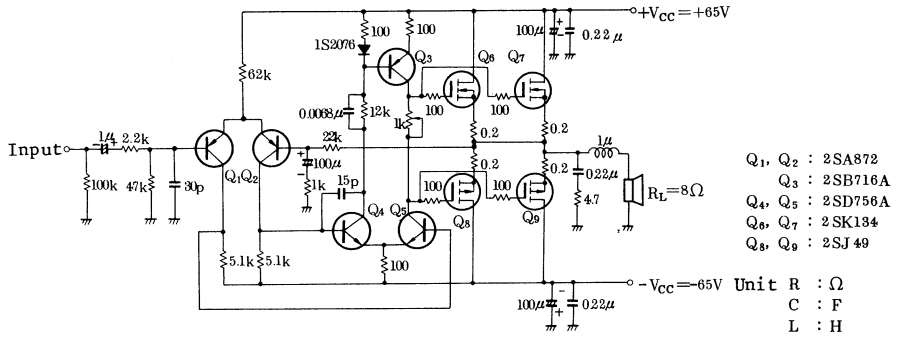


Fig. 4-3 P_O=100W Power Amp. Circuit Diagram

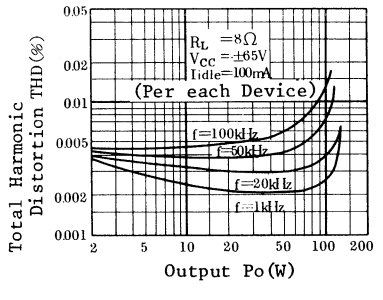


Fig. 4-4 Total Harmonic Distortion vs. Output Characteristics

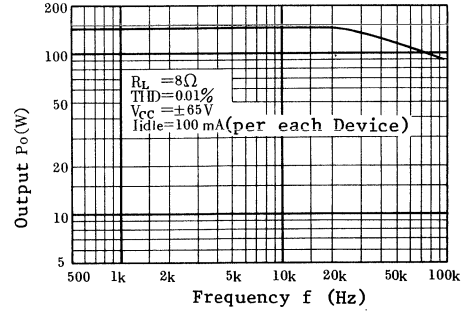


Fig. 4-5 Power Band Width

● 100W Output THD≒0.01%, f=50kHz
(All FET DC Amplifier)

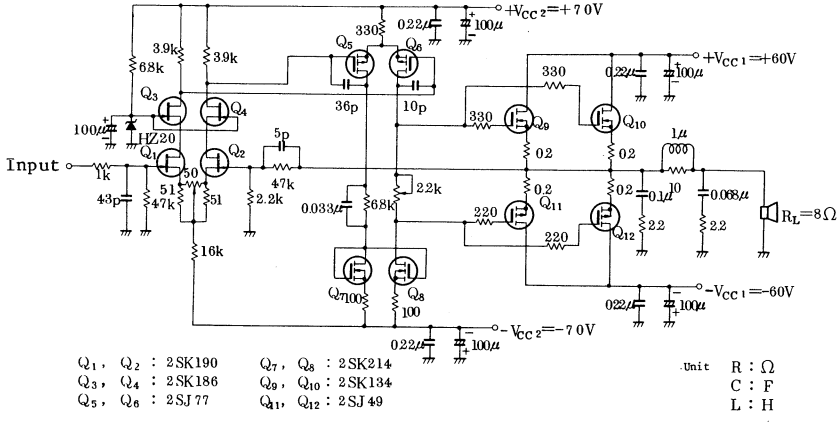


Fig. 4-6 Po=100W All FET Power Amp. Circuit Diagram

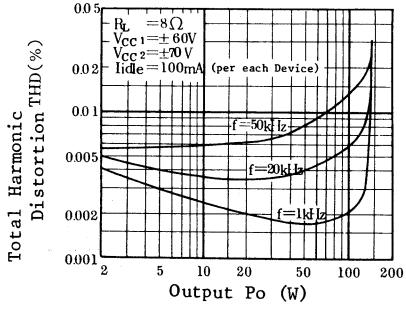


Fig. 4-7 Total Harmonic Distortion vs. Output Characteristics

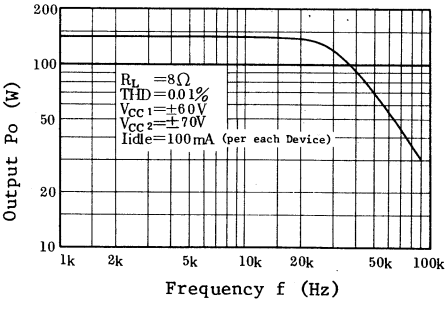


Fig. 4-8 Power Band Width

1.2 PWM Amplifier

The PWM (Pulse Width Modulation) Amplifier is a signal reproducing system in which a input signal is converted to a pulse signal whose width or duty cycle is proportional to the input signals amplitude. This variable duty cycle but constant amplitude signal is amplified, low pass filtered, and then applied to the load, losses are primarilly switching losses in the output devices. This allows a very high output power with very small physical size.

The most important characteristic required for a output device in a PWM amplifier is high switching speed. The t_{off} speed of a bipolar transistor is slower than that of a power MOS FET of similar power rating. The t_{off} ($t_{off}=t_{d(off)}+t_f$) value of a power MOS FET is only 100 ∿ 200ns, giving it an advantage in PWM switching operation of several hundred kHz.

(1) Theory & Block Diagram of PWM Amplifier

Fig. 4-9 and Fig. 4-10 show the block diagram and the waveform of a PWM amplifier.

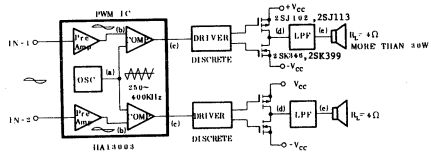


Fig. 4-9 PWA Amp. Block Diagram

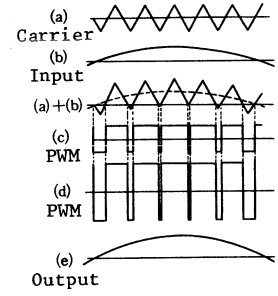


Fig. 4-10 Waveform

In this PWM amplifier, the input signal (b) is added to the carrier signal (a) (a triangular wave) through a comparator, and then that signal ((a) + (b)) is converted to a pulse signal whose pulse width is proportional to the input signal level. This means that the pulse duty cycle is proportional to the input signal level.

The pulse signal (c) drives the output power devices. The power devices switch the power supply, and the resulting output power is passed to a low pass filter (hereinafter referred to as LPF). The original signal input (b) is reproduced amplified (e) at the output of the LPF.

When the frequency of carrier signal (a) is higher, the quantity of information is more accurate and the distortion is lower. According to information theory, if the frequency is more than twice as high as the maximum transmission frequency, the original frequency can be reproduced. In the PWM amplifier, however, the distortion will be worse, because the lower side band is mixed into the audio signal. Therefore, if the maximum transmission frequency is 20 ∿ 50kHz, the carrier frequency should be normally 200 ∿ 500kHz (5 ∿ 10 times).

(2) Power Efficiency of PWM Amplifier

In a class-B amplifier, the amplification device operates as a resistance, so the device loss is large. On the other hand, in a PWM amplifier, since the switch is connected directly to the power supply, and the voltage-current product in a ideal switch is always 0, there is no loss. In fact, however, there is loss proportional to the output, because of the ON resistance (R_{ON}) of the switch and the switching delay time.

Fig. 4-11 shows the efficiency vs. output power characteristics. Compared with a class-B amplifier, the efficiency of a PWM amplifier is better, under stated conditions.

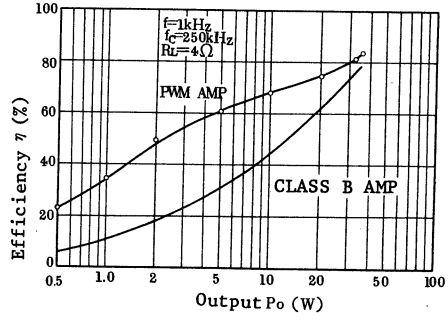


Fig. 4-11 Efficiency vs. Output Characteristics

(3) Relation between output power device and distortion

Distortion in a PWM amplifier occurs, under the influences of; 1) frequency of carrier signal, 2) linearity of triangular wave and 3) attenuation of LPF. In this section, we would like to explain the distortion that occurs at the output stage of the power switching circuit.

Fig. 4-12 shows a PWM output circuit in which power MOS FET's are used, and Fig. 4-13, the operating waveforms.

(a) shows driving voltage waveform (Vi) and (b) ∿ (e), voltage and current waveform at each point. The current can't be changed instantaneously because of the LPF's inductance, resulting in the waveform shown in (e). Examining the current more minutely, from t_1 to t_2, Q_1 is in ON state and forward current (i_1) flows. As soon as the Q_1 turns OFF, a inverse voltage is generated by the LPF's inductance and to absorb it, current (i_2) flows through the Q_2 diode ($t_2 \sim t_3$). Then Q_2 turns ON and forward current (i_3) flows ($t_3 \sim t_4$). Then current (i_4) flows through the Q_1 diode ($t_4 \sim t_5$). The current flows repeating the above operations. Here, the important point is that the current can flow backward. This means that a power MOS FET does not require an external commutating diode because it has an equivalent backward diode. On the other hand, if a bipolar transistor is used in the output stage, an external diode is needed.

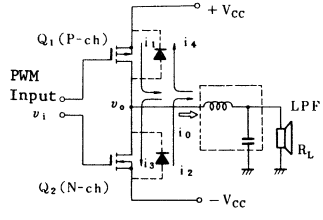


Fig. 4-12 Equivalent Circuit of PWM Output Stage

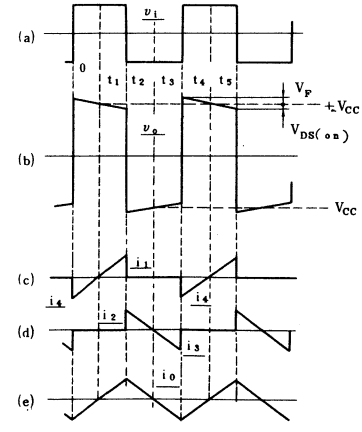


Fig. 4-13 Waveform (Unmodulated)

As for the voltage waveform (V_o), the remaining voltage $V_{DS(on)}$ and the backward diode V_F of power MOS FET cause amplitude fluctuation of the output voltage. Therefore the waveform as shown in (b) is generated, instead of a correct square wave.

When a input signal is supplied, the pulse width is modulated and power is provided to the speaker, the current flown to LPF is as shown in Fig. 4-14. The output waveform is determined like this; if the triangular current is positive, it is determined by the forward current of P channel and the backward current of N channel, and if the triangular current is negative, it is determinend by the forward current of N channel and the backward current of P channel.

As for the MOS FET output characteristics (V_{DS} vs. I_D characteristics), in the standard MOS FET, as shown by the dotted line in Fig. 4-15, the diode characteristics are seen in the reverse area. Because of this non-linear characteristics, the voltage drop of the output pulse is non-linear and a distortion is caused. Therefore a device is required to have the same forward and backward characteristics.

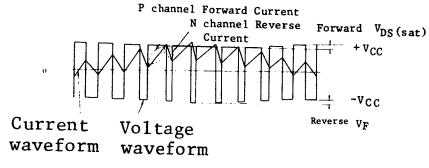


Fig. 4-14 Output Waveform (Modulated)

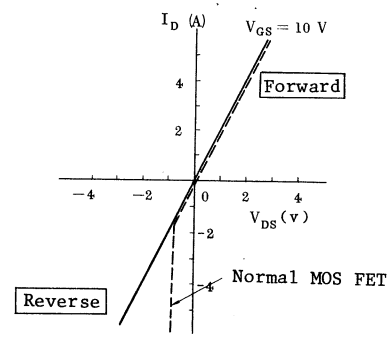
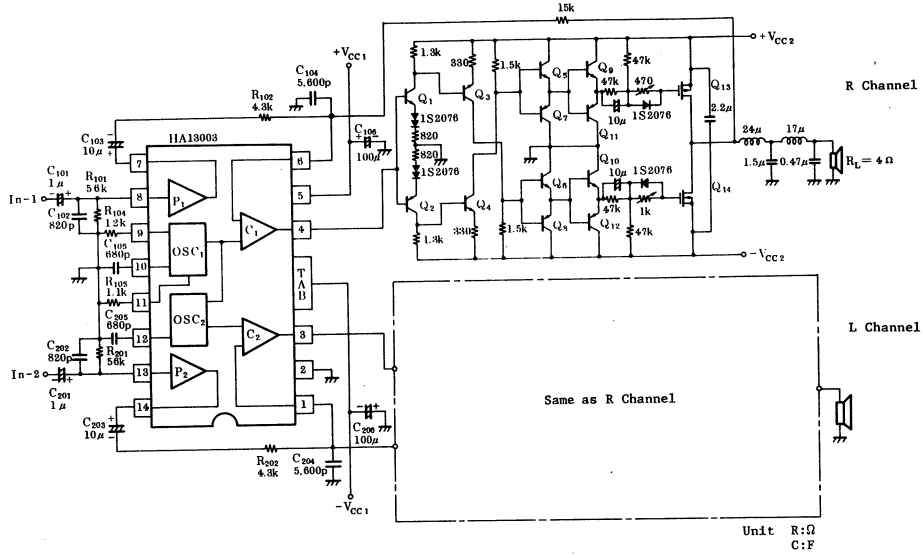


Fig. 4-15 I_D-V_{DS} Characteristics

(4) Application and Line-up



$\pm V_{CC1}=\pm 10V$
$\pm V_{CC2}=\pm 25V$
$fosc \fallingdotseq 300kHz \left(\frac{1}{4 \cdot C_{105} \cdot R_{105}}\right)$
$R_L=4\Omega$

Q_1, Q_4, Q_5, Q_6 : 2SC2308
Q_2, Q_3, Q_7, Q_8 : 2SA1030
Q_9, Q_{10} : 2SD667
Q_{11}, Q_{12} : 2SB647
Q_{13} : 2SK346, 2SK428
Q_{14} : 2SJ102, 2SJ122

Note
1) As the interference of linking between the switching power MOS FET toward the modulator IC affects the Total Harmonic Distortion and output noise, the electromagnetic shielding over the power MOS FET, its driver circuit and demodulation filter are required.

Fig. 4-16 Po=40~60W PWM Power Amp for Car Stereo

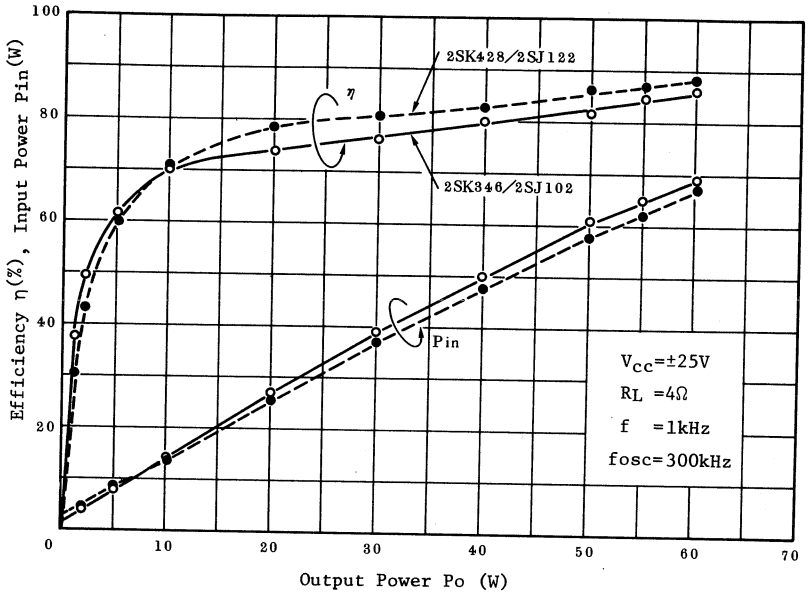


Fig. 4-17 η,Pin - Po Characteristics

Table 4-2 Line-up of Devices for PWM Power Amp

Audio Output Po (W)		Type Number		Package	Absolute Max. Ratings			Electrical Characteristics (typ)		
Single Pushpull	Parallel Pushpull	N-ch	P-ch		VDSS [V]	ID [A]	PD* [W]	RDS(on) [Ω]	ton [ns]	toff [ns]
30~40	—	2SK346	2SJ102	TO-220	60	5	30	0.3	40/60	70/100
40~60	—	2SK428	2SJ122		60	10	50	0.1/0.15	60/80	120/200
60~80	—	(2SK551)	(2SJ127)	TO-220	100	10	75	0.15/0.20	50/70	110/160
		2SK399	2SJ113	TO-3P			100	0.2/0.25		
80~100	—	2SK413	2SJ118		140	8	100	0.4	50/70	110/160
		2SK414	2SJ119		160					

Note

( ) ; Under Development

* ; Tc=25°C

2. High Speed Power Switching

2.1 Switching Regulator

● Two-transistor Push-pull system 250kHz, 150W (5V, 30A) switching Regulator

Fig. 4-18 shows the block diagram of a two-transistor push-pull system switching regulator in which the 2SK298 is used.

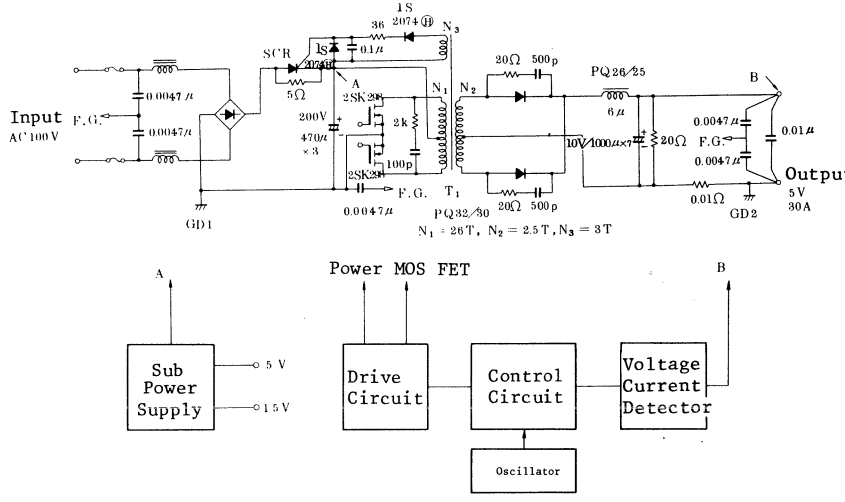
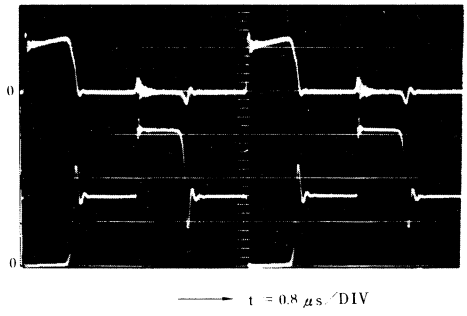


Fig. 4-18 Block Diagram



I_D (2A/DIV)

V_{DS} (50V/DIV)

Fig. 4-19 Waveform for Circuit of Figure 6-16 (Vout=5V, I_D=15A)

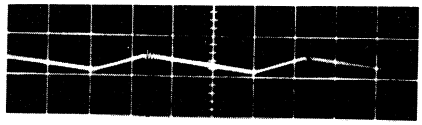


Fig. 4-20 Ripple Waveform of Output Voltage
(V_{out}=5V, I_D=15A)

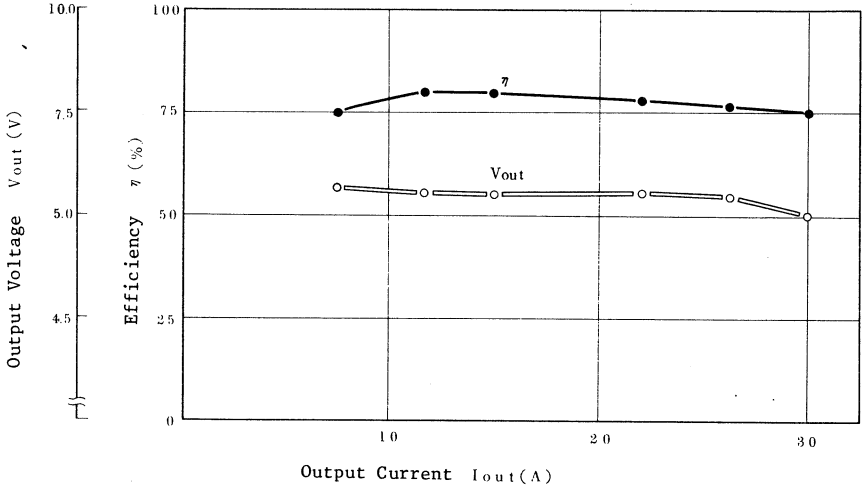


Fig. 4-21 Output and Efficiency vs. Output Current Characteristics

< Circuit Description >

(1) In rush current protection circuit

This circuit is to limit the charging current flowing to the input capacitor when the power supply turns ON. When the sub-power supply circuit turns ON and the main switching transistor (power MOS FET) begins to operate, a voltage is generated at the coil (N_3). By charging capacitor C by the time constant of R and C, the SCR gate is driven. This delay time prevents over current.

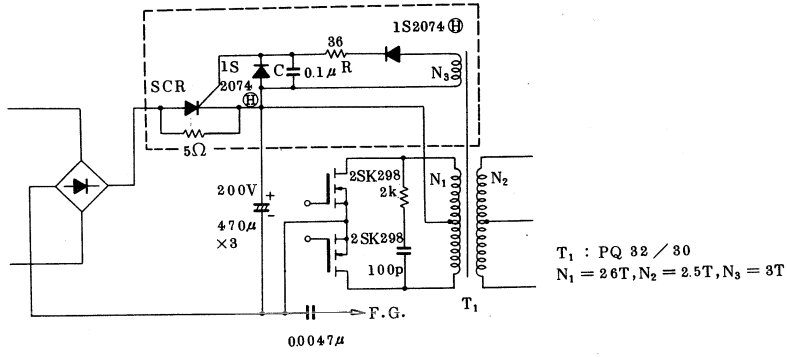


Fig. 4-22 Rush Current Protection Circuit (in dotted line)

(2) Sub Power Supply Circuit

The sub power supply circuit is a blocking oscillator whose secondary output is stabilized by three-terminal regulators; 5V output for IC driving, and 15V output for power MOS FET driving.

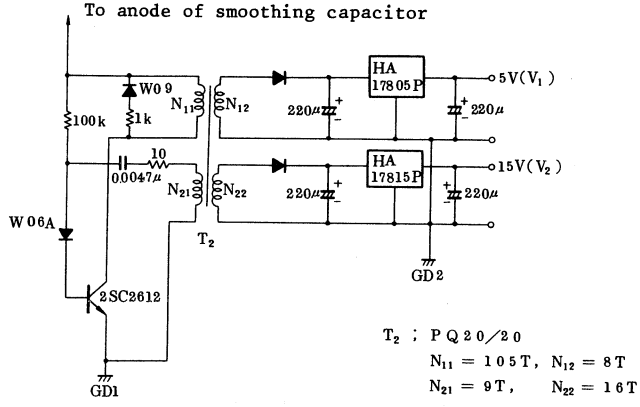


Fig. 4-23 Sub Power Supply Circuit

(3) Control Circuit

Since the switching frequency is very high (250kHz), the control circuit is made by IC's as shown in Fig. 4-23.

The functions of the IC's are as follows.

- IC_1: reference oscillation (500kHz)
- IC_2: pulse width control
- IC_3: 2-phase division
- IC_4: drive output . shut down
- IC_5: voltage detection, detection of over current, detection of over voltage

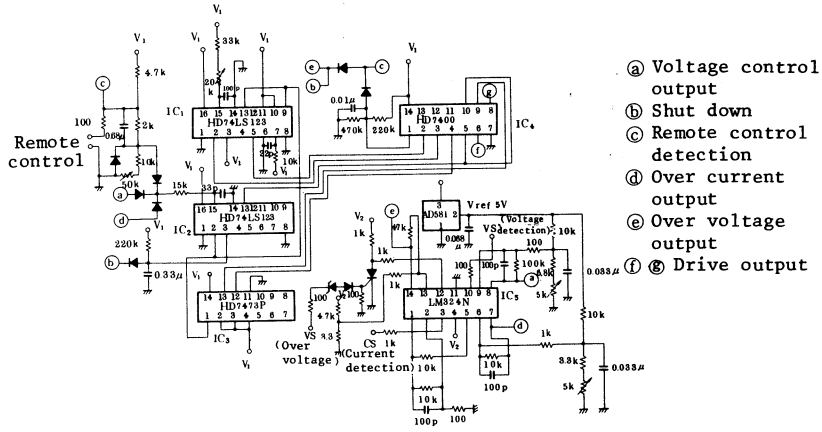


Fig. 4-24 Control Circuit

(4) Drive circuit

The drive circuit is coupled by a pulse transformer for isolation. When T_{r1} is in the ON state, the input capacitance of the power MOS FET is charged through the 330Ω resistance. When T_{r1} turns OFF, T_{r2} is turned ON by the flyback voltage and the input capacitance is discharged by the 51Ω resistance.

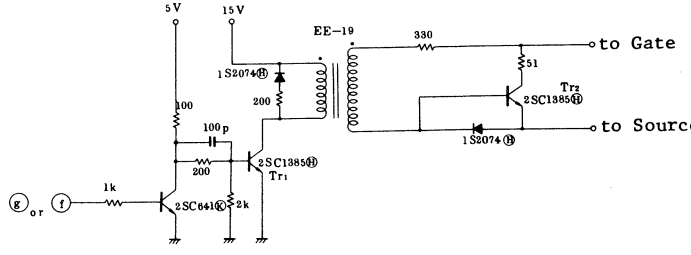


Fig. 4-25 Drive Circuit

< Noise >

(1) Countermeasure to noise

In this circuit noise is produced by the high switching speed of the power MOS FETs.

Normal mode noise will be reduced by adding capacitors to both sides of the output, as shown in Fig. 4-26.

Common mode noise will be reduced by returning the noise to the generation point, as shown in Fig. 4-26 (a). As shown in Fig. 4-26 (b), if a choke coil is inserted for common mode suppression, the noise will be further reduced.

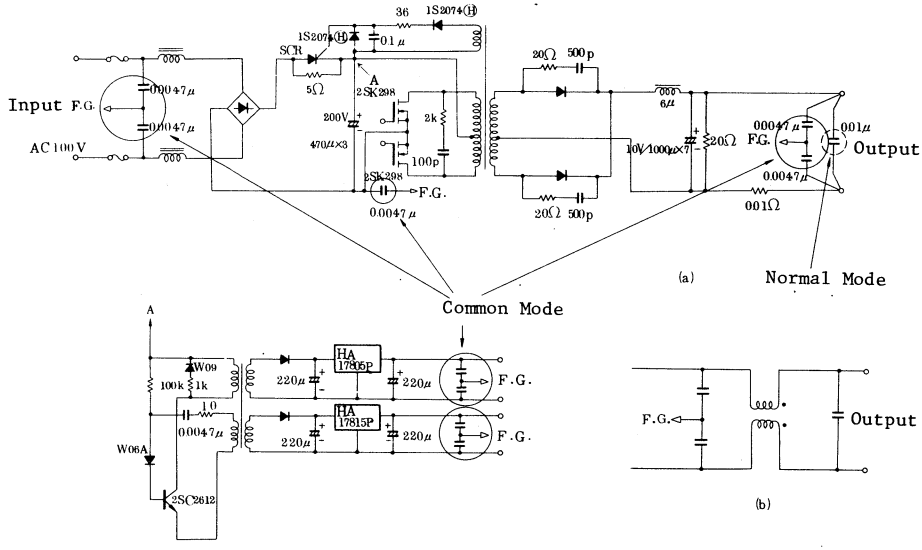


Fig. 4-26 Countermeasure to Noise

(2) Drive Circuit and Noise

As described in the preceding section (1), noise is generated because of the high speed operation of the power MOS FETs. Especially, the ON time has large influence on noise generation. This means that noise can be reduced by improving the drive circuit.

Table 4-3 Drive Circuit and Noise

Item \ Gate Circuit	① R_1 ($R_1 \leqq rg$)	② C_{gd}, R_1	③ R_1 ($R_1 > rg$)	④ D_1, R_1	⑤ D_1, C_1, R_1, R_2
Parameter	$R_1 = 51\Omega$	$C_{gd} = 50$ pF $R_1 = 51\Omega$	$R_1 = 551\Omega$	$R_1 = 551\Omega$	$C_1 = 300$ pF $R_1 = 551\Omega$ $R_2 = 300\Omega$
Turn-On Time (ns)	30	130	90	90	120
Turn-Off Time (ns)	280	1550	670	280	280
Output Noise (mV) p-p	570	140	135	110	100
Switching Loss (W)	2.7	30.5	6.6	3.0	4.14
Remarks	Switching Loss;Small Switching Time;Small Noise ;Large	Switching Loss;Maximum Switching Time;Large Noise ;Small	Switching Loss;Large Turn Off Time ;Large Noise ;Small	Switching Loss;Small Turn Off Time ;Small Noise ;Small Selection of a constant ;Difficult	Switching Loss;Small Turn Off Time ;Small Noise ;Small

Test Conditions : Input AC 100V, Output 5V · 10A,
Switching Frequency 100 kHz

- ONE TRANSISTOR FORWARD SYSTEM, 500kHz, 50W (5V, 10A) SWITCHING POWER SUPPLY

Fig. 4-27 and Fig. 4-28 respectively show the switching power supply circuit block diagram and its waveforms.

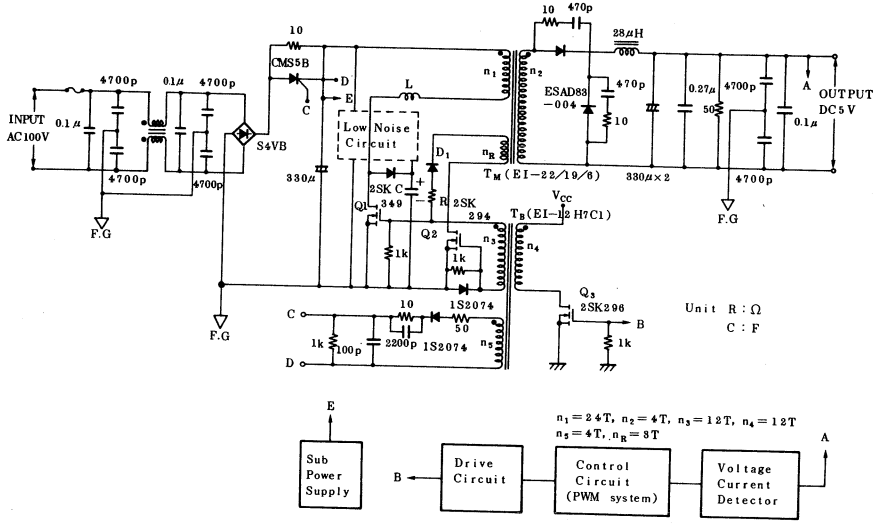


Fig. 4-27 Block Diagram of One-Transistor Forward System, 500 kHz, 50W (5V, 10A).

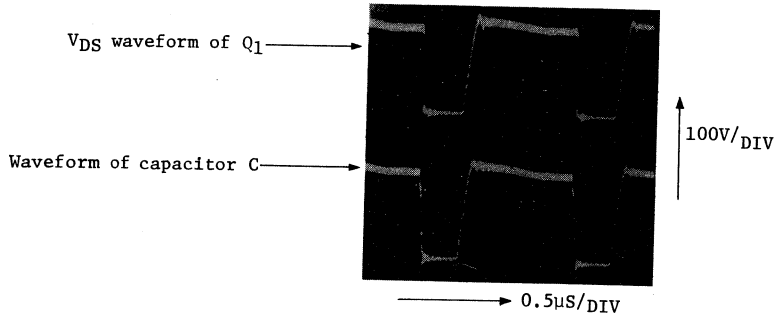


Fig. 4-28 Waveforms (at 5V, 9.1A)

[High speed drive circuit]

To allow a higher frequency switching power, the most important thing is to turn off the main switching device in high speed. A control current with a high peak value is necessary to turn a power MOS FET off. Here, we adopt a simple circuit by utilizing the main circuit to supply a high peak current at turn-off. This circuit operates as follows.

When the MOS FET Q_3 turns on, a current flows via transformer T_B to Q_1 gate, and Q_1 is turned on. In consequence, a voltage is induced in the coils n_1 and n_R. The black dot in the figure indicates the positive polarity. Q_2 is off with inverse bias by voltage drop in the diode D_2.

Next, when Q_3 is turned off, the current in T_B flows through the gate to source of Q_1 and the source to gate of Q_2 and turns Q_2 on. Q_1 is still on, right after Q_2 turns on.

Therefore, the above mentioned voltage in the coils n_1 and n_R still remains. By Q_2 turning on, current from n_R flows to the source - gate of Q_2 and Q_1, the resistor R, and the diode D_1 and turns Q_1 off. When Q_1 turns off, a reverse voltage to the dotted polarity is generated in n_1 and n_R. This voltage is blocked by D_1.

With the above operation, an inverted high peak gate current can be generated from the main circuit to Q_1.

[Noise reduction]

The output noise is reduced by L and C in the circuit. This controls the voltage change rate by time of which voltage is supplied to the primary coil at on or off of the main switching device. The reactor L restrains the current increase in the primary coil n_1, when Q_1 (main switching device) turns on. The capacitor C restrains the change rate of the voltage induced in the primary coil n_1, when Q_1 turns off.

The part encircled by a dotted line in the figure is discharge circuit for the capacitor C which is charged with the polarity indicated in the figure after Q_1 was turned off.

This discharge circuit feeds the charged energy in C back to the rectified DC supply in the primary part, while Q_1 is on. The circuit also discharges C to 0V until Q_1 is turned off. The constants of L and C are determined by analyzing the harmonics in the voltage supplied to the

primary coil n_1, so that the resonant frequency of the equivalent high-pass filter between primary and secondary coils is removed.

The output noise waveform from the above described circuit, and without countermeasures, are shown in Fig. 4-29 and Fig. 4-30 respectively. You can see in the figures that the output noise is significantly reduced.

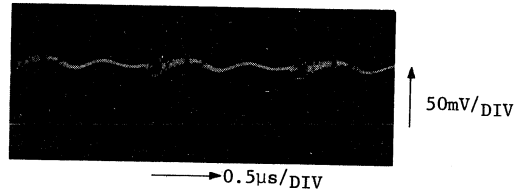


Fig. 4-29 Output Noise Waveform with the Circuit Introduced (Synchroscope 150 MHz, 5V, 10A)

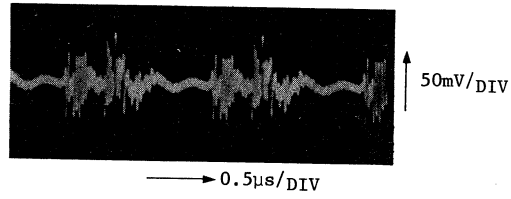


Fig. 4-30 Output Noise Waveform without Countermeasures (Synchroscope 150 MHz, 5V, 10A)

A comparison of the volume with main transformer, choke coil and output smoothing capacitor in 50 kHz, 50W (5V, 10A) output switching power supply made on an experimental basis in our company is shown in Table 4-4. In 500 kHz switching power supply, 26% of the main transformer volume, 25% of the choke coil volume and 50% of the output smoothing capacitor volume; i.e. 65% of the total volume were reduced, in comparison with 50 kHz switching power supply.

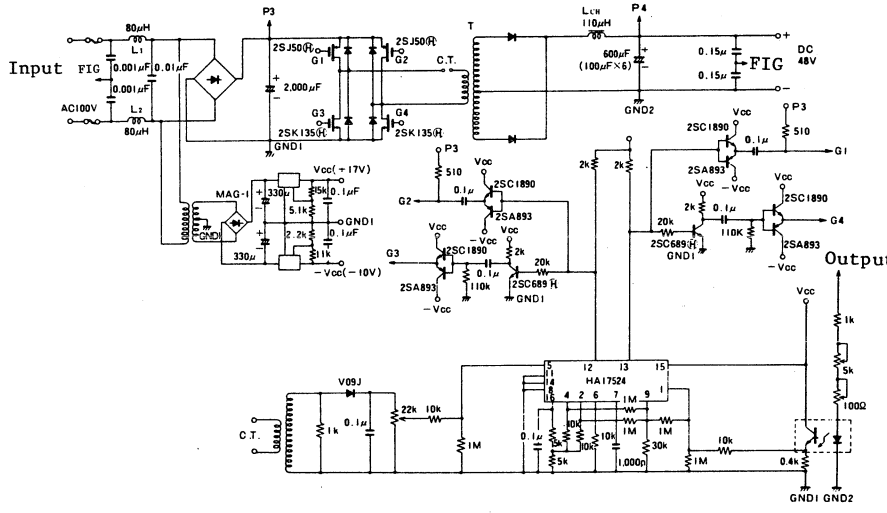
Fig. 4-4 A Comparison of the Volume of Main Transformer, Choke Coil and Output Smoothing Capacitor in 5V, 10A Output Switching Power Supplys

	50kHz switching power supply	500kHz switching power supply
Main transformer volume	16000mm^3	4200mm^3 (26%)
Choke coil volume	8500mm^3	2100mm^3 (24%)
Output smoothing capacitor volume	16000mm^3	8000mm^3 (50%)

● Four-transistor full-bridge type 100kHz, 400W switching regulator

Fig. 4-31 shows the circuit of four-transistor full-bridge type switching regulator. This circuit has the following characteristics.

- output; 400W (48V, 8A)
- input; AC 100V
- operation frequency; 100kHz
- control IC; HA17524
- isolation; photo coupler
- efficienty; at full load 80%
  ; at 200W output 85%



L1,L2:T type core φ1.5mm wire 13T
LCH:EI50 core Cap 0.3mm
φ1mm wire 6 wires wound separately

T:EI60 core
1st side φ1.5mm Wire 7T
2nd side φ1mm wire 4T;
5 wires wound separately

C.T.:EI30 core
1st side φ1.5mm wire 1T
2nd side φ0.5mm wire 25T

Fig. 4-31 Four-transistor Full Bridge System Switching Regulator

This circuit operates as a switching regulator (AC 100V, direct rectification type), using N-channel & P-channel MOS FET's for four-transistor full bridge. To make good use of the high speed capability of power MOS FETs, the switching cycle is set at 100kHz. As a result, we had 80% efficiency at full load and maximum 85% efficienty (at 200W output).

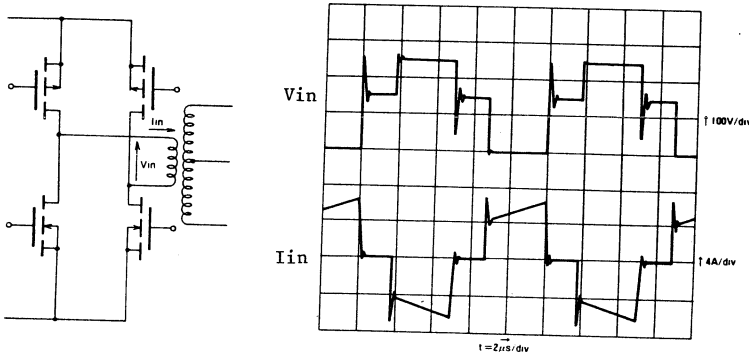


Fig. 4-32 Waveform (Full loaded)

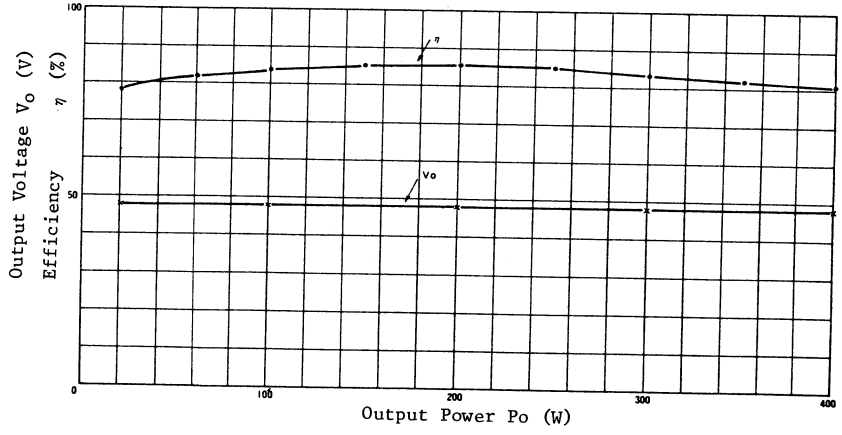


Fig. 4-33 Output Voltage and Efficiency vs. Output Power Characteristics

● One-transistor system 250kHz, 60W, low noise switching regulator

Fig. 4-34 shows the circuit of one-transistor system switching regulator. It has the following characteristics.

- output; 5V, 12A
- input; 48±5V
- operation frequency; 250kHz
- efficiency; at full load 83%
  ; at 20W output 87%
- spike noise voltage; 10mV$_{p-p}$

The noise reduction method used in this circuit is as follows:

(1) Good use is made of the source connected case of the power MOS FET.

(2) Loose coupling of the output transformer.

(3) Switching curve softened by mirror integration with the primary circuit of transformer, connecting the capacitor between drain and source.

With the above method, the spike components will be removed almost completely. Radiation to the outside can be prevented by shielding.

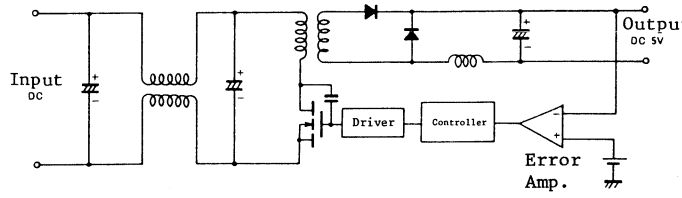


Fig. 4-34 One-transistor type Switching Regulator (Block Diagram)

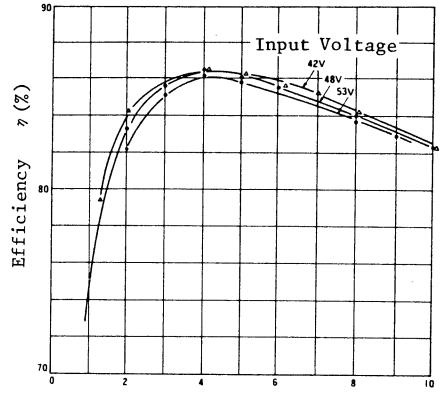


Fig. 4-35 Efficiency vs. Output Current Characteristics

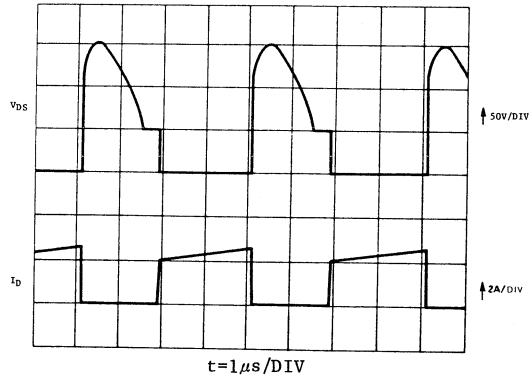


Fig. 4-36 Waveform

2.2 High-speed Drive Circuit

A switching regulator has two types of drive circuits; one is direct type drive and the other is isolated type drive.

● Direct type

(1) Additional Buffer Circuit

Fig. 4-37 shows additional buffer Circuit. In this circuit, the output impedance of the drive circuit is lowered through NPN and PNP complementary symmetry emitter follower, resulting in high speed.

(2) Positive Feedback type Circuit

Fig. 4-38 shows positive feedback type circuit, in which positive feedback is applied by sub-coil (n_3), resulting in high speed switching. The operation theory is as follows.

i) FET_1 is driven by inverter and drain current flows.

ii) Voltage is generated by n_3 and the input capacitance (Ciss) is charged through R_1.

iii) According to turn ON process of FET_1, a positive feedback is applied to the gate.

iv) When the FET_2 turns ON and the gate of FET_1 is grounded, resulting in discharge of Ciss, the FET_1 turns OFF.
Fig. 4-39 shows the waveform between drain and source.

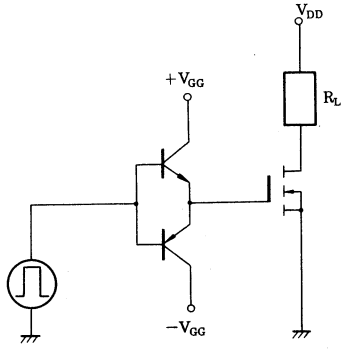


Fig. 4-37 Additional Buffer Circuit

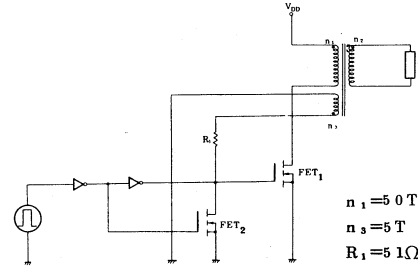


Fig. 4-38 Positive Feedback Circuit

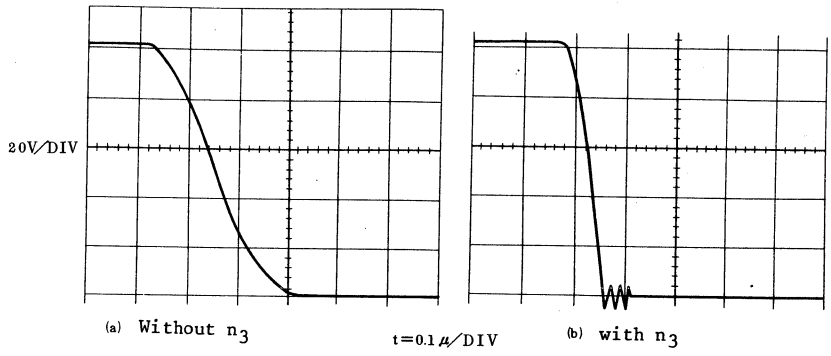


Fig. 4-39 Drain-Source Waveform(I_D=2 A) (2SK298)
n_1=50 T , n_3=5T , R_1=51Ω

● Isolation Type

The following circuits operate by making use of the flyback voltage which is generated during the OFF period.

(1) Diode Switch Type

This circuit is the simplest. In this circuit, the input capacitance of FET_1 is forced to be discharged by the flyback voltage which is generated when FET_2 turns OFF, and high speed switching is achieved. This circuit has a problem in that the turn off time of FET_1 is not constant because the flyback energy depends on the ON time (pulse width).

Fig. 4-40 and Fig. 4-41 show the circuit and the waveform respectively.

(2) FET Switch Type (1)

The circuit in Fig. 4-42 is an improved one of the circuit in Fig. 4-40. In this circuit, the charge stored in Ciss is discharged when FET_2 is turned ON by the flyback voltage, and the gate of FET_1 is grounded. In this case, the turn off time is constant in spite of the pulse width fluctuations, because the effect of FET_2 is larger than that of the flyback.

Fig. 4-43 shows the waveform between drain and source.

(3) FET Switch Type (2)

The circuit shown in Fig. 4-44 yields even higher performance than that of Fig. 4-42. In this circuit, when FET_2 is turned ON by the flyback voltage, the voltage generated at n_5 will discharge the FET's Ciss positively with the time constant R·Ciss. As obvious from the operation waveform of Fig. 4-45, the turn on time and the turn off time are both less than 30ns.

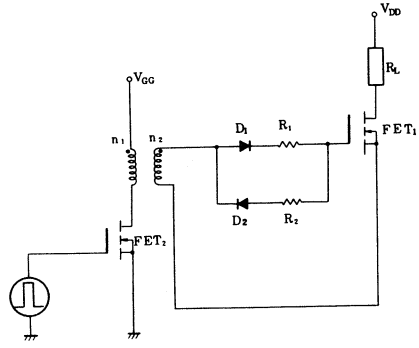


Fig. 4-40 Diode Switch Type

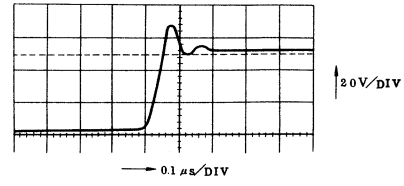


Fig. 4-41 Drain-Source Waveform ($I_D = 2A$, 2SK 298)
$n_1 : n_2 = 1 : 1$
$R_1 = R_2 = 50\Omega$

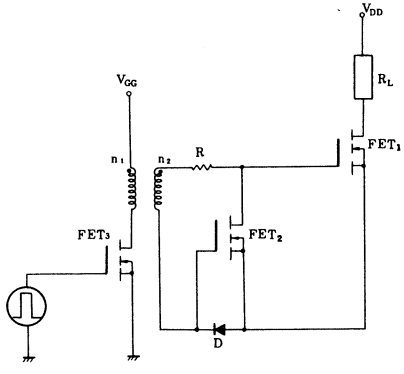


Fig. 4-42 FET Switch Type

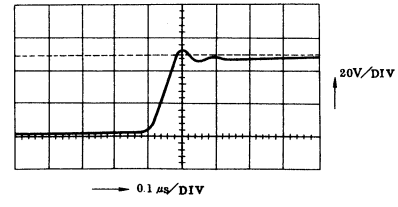


Fig. 4-43 Drain-Source Waveform
($I_D = 2A$, 2SK 298)
$n_1 : n_2 = 1:1$ $R = 50\Omega$

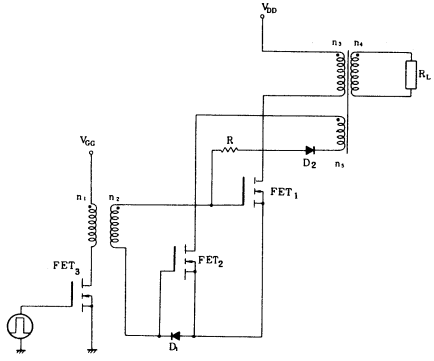


Fig. 4-44 FET Switch Type

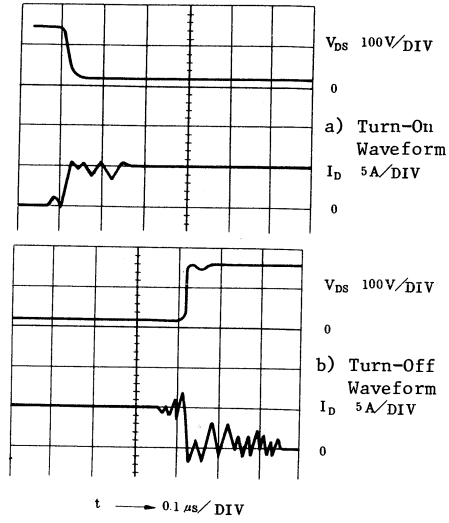


Fig. 4-45 Waveform (2SK298)
$n_1 : n_2 = 1 : 1$, $n_3 = n_4 = 60T$, $n_5 = 6T$
$R = 10\Omega$, D_1, D_2 : 1S2074Ⓗ

3. High Frequency Power Amplifier

As for transmitter applications, transistorization of 5 ∿ 10kW medium wave broadcasting transmitters has been achieved. The bipolar transistors used however, have some problems regarding thermal runaway, frequency characteristic, modulation linearity, etc. Transistorization in short wave broadcasting has not yet been realized, because there is not a suitable device.

We would like to show a fully-transistorized medium wave broadcasting transmitter and a fully-transistorized short wave broadcasting transmitter, in which a high output is provided by parallel operation of power MOS FETs.

3.1 1kW Medium Wave Broadcasting Transmitter *1)

Fig. 4-46 shows a block diagram of a 1kW medium wave broadcasting transmitter. This system has the following characteristics.

- Frequency; 1197kHz
- Output; 1100W
- Power supply; AC 200V, Single phase 50Hz
- Efficiency (without modulation)
  - Total efficiency; 61.9%
  - Efficiency at modulation part; 93.6%
  - Efficiency at non-modulation part; 84.4%
- Modulation System; pulse width modulation

Power MOS FETs used in the transmitter provide the following features.

(1) Low Power Consumption

Power MOS FET requires no pre-modulation because of its high efficiency and high gain.

(2) High Performance

The distortion introduced by the pulse width modulation stage is very small because of its switching speed. A high carrier frequency can be used in the PWM modulator for extended overall frequency response.

(3) High Reliability

The power MOS FET is inherently rugged and may be connected in parallel without any special considerations. It is possible to use many devices in parallel, and through their redundancy, high reliability is realized.

(4) Easy Thermal Design

The use on many parallel devices aids thermal dispersion, and results in easy thermal design.

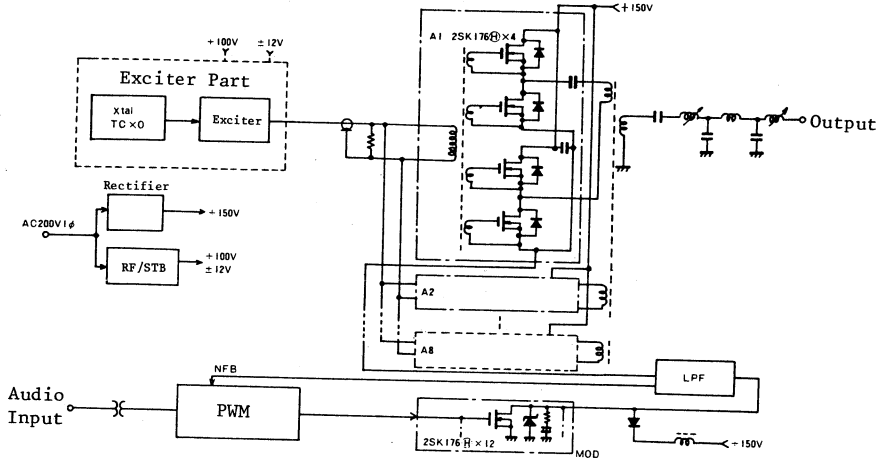


Fig. 4-46 Block Diagram of 1kW Medium Wave Broadcasting Transmitter

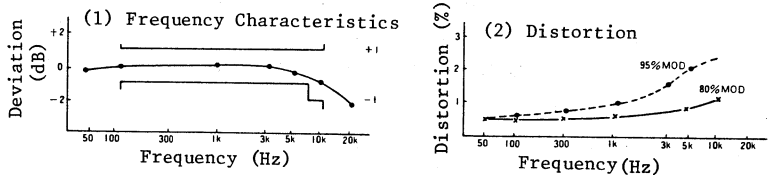


Fig. 4-47 Main Characteristics

3.2 600W Short Wave Broadcasting Transmitter *2)

Fig. 4-48 shows the circuit of the power amplifier circuit. The characteristics of this circuit are as follows:

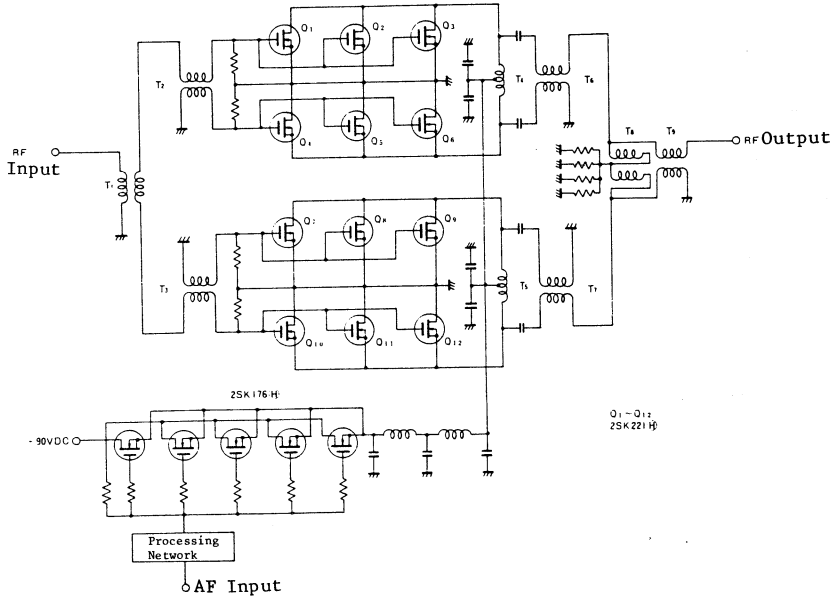
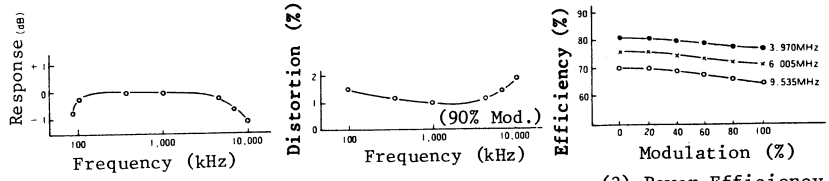


Fig. 4-48 Power Amplifier (200W Unit)



(1) Frequency Characteristics (2) Distortion Characteristics (3) Power Efficiency

Fig. 4-49 Main Characteristics

- Frequency; 3.970MHz, 6.005MHz, 9.53MHz
- Output; 600W (four 200W units using 2SK221Ⓗs)
- Efficiency (without modulation); 81% at 3.970MHz
  77% at 6.005MHz
  70% at 9.535MHz
- Modulation System; PWM Modulation System (using a 2SK176Ⓗ)

This is the circuit of a short wave broadcasting transmitter with 600W output, in which the 2SK221Ⓗ is used. By using four 200W output units, the redundancy is increased and high reliability is achieved. Also, a PWM modulation system is used, resulting in smaller size, lighter weight and higher efficiency. Modulation is performed at 100kHz repetitive frequency, using the 2SK176Ⓗ.

3.3 VHF High Power Amplifier Circuit.

Power MOS FET is applicable to higher voltage circuits, and necessary output power can be obtained with a small current. Fig. 4-50 shows the VHF high power amplifier circuit using 2SK317. The input capacitance is about 600pF, so the input impedance at 100MHz is small, (Z_{in}=1-1jΩ) and the output impedance is small too (it's about 1.5-25jΩ at 100MHz). Owing to the above factors, the rotation to inductive area of the in-output circuit occurs by using series inductance, then, these circuits are matched with 50Ω by series and parallel capacitance. 180W output power, 80% drain efficiency can be obtained with 80V supply voltage, 8W input power, 100MHz frequency. 120W output power, 60% drain efficiency can also be obtained at the frequency of 175MHz. The current is as small as 2.8A, 2.5A respectively. In the case of push-pull circuit which adopts a couple of 2SK317s, 270W output power, 80% drain efficiency can be obtained with 90V supply voltage, 20W input power. As for input circuits, 50Ω co-axial cable balun is determined as 38.2cm so that the input signals can be applied with different phases. The output circuit consists of balun and filter, and the length of the output balun is determined as 11cm, aiming at maximum efficiency.

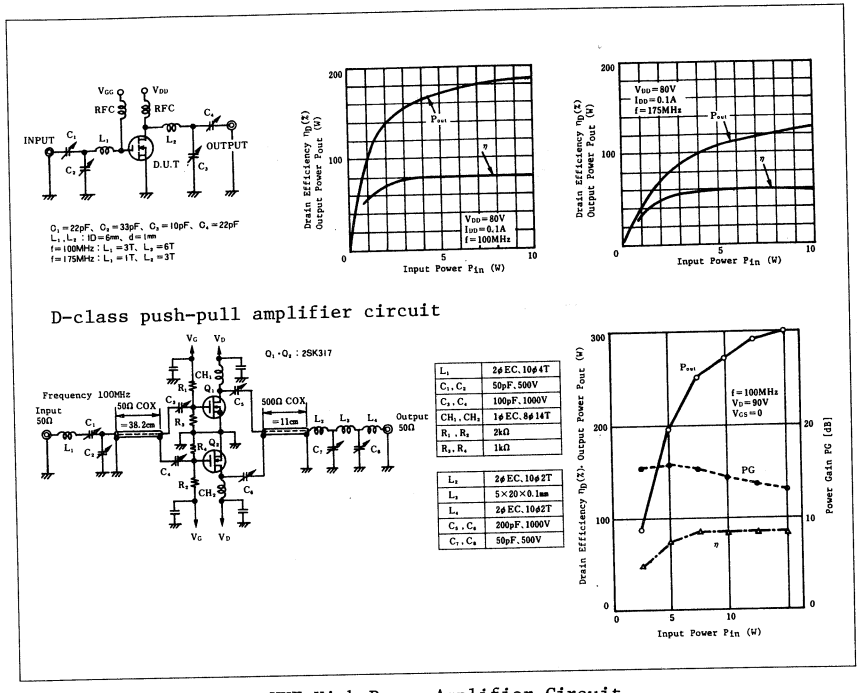


Fig. 4-50 VHF High Power Amplifier Circuit

(1) 900MHz 1W power amplifier circuit (PF0001)

The PF0001 is a high frequency power MOS FET amplifier and the output power; 1W (typ.) can be obtained. It is single stage amplifier using the HS8709 chip. Fig. 4-51 shows the internal equivalent circuit and dimensional outline of the PF0001. The matching circuit is formed on the ceramic substrate by using micro-strip line and chip condenser. 1.1W output power, 50% total efficiency, power gain 10dB (typ.) can be obtained at 100mW input power. As for gain reduction value controlled variable by the APC terminal, 5dB or more can be obtained by changing the APC voltage from 8V to 0V.

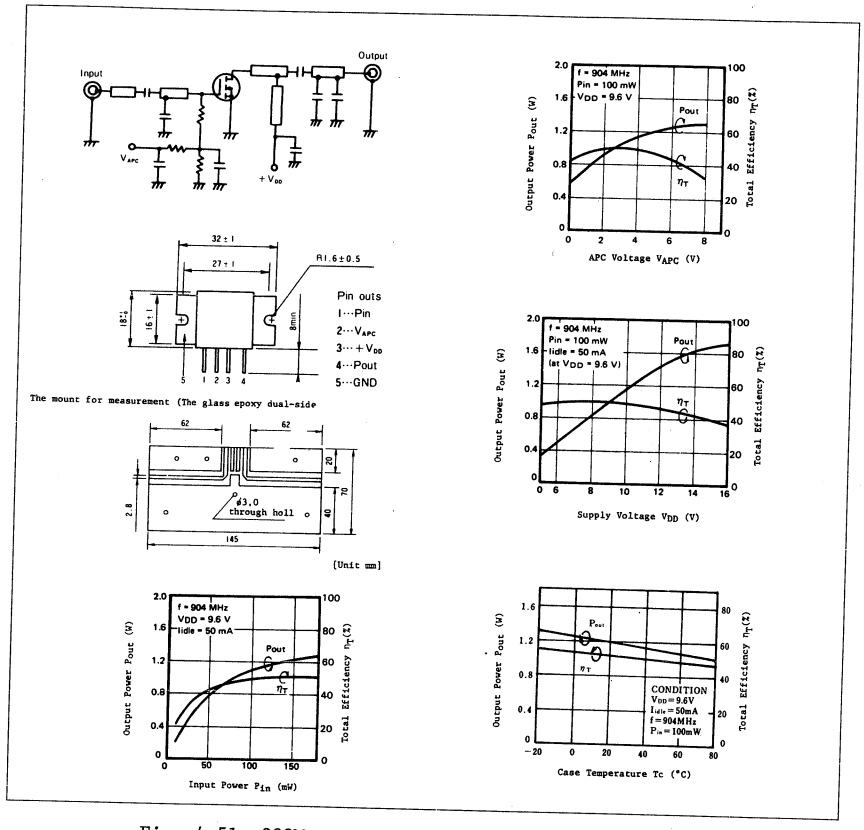


Fig. 4-51 900MHz 1W Power Amplifier Circuit (PF0001)

(2) 900MHz 8W power amplifier circuit (PF0002)

The PF0002 is a high frequency power MOS FET amplifier. It is a two stage amplifier using HS8709 and HS8711 chips. Fig. 4-52 shows the internal equivalent circuit and dimensional outline. The applicable range of supply voltage is 7 to 16V, the frequency range is 860 to 910MHz. As for gain reduction value controlled variable by the APC terminal, 5dB or more can be obtained by changing the APC voltage 8V to 0V.

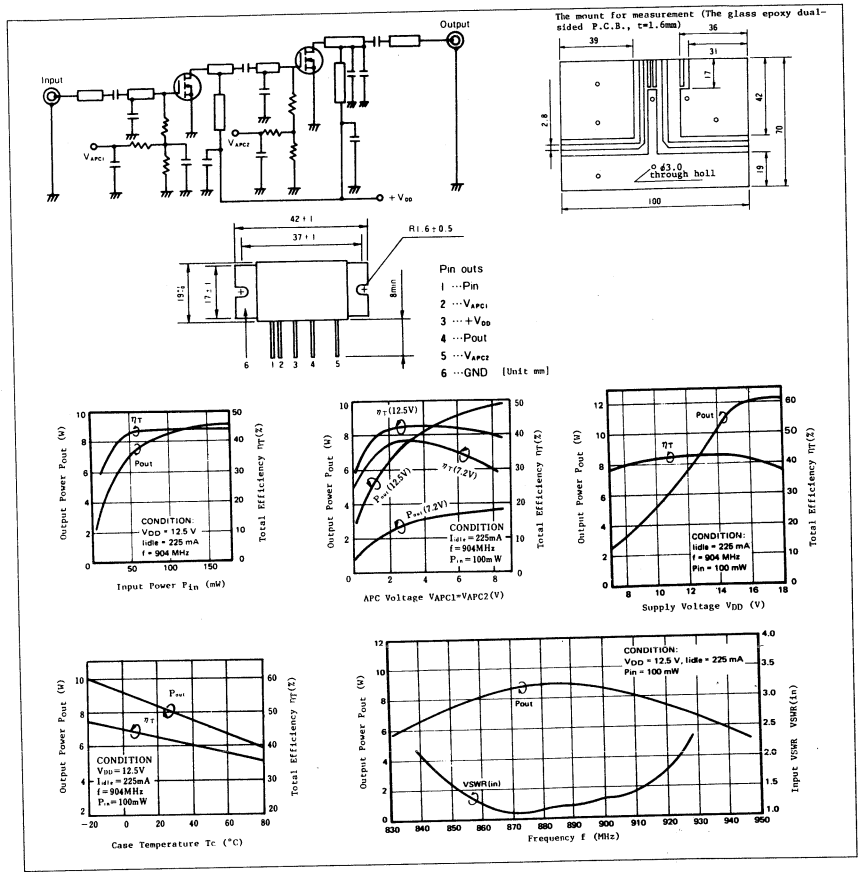


Fig. 4-52 900MHz 8W Power Amplifier Circuit (PF0002)

(3) 900MHz power amplifier circuit (HS8708)

The HS8708 is power MOS FET and its applicable input power is 10 to 50mW. It is sealed into the chip carrier. Fig. 4-53 shows the 900MHz pre-drive circuit using this FET. 400mW output power, 40% efficiency can be obtained at 20mW input power, when V_{DD}=12.5V. The output power can be controlled from 300mW up to almost 0mW by changing the gate voltage from 2.0V to 0.

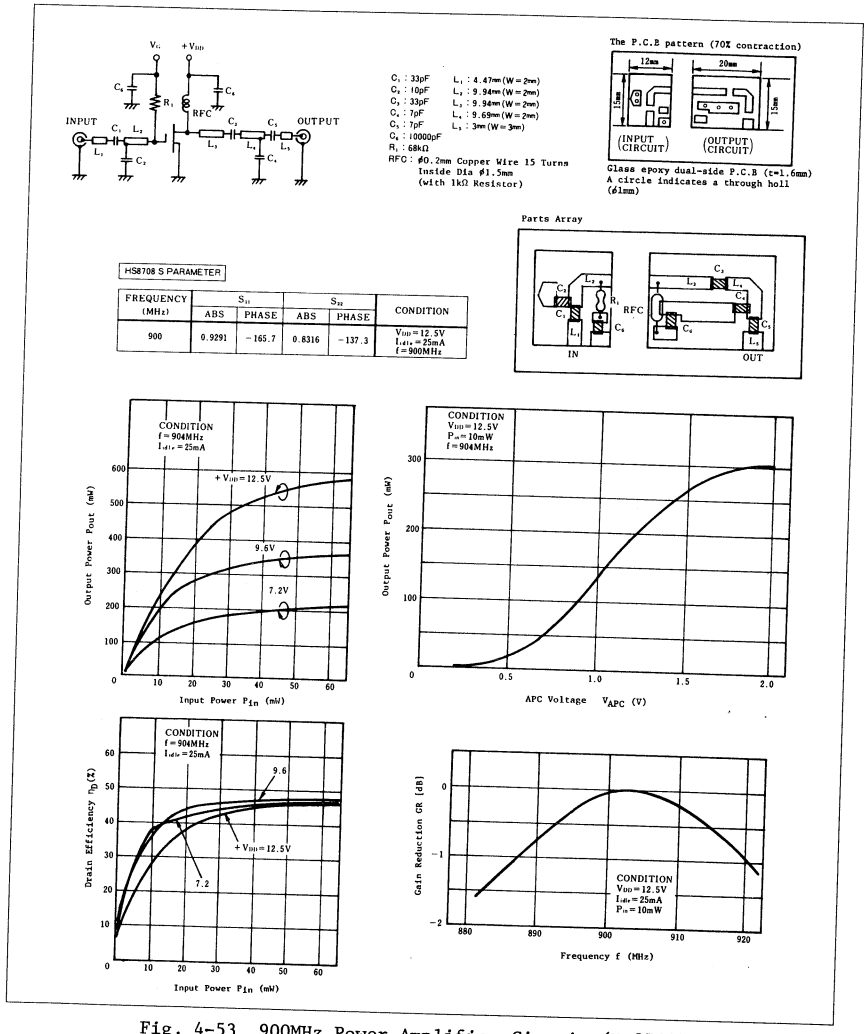


Fig. 4-53 900MHz Power Amplifier Circuit (HS8708)

(4) 900MHz power amplifier circuit (HS8709)

The HS8709 is power MOS FET of 100mW input power. The chip used for the PF0001 and the drive stage of PF0002, is sealed into the chip carrier. Fig. 4-54 shows the drive circuit by using this FET. The output power 1.5W, 50% efficiency can be obtained when V_{DD}=12.5V, 100mW input power.

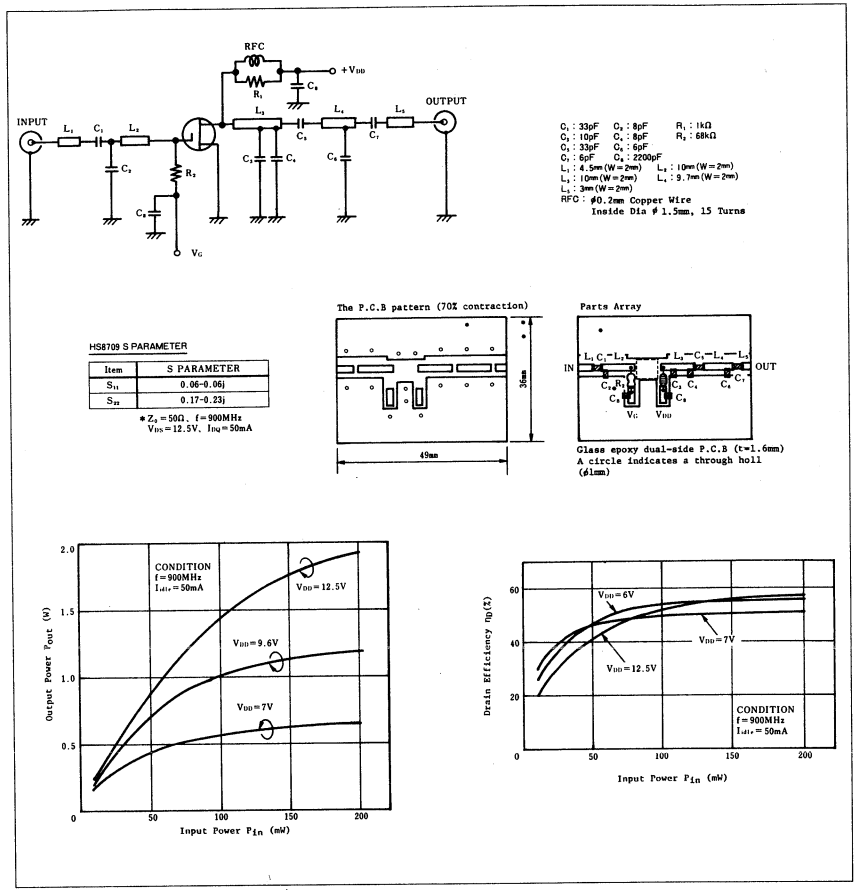


Fig. 4-54 900MHz Power Amplifier Circuit (HS8709)

(5) 900MHz two stage power amplifier circuit

Fig. 4-55 shows a two stage power amplifier circuit using HS8708, HS8709. 2.5W output power, 50% total efficiency can be obtained when V_{DD}=12.5V, 20mW input power. The power control by using 1st and 2nd gate voltages in the case of 10mW input power, the output power can be controlled from 2.5W to almost 0, by changing the gate voltage from 2V to 0. The gain reduction value is about 7dB with 30mW input power.

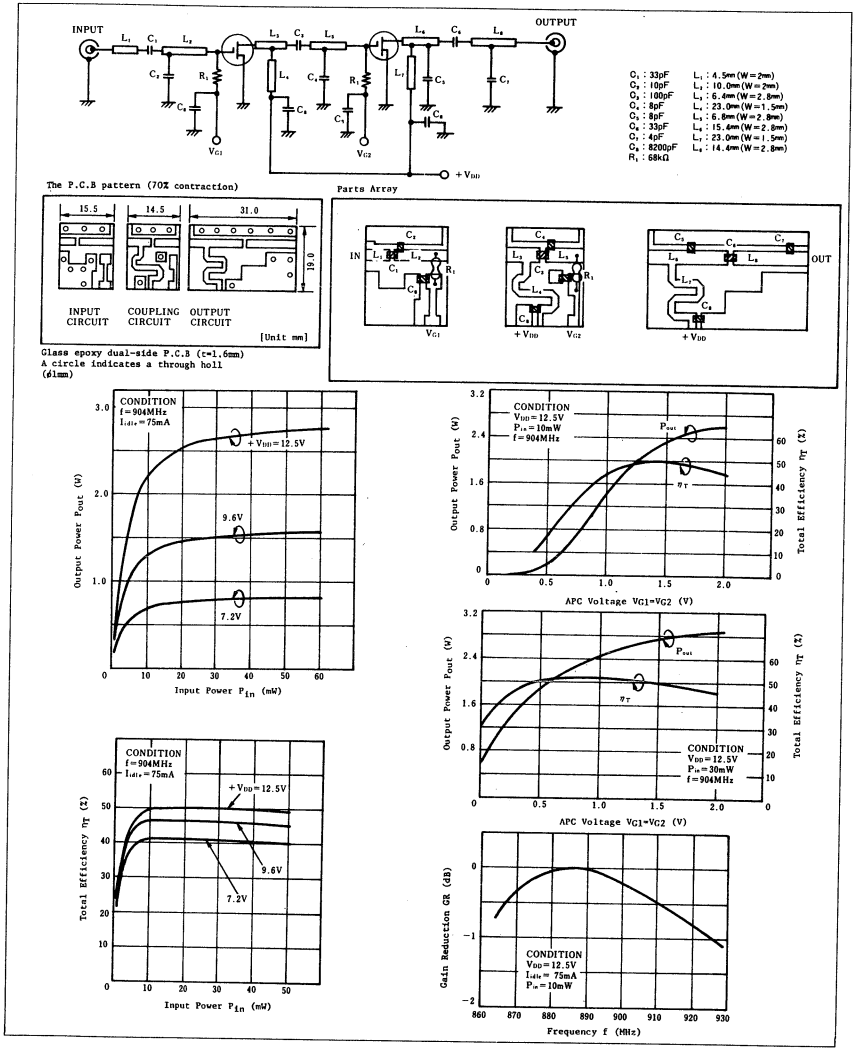


Fig. 4-55 900MHz Two Stage Power Amplifier Circuit

(6) 900MHz power amplifier circuit (HS8711)

The HS8711 is power MOS FET used for final stage of PF0002. Fig. 4-56 shows the power amplifier circuit using this FET. 8W output power, 55% efficiency can be obtained when V_{DD}=12.5V, 1.6W input power. In the case of 7V supply voltage, 3.5W output power, 49% efficiency can also be obtained.

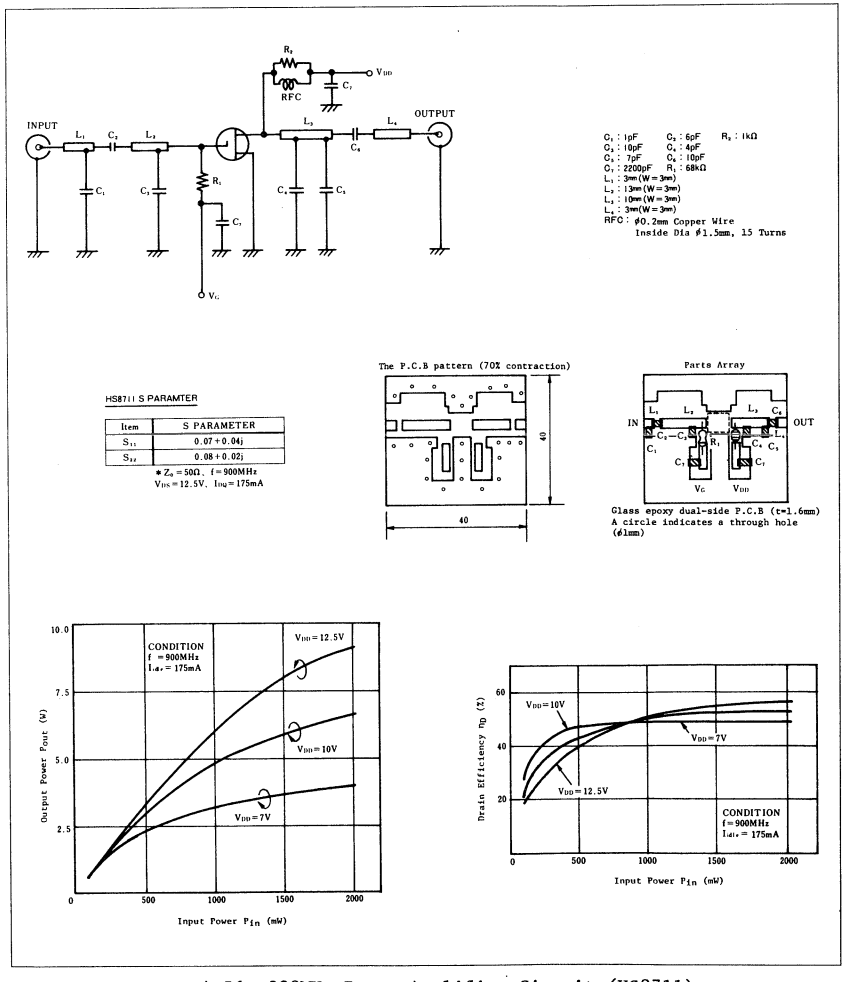


Fig. 4-56 900MHz Power Amplifier Circuit (HS8711)

4. Motor Control

Formerly, bipolar transistors or thyristors have been used for speed control of DC and AC motors. Recently, however, power MOS FETs are used for motor control, owing to their low R_{ON}. Power MOS FETs used for motor control have the following features.

(1) Since the switching speed of the power MOS FET is very fast, the chopping frequency of the motor control can be increased to 10kHz ∿ 20kHz. This is 10 times as high as conventionally used, resulting in quick response, high efficiency, reduced noise, and small size.

(2) As for the electrical characteristics, the power MOS FET has a negative temperature coefficient, so it has wide ASO (Area of Safety Operation).

(3) Since the power MOS FET is driven by voltage, it requires little driving current, resulting in a simple drive circuit.

(4) The power MOS FET has a parasitic diode between source and drain. This diode has comparatively high switching speed and the current rating is equal to that of the power MOS FET. It can be used as a fly-wheel diode. Therefore, the external commutation diode can be eliminated and the number of components can be reduced.

Table 4-4 The Characteristics of Power MOS FET and Advantages in Motor Control

Features	Advantages in motor control
Switching speed is fast.	High efficiency, reduced noise and small-sized by high operating frequency
Voltage control	Little driving power, resulting in a simple drive circuit
Negative temperature coefficient of current	Easy to have higher current capability with parallel connection due to no local current concentration
Built-in diode between drain and source	It can be used as a fly-wheel diode, and the number of components can be reduced
P/N channel complimentary	The number of components can be reduced by the simple drive circuit

Fig. 4-57 shows inverter circuit in which 2SK313 is used at $Q_1 \sim Q_6$. The built-in diode between drain and source is relatively high speed and can be used as a fly-wheel diode. Therefore, external high-speed fly-wheel diode is not required, the number of components can be reduced. As for electrically short accident in the inverter circuit, Power MOS FETs take longer time than bipolar transistor to breakdown, and over-current protection circuits can be easily designed. Fig. 4-58 shows the results of load short test.

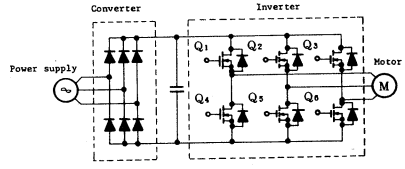


Fig. 4-57 Power MOS FET Inverter

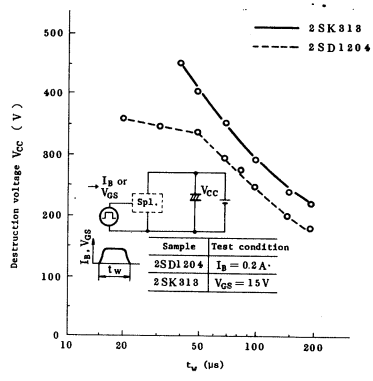


Fig. 4-58 Destruction voltage at load short test

● Gate Drive Circuit

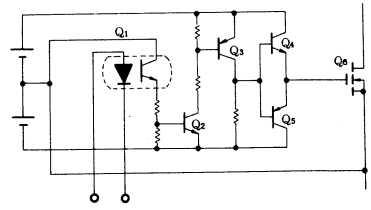
Fig. 4-59 shows basic gate drive circuit in which Power MOS FET is used. There are several kinds of circuit. The circuit needs less drive power due to voltage control than the current control of bipolar transistor, and can compose by small signal transistors.

The comparison of driving power with bipolar transistor is shown in Fig. 4-60.

This figure shows the characteristics of 1.2kW DC brushless motor drive using the inverter circuit in which power MOS FET, 2SK313 (V_{DSS} 450V, I_D 12A) or darlington transistor 2SD1204 (V_{CEO} 400V, I_C 15A) is used. As for driving power, the total of the transformer loss at driving circuit and the control circuit loss and the drive circuit loss is measured as sub power supply input. The drive power loss of Power MOS FET, 2SK313, is less than that of darlington transistor. Concerning with inverter efficiency, Power MOS FET shows almost same level as darlington transistor because of rather low driving frequency of 2.2kHz.

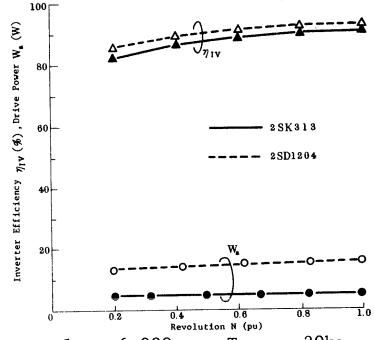
If Power MOS FET is used, power supply components for driving can be simplified due to low drive power loss (Fig. 4-61). Fig. 4-61 (a) shows the method that obtains positive and negative power supply from inverter input DC voltage using zener diode. Fig. (b) shows the method that obtains positive and negative power supply using power supply transformer. The method using power supply transformer does not need power stability due to voltage control gate drive.

The gate drive circuit can save energy and be minimize by using Power MOS FET.



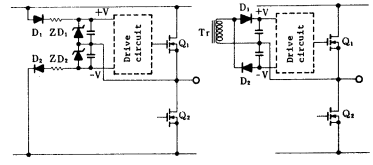
Q_1; Photo Coupler
Q_2~Q_5; Drive Transistor
Q_6; Power MOS FET

Fig. 4-59 Gate Drive Circuit of Power MOS FET



Note: 1 pu=6,000rpm Torque 20kg·cm

Fig. 4-60 Comparison of Drive Power of 1.2 kW DC Brushless Motor Operation



Q_1, Q_2; Power MOS FET
D_1, D_2; Diode
ZD_1,ZD_2; Zener Diode
Tr ; Power Supply Transformer

Fig. 4-61 Structure of Drive Power Supply for Power MOS FET on Upside Arm

● Gate Drive Circuit with P,N Channel Complimentary Power MOS FET

As for bipolar transistor, the complimentary characteristics of current gain and high breakdown voltage for PNP type is difficult to design. As for Power MOS FET, high breakdown voltage and high current of P channel is rather easy.

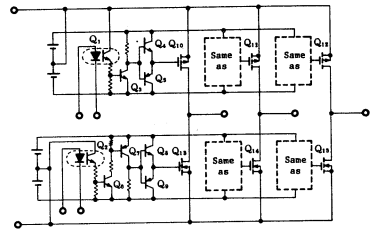
The circuit with P and N channel complimentary Power MOS FET is shown in Fig. 4-62. If P channel devices are used in upside arm of inverter and N channel devices are in the under arm, drive power supply are needed only for each arm. Table 4-5 shows comparison between P/N channel and all N channel complimentaly components about the number of components. The number of drive power supply for P/N channel is as half as that of all N channel one and the number of components for P/N channel is 24% less than that of all N channel.

The drive circuit can be thus significantly simplified.

Table 4-5 Comparison of the number of components between P/N channel complementary circuit, all N channel circuit

	P/N Channel Complementary Circuit		All N Channel Circuit	
	Upside Arm	Under Arm	Upside Arm	Under Arm
Transistor	9	12	12	12
Resistor	9	15	15	15
Photo Coupler	3	3	3	3
Drive Power Supply	5	5	15	5
Total	26	35	45	35
	61		80	

Note; Unit (piece)



Q_1 , Q_2 ; Photo Coupler
Q_3 ~ Q_9 ; Drive Transistor
Q_{10} ~ Q_{12} ; P Channel Power MOS FET (2SJ116)
Q_{13} ~ Q_{15} ; N Channel Power MOS FET (2SK313)

Fig. 4-62 Drive Circuit with P and N Channel Complementary Power MOS FET

4.1 Precautions in Handling the Built-in Diode

An built-in diode of the power MOS FET is used as a commutating diode in a motor control circuit. In this case, if the reverse voltage is charged immediately after a high current is supplied to the diode, it may be destroyed depending on the circuit and the operating conditions.

Fig. 4-63 and 4-64 shows a basic motor control circuit and the waveform of the motor control operation. These waveforms are at Q_2 and Q_3 off and Q_1 and Q_4 on. Q_4 is continuously on when Q_1 is chopping.

At gate drive signal entering G_1, Q_1 turns on and i_{D1} flows. When the current i_{D1} of Q_1 stops, the regenerative current i_F flows through the built-in diode of Q_2, by energy stored in the inductance of the motor. In this state, if Q_1 turns on, Q_2 is shortened because of the reverse recovery time t_{rr} of the built-in diode of Q_2, and excess recovery current i_{Dr} flows.

This excess recovery current may destroy the diode at a point in the shaded area in the figure, which indicates the period in which the built-in diode voltage recovers. Therefore, restricting the recovery current i_{Dr} is an effective method to prevent diode destruction. Table 4-6 shows the detailed circuit countermeasures.

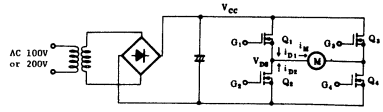
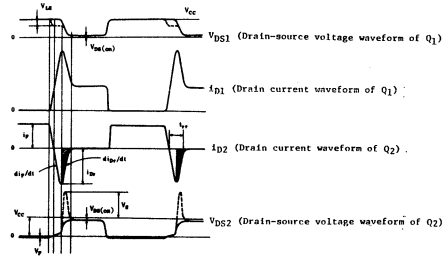


Fig. 4-63 Basic Motor Control Circuit

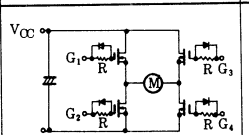
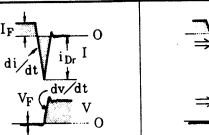
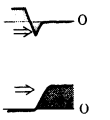
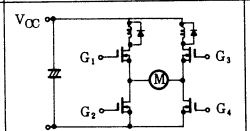
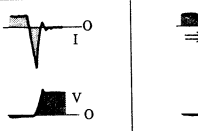
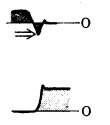
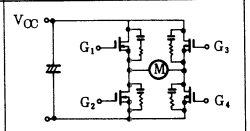
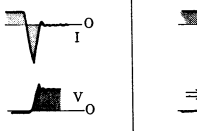
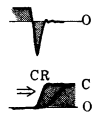
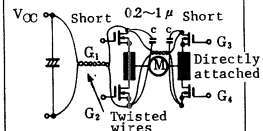
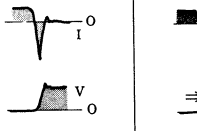
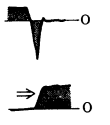
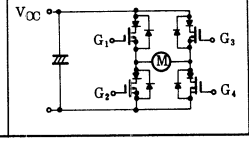
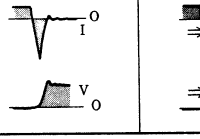
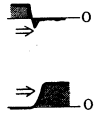


<Description>

i_F : Forward current of Q_2 built-in diode
V_F : Forward voltage drop of Q_2 built-in diode
$V_{DS(on)}$: Drain-source saturation voltage of Q_2
t_{rr}: Reverse recovery time of Q_2 built-in diode
V_{LS}: Voltage drop with circuit inductance Ls
i_{Dr}: Reverse recovery current of Q_2 built-in diode
(depends on the drive signal source impedence di_F/dt of Q_1, circuit inductance Ls, supply voltage V_{CC}, and electric charge Q_{rr} (or t_{rr}) in the built-in diode)
V_S : Spike voltage
(depends on the inductance Ls, i_{DR}, and di_{DR}/dt of the circuit)

Fig. 4-64 Waveform of the Motor Control Operation

Table 4-6 Circuit Countermeasures against Built-in Diode Destruction

Classification	Countermeasures	Circuit	Waveforms of the built-in diode		Circuit constants, etc.
			Before improvement	After improvement	
①	Delay the turn-on time, by inserting a resistor and diode which are connected in parallel into the gate of the Power MOS FET. This controls di/dt and dv/dt of the built-in diode to restrict the recovery current (in this case, the turn-off time does not have to be delayed).				$R = 330\,\Omega \sim 820\,\Omega$ ($di/dt = 20 \sim 50\,A/\mu s$)
②	Insert an L and diode connected in parallel into the drain of the Power MOS FET. This controls di/dt to restrict the recovery current i_{Dr}.				$L = 2\,\mu H \sim 20\,\mu H$
③	Insert a C or CR snubber between the drain and source of the Power MOS FET to restrict dv/dt and voltage spike of the built-in diode.				$R = 10 \sim 47\,\Omega$ $C = 0.01\,\mu F \sim 0.1\,\mu F$ Wiring of the snubber should be as short as possible.
④	Wires between +, - terminals of the power supply line and the drain/source of each arm (in the case of N/N) should be twisted C are also connected. By directly attaching wires to the upper and lower arms and minimizing stray the inductance, the voltage spike and dv/dt are restricted.				Should be done together with countermeasures ① to ③.
⑤	Connect the fast diode to the external of the Power MOS FET not to flow the current in the built-in diode.				

5. Analog Switch

When two power MOS FET's are connected in series, they operate as a two-way analog switch (Fig. 4-65).

Remember that the power MOS FET is made to have a diode between drain and source. When applying a positive bias between gate and source, the V_{DS} vs. I_D characteristics are as shown in Fig. 4-66.

When the current is small, the current flows through the channel in both FET's, therefore the V_{DS}-I_D characteristics is shown by a straight line of 2×R (R is ON resistance of one FET). When the current is further increased, it will flow through the diode of one FET and the V_{DS}-I_D characteristics approaches the diode characteristics.

Important characteristics of Power MOS FET for analog switch are on-resistance (Ron) and off-resistance (Roff) mentioned below.

(1) Ron

This is the remaining resistance at switch on. The lower, the better.

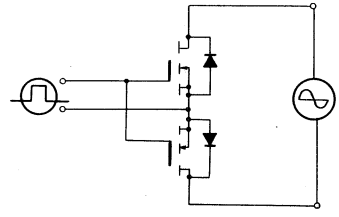


Fig. 4-65 Analog Switch

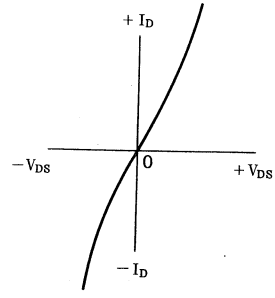


Fig. 4-66 V_{DS}-I_D Characteristics

(2) R_{off}

R_{off} is the resistance between the ends of the switch when the switch is open and is equivalent to insulation resistance of mechanical switch. The higher this resistance is, the better the switch is. It means that leak current (I_{DSS}, I_{DSX}) is small. (Several nA to several ten nA in general)

In low current area, R_{on} of the built-in diode of Power MOS FET can be small, applying positive gate-source bias (Fig. 4-67). It is superior to diode switch. When the gate-source bias is 0 or negative, the characteristics are the same as that of general diode. As Power MOS FET has enhancement characteristics, leak current remains unchanged when V_{GS} is applied 0.5 ~ 1.0V positive bias induced by, such as, external circuit noise.

Power MOS FET can show its ability to a bi-directional (it can switch alternative current) analog switch which has good linearity.

The characteristics of 2SK294 is shown in Fig. 4-68.

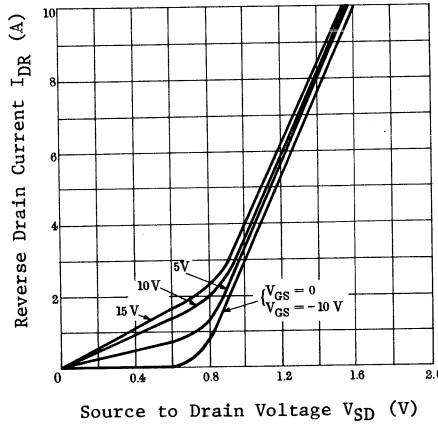


Fig. 4-67 Characteristics of Built-in Diode (2SK294)

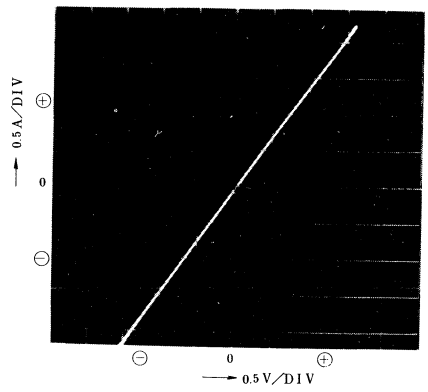
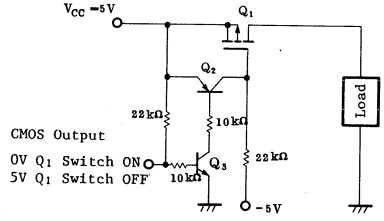


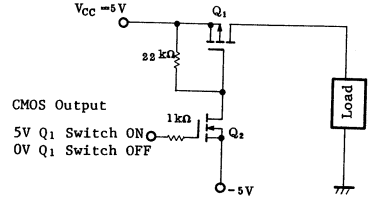
Fig. 4-68 Characteristics of 2SK294

The switching circuits, in which 2SJ120 and 2SJ121 are used, are shown in Fig. 4-69 and 4-70.



Q_1: 2SJ120 Q_2: 2SA1052
Q_3: 2SC2462

Fig. 4-69 Switching Circuit with 2SJ120



Q_1: 2SJ121
Q_2: 2SK416

Fig. 4-70 Switching Circuit with 2SJ121

6. Character Display

The recent increase in office automation has lead to the need for higher resolution color and monochrome displays requiring bandwidths of 40 to 80 MHz. To meet these requirements, the transistor used for video output should have high breakdown voltage, small I/O capacitances and excellent high frequency characteristics.

In a transistor, the breakdown voltage and the high frequency characteristics are contrary to each other, so it is difficult to realize 40 to 80MHz bandwidth current bipolar transistors for video output, because of their high frequency characteristics. By using the 2SK352 in high-resolution cathode-ray tube displays this bandwidth can be realized.

6.1 Features

Since the 2SK511 is designed to have small I/O capacitance and high gm, it can be used not only for video output but also for high-output, wide-band, high-impedance amplifiers in measuring instruments, etc. Table 4-7 and Table 4-8 show the absolute maximum ratings and the electrical characteristics respectively.

Table 4-7 ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	250	V
Gate to Source Voltage	V_{GSS}	±9	V
Drain Current	I_D	0.3	A
Drain peak Current	I_D(peak)	0.5	A
Channel Dissipation	Pch*	8	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55∿+150	°C

*T_C=25°C

Table 4-8 ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA , V_{GS}=0	250	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±9V , V_{DS}=0	-	-	± 1	mA
Drain Current	I_{DSS}	V_{DS}=200V , V_{GS}=0	-	-	1	mA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	1.0	-	5.0	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=0.1A , V_{GS}=9 V	-	3.0	5.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=0.15A , V_{DS}=20V	50	80	-	mS
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	20	-	pF
Output Capacitance	Coss		-	10	-	pF
Reverse Transfer Capacitance	Crss		-	2.5	-	pF

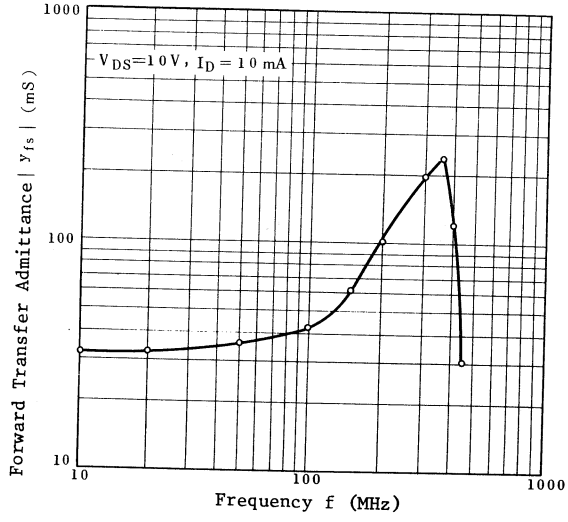


Fig. 4.71 $|y_{fs}|$ -f Characteristics

● Excellent high frequency characteristics

The 2SK511 has high cut-off frequency (f_C), 250MHz (typ). Compared with that of bipolar transistors (f_T=80MHz(typ); i.e. f_C=5MHz), it is 50 times higher. Fig. 4-71 shows $|y_{fs}|$ vs. frequency characteristics.

● Small I/O capacitances

In video amplifiers, the band width depends on the output capacitance (Coss). In the 2SK511, the output capacitance (Coss) is reduced to 10pF, and the input capacitance (Ciss), 20pF.

With small I/O capacitances, a high amplification factor is obtained, without reducing the mutual conductance($|y_{fs}|$ =80mS(typ)).

● ASO(Area of Safe Operation)

The 2SK511 has no secondary breakdown area. The rating of Pch=8W is guaranteed to the extent of V_{DS}=250V.

6.2 Application Notes

We would like to describe the use of the 2SK511 in a video output stage.

● Wide Band Width

The I/O capacitances of the 2SK511 are small, and to further reduce their effect, the common gate connection is recommended. In this case, the source will be driven by high speed TTL or a high speed switching transistor (2SC3652 etc.)

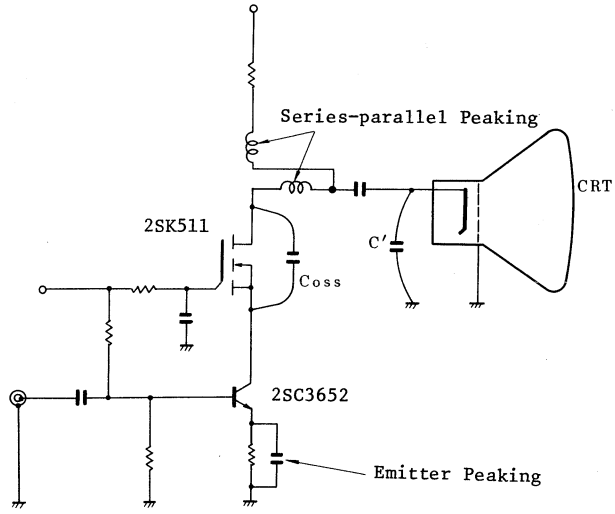


Fig. 4-72 Video Output Circuit

Generally, the high cut-off frequency of a RC coupled amplifier is determined by load resistance (R_L), the output capacitance (Coss) of the transistor and the cathode-ray tube's capacitance (C'). Therefore, to take advantage of the high frequency characteristics of the 2SK511, we recommend use of parallel, series, and emitter peaking. When using the 2SK352 in the digital (switching) mode, use a speed-up capacitor.

The 2SC3025 and the 2SC3026 (V_{CBO}=1500V, 1700V, I_C=5A, fall time t_f=0.5μs max.) are horizontal deflection output transistors for television receivers.

7. Ultrasonic Equipment

We would like to describe the power MOS FETs use in ultrasonic wave diagnostic equipment. Formerly, bipolar transistors have been used for high-voltage and high-speed switching devices used to generate pulse voltage for ultrasonic wave diagnostic equipment. Recently, as ultrasonic wave diagnostic equipment is required to have higher performance and higher operating frequency, the power MOS FETs small package, high breakdown voltage, and low ON resistance has LED to its use.

Fig. 4-73 shows the block diagram and Fig. 6-54 shows the high voltage pulse generator circuit and the voltage waveform. This circuit has the following functions. 1) The pulse voltage (Vp-p) is as large as possible 2) The frequency component of the pulse voltage oscillation waveform is high. The power MOS FET provides high switching speed and excellent frequency characteristics. By using power MOS FETs, ultrasonic wave diagnostic equipment can operate with high frequency and meets the conditions (1) and (2), resulting in clear pictures.

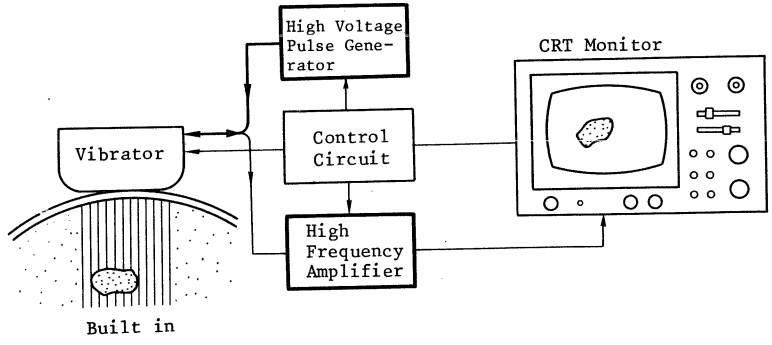


Fig. 4-73 Block Diagram

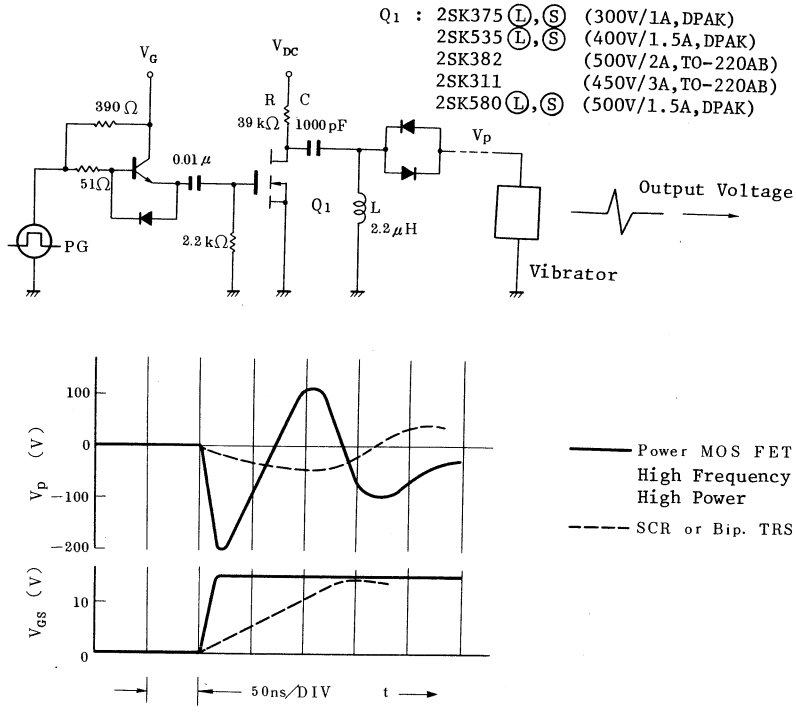


Fig. 4-74 High Voltage Pulse Generator & Waveform

8. Others

Power MOS FETs can be used for many applications, such as magnetic bubble memory driver, electrical discharge machine, laser pulser, actuator, relay driver, lamp driver, etc.

Reference Books

*1) Kurisu, Yoshida, Kiyama, Full---transistorized Medium Wave Broadcasting Transmitter Using Power MOS FET

*2) Aoyagi, Inoue, "Short Wave Broadcasting Transmitter using FET", Television Academy Technology Report, RE79-24

POWER-MOS FET
CROSS REFERENCE LIST

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TABLE OF CONTENTS

1. Toshiba 513
2. NEC 518
3. Matsushita 522
4. Fuji Electrik 524
5. Mitsubishi 527
6. International Rectifier 528
7. Siliconix 534
8. Motorola 538
9. Siemens 544
10. RCA 547

Note 1) The Hitachi devices are a „form, fit and function" replacement for the Indicated type number, but subtile differences in characteristics or specifications may exist. Refer to the individual specifications when you use.

Note 2) In Hitachi type number , „HS" means the device under development.

POWER MOSFET Cross Reference List

MAKER; TOSHIBA 1

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
2SK324	TO-3	400	10	0.45	0.60	2SK312	400	12	0.67	0.90
2SK325	TO-3	450	10	0.5	0.7	2SK313 2SK512	450 500	12	0.67 0.55	0.90 0.65
2SK355	TO-3	150	12	0.12	0.18					
2SK356	TO-3	250	12	0.20	0.25	2SK401	250	10	0.3	0.4
2SK357	TO-220AB	150	5	0.6	0.9					
2SK358	TO-220AB	250	5	0.7	1.0					
2SK385	TO-3PL	400	10	0.45	0.60	2SK556	450	12	0.40	0.55
2SK386	TO-3PL	450	10	0.5	0.7	2SK556	450	12	0.40	0.55
2SK387	TO-3PL	150	12	0.12	0.18	HS78157	150	15	0.12	0.15
2SK388	TO-3PL	250	12	0.20	0.25	2SK1135	250	15	0.16	0.22
2SK405	TO-3P	160	8	0.5	1.6	2SK414 2SK1058	160	8 7	0.4 1.0	0.5 1.6
2SK422	TO-92M	60	0.7	1.4	2.8					
2SK423	TO-92M	100	0.5	2.4	4.5					
2SK442	TO-220AB	70	10	0.2	0.4	2SK549 *2SK970	60	10	0.12	0.15
2SK447	TO-3PL	250	15	0.15	0.24	2SK1135	250	15	0.16	0.22
2SK525	TO-220FM	150	10	0.2	0.28	HS76127	120	10	0.15	0.20
2SK526	TO-220FM	250	10	0.4	0.6	2SK741	250	7	0.40	0.55
2SK527	TO-220FM	60	10	0.10	0.14	*2SK1093	60	10	0.12	0.15
2SK528	TO-220FM	400	2	1.6	2.2					
2SK529	TO-220FM	450	2	1.8	2.6					
2SK530	TO-220FM	400	5	1.0	1.4	HS76129	450	4	1.0	1.4
2SK531	TO-220FM	450	5	1.1	1.6	HA76129A	500	4	1.2	1.5
2SK532	TO-220FM	60	12	0.07	0.085	*2SK1094	160	15	0.055	0.065
2SK537	TO-220AB	900	1	8.2	9.0	2SK1199	900	2	5.0	7.0
2SK538	TO-3P	900	3	3.3	4.5	2SK534 HS78139	800 900	5	3.0	4.0
2SK539	TO-3PL	900	5	2.1	2.5	2SK695 HS78141	800 900	5 6	2.0	3.0
2SK568	TO-3PL	450	8	0.47	0.75	2SK682	450	12	0.40	0.55
2SK572	TO-3P	150	15	0.12	0.18	HS78157	150	15	0.12	0.15
2SK573	TO-3P	250	15	0.24	0.32	2SK1135	250	15	0.16	0.22
2SK578	TO-3P	150	15	0.15	0.22	2SK1135	250	15	0.16	0.22

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; TOSHIBA 2

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
2SK643	TO-3P	450	10	0.6	0.8	2SK641	450	10	0.6	0.8
2SK644	TO-3P	500	10	0.7	1.0	2SK642	500	10	0.7	1.0
2SK673	TO-220AB	60	15	0.085	0.11	*2SK971	60	15	0.055	0.065
2SK674	TO-220AB	60	25	0.04	0.06	*2SK971	60	15	0.055	0.065
2SK675	TO-3PL	60	40	0.03	0.045	HS78145	100	40	0.025	0.03
2SK678	TO-3PL	500	13	0.32	0.40	2SK560	500	15	0.3	0.4
2SK693	TO-3PL	450	13	0.32	0.40	2SK559	450	15	0.25	0.36
2SK694	TO-3PL	500	12	0.4	0.5	2SK557	500	12	0.45	0.60
2SK788	TO-3P	500	13	0.4	0.5	2SK557 HS78099A	500	12	0.45	0.60
2SK789	TO-3P	450	15	0.3	0.4	2SK559 HS78101	450	15	0.25	0.36
2SK790	TO-3P	500	15	0.3	0.4	2SK560 HS78101A	500	15	0.3	0.4
2SK791	TO-220AB	850	3	3.3	4.5	2SK513 HS76125	800	3	5 4.5	6 6
2SK792	TO-220AB	900	3	3.3	4.5	2SK1199	900	2	5.0	7.0
2SK793	TO-3P	850	5	2.1	2.5	2SK695	800	5	2.0	3.0
2SK794	TO-3P	900	5	2.1	2.5	2SK695 HS78141	800 900	5 6	2.0	3.0
2SK849	TO-3P	60	40	0.03	0.045					
2SK850	TO-3P	100	35	0.045	0.06	2SK622 *HS78147	150 100	20 30	0.06 0.05	0.75 0.06
2SK851	TO-3P	200	30	0.07	0.085					
2SK856	TO-220AB	60	45	0.02	0.03	*HS76099	60	27	0.02	0.025
2SK857	TO-3P	60	45	0.02	0.03	*HS78125	60	40	0.014	0.018
2SK858	TO-220AB	600	2	2.9	4.0					
2SK888	TO-220AB	100	15		0.18	2SK740	150	10	0.12	0.15
2SK889	TO-220AB	100	27		0.085	*HS76121	100	20	0.07	0.085
2SK890	TO-220AB	200	10		0.4	2SK741	250	7	0.40	0.55
2SK891	TO-220AB	200	18		0.18					
2SK892	TO-220AB	500	2.5		3.0	HS76079A	500	3	2.0	3.0
2SK893	TO-220AB	500	5		1.5	2SK553 *HS76091A	500	5	1.2	1.5
2SK894	TO-220AB	500	8		0.85	HS76093A	500	8	0.6	0.85
2SK895	TO-3P	450	12		0.55	2SK556 HS78099	450	12	0.40	0.55
2SK896	TO-3P	500	12		0.60	2SK557 HS78099A	500	12	0.45	0.60

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; TOSHIBA 3

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
YTF150	TO-3	100	40	0.045	0.055					
YTF151	TO-3	60	40	0.045	0.055					
YTF152	TO-3	100	33	0.06	0.08					
YTF153	TO-3	60	33	0.06	0.08					
YTF220	TO-3	200	5	0.5	0.8					
YTF221	TO-3	150	5	0.5	0.8					
YTF222	TO-3	200	4	0.8	1.2					
YTF223	TO-3	150	4	0.8	1.2					
YTF230	TO-3	200	9	0.25	0.40	2SK401	250	10	0.3	0.4
YTF231	TO-3	150	9	0.25	0.40					
YTF232	TO-3	200	8	0.4	0.6	2SK401	250	10	0.3	0.4
YTF233	TO-3	150	8	0.4	0.6					
YTF240	TO-3	200	18	0.14	0.18					
YTF241	TO-3	150	18	0.14	0.18					
YTF242	TO-3	200	16	0.20	0.22					
YTF243	TO-3	150	16	0.20	0.22					
YTF250	TO-3	200	30	0.07	0.085					
YTF251	TO-3	150	30	0.07	0.085					
YTF252	TO-3	200	25	0.09	0.12					
YTF253	TO-3	150	25	0.09	0.12					
YTF440	TO-3	500	8	0.80	0.85					
YTF441	TO-3	450	8	0.80	0.85					
YTF442	TO-3	500	7	1.0	1.1					
YTF443	TO-3	450	7	1.0	1.1					
YTF450	TO-3	500	13	0.3	0.4	2SK1064	500	15	0.3	0.4
YTF451	TO-3	450	13	0.3	0.4	2SK1063	450	15	0.25	0.36
YTF452	TO-3	500	12	0.4	0.5	2SK1064	500	15	0.3	0.4
YTF453	TO-3	450	12	0.4	0.5	2SK1063	450	15	0.25	0.36
YTF520	TO-220AB	100	8	0.25	0.30	2SK551	120	10	0.15	0.20
YTF521	TO-220AB	60	8	0.25	0.30	2SK549 * 2SK970	60	10	0.12	0.15

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; TOSHIBA 4

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
YTF522	TO-220AB	100	7	0.3	0.4	2SK551	120	10	0.15	0.20
YTF523	TO-220AB	60	7	0.3	0.4	2SK549 *2SK970	60	10	0.12	0.15
YTF530	TO-220AB	100	14	0.14	0.18	2SK551	120	10	0.15	0.20
YTF531	TO-220AB	60	14	0.14	0.18	2SK549 *2SK970	60	10	0.12	0.15
YTF532	TO-220AB	100	12	0.20	0.25	2SK551	120	10	0.15	0.20
YTF533	TO-220AB	60	12	0.20	0.25	2SK549 *2SK970	60	10	0.12	0.15
YTF540	TO-220AB	100	27	0.07	0.085	*HS76121	100	20	0.07	0.085
YTF541	TO-220AB	60	27	0.07	0.085	*2SK971	60	15	0.055	0.065
YTF542	TO-220AB	100	24	0.09	0.11	*HS76121	100	20	0.07	0.085
YTF610	TO-220AB	200	2.5	1.0	1.5					
YTF611	TO-220AB	150	2.5	1.0	1.5					
YTF612	TO-220AB	200	2	1.5	2.4					
YTF613	TO-220AB	150	2	1.5	2.4					
YTF620	TO-220AB	200	5	0.5	0.8					
YTF621	TO-220AB	150	5	0.5	0.8					
YTF622	TO-220AB	200	4	0.8	1.2					
YTF623	TO-220AB	150	4	0.8	1.2					
YTF630	TO-220AB	200	9	0.25	0.40	2SK741	250	7	0.40	0.55
YTF631	TO-220AB	150	9	0.25	0.40	2SK741	250	7	0.40	0.55
YTF632	TO-220AB	200	8	0.4	0.6	2SK741	250	7	0.40	0.55
YTF820	TO-220AB	500	2.5	2.5	3.0	HS76079A	500	3	2.0	3.0
YTF821	TO-220AB	450	2.5	2.5	3.0	HS76079	450	3	1.8	2.8
YTF822	TO-220AB	500	2	3.0	4.0	HS76079A	500	3	2.0	3.0
YTF823	TO-220AB	450	2	3.0	4.0	HS76079	450	3	1.8	2.8
YTF830	TO-220AB	500	4.5	1.3	1.5	2SK553 HS76091A	500	5	1.2	1.5
YTF831	TO-220AB	450	4.5	1.3	1.5	2SK552 HS76091	450	5	1.0	1.4
YTF832	TO-220AB	500	4	1.5	2.0	2SK553 HS76091A	500	5	1.2	1.5
YTF833	TO-220AB	450	4	1.5	2.0	2SK552 HS76091	450	5	1.0	1.4

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; TOSHIBA 5

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
YTF840	TO-220AB	500	8	0.8	0.85	2SK555 HS76093A	500	7 8	0.7 0.60	1.0 0.85
YTF841	TO-220AB	450	8	0.8	0.85	2SK554 HS76093	450	7 8	0.60 0.55	0.85 0.75
YTF842	TO-220AB	500	7	1.0	1.1	2SK555 HS76093A	500	7 8	0.7 0.60	1.0 0.85
YTF843	TO-220AB	450	7	1.0	1.1	2SK554 HS76093	450	7 8	0.60 0.55	0.85 0.75
YTFP150	TO-3P	100	40	0.045	0.055	*HS78147	100	30	0.05	0.06
YTFP151	TO-3P	60	40	0.045	0.055	*HS78147	100	30	0.05	0.06
YTFP152	TO-3P	100	33	0.06	0.08	*HS78147	100	30	0.05	0.06
YTFP153	TO-3P	60	33	0.06	0.08	*HS78147	100	30	0.05	0.06
YTFP450	TO-3P	500	13	0.3	0.4	2SK560 HS78101A	500	15	0.3	0.4
YTFP451	TO-3P	450	13	0.3	0.4	2SK559 HS78101	450	15	0.25	0.36
YTFP452	TO-3P	500	12	0.4	0.5	2SK560 HS78101A	500	15	0.3	0.4
YTFP453	TO-3P	450	12	0.4	0.5	2SK559 HS78101	450	15	0.25	0.36
2SJ115	TO-3P	-160	-8	0.7	1.6	2SJ119 2SJ162	-160	-8 -7	0.4 1.0	0.5 1.6
2SJ123	TO-220AB	-70	-10	0.2	0.4	2SJ122	-60	-10	0.15	0.2
2SJ126	TO-220FM	-60	-10	0.27	0.4	2SJ102	-60	-5	0.3	0.4

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; NEC 1

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
2SK338	TO-220AB	450	5	1.1	1.5	2SK552	450	5	1.0	1.4
2SK339	TO-220AB	100	5	0.35	0.5	2SK295	100	5	0.5	0.56
2SK446	DPAK	20	2	0.25	0.4	* 2SK973	60	2	0.25	0.35
2SK459	TO-220AB	200	10	0.35	0.5	2SK741	250	7	0.40	0.55
2SK462	DPAK	60	2	0.35	0.5	* 2SK973	60	2	0.25	0.35
2SK463	TO-220AB	60	5	0.18	0.3	* 2SK970	60	10	0.12	0.15
2SK464	TO-220AB	60	10	0.13	0.2	* 2SK970	60	10	0.12	0.15
2SK468	DPAK	100	2	0.5	1.0	2SK429	100	3	0.5	0.7
2SK470	TO-220AB	100	10	0.18	0.3	2SK551	120	10	0.15	0.20
2SK479	TO-3P	250	15	0.3	0.4	2SK412	250	10	0.3	0.4
2SK482	TO-220AB	450	5	1.3	2.0	2SK552	450	5	1.0	1.4
2SK484	TO-3P	450	8	0.8	1.0	2SK642	500	10	0.7	1.0
2SK490	TO-3P	400	10	0.7	0.8	2SK641	450	10	0.6	0.8
2SK542	TO-220AB	150	2	1.0	1.5					
* 2SK591	TO-220FM	60	15	0.035	0.055	* 2SK1095	60	25	0.033	0.04
* 2SK611	DPAK	100	1	3.0	5.0					
* 2SK612	DPAK	100	2	0.3	0.45	HS72027	100	3	0.3	0.45
* 2SK654	DPAK	100	1	1.2	3.0					
* 2SK659	TO-220FM	60	12	0.05	0.075	* 2SK1094	60	15	0.055	0.065
* 2SK679	TO-92	30	0.5	0.5	1.0	* 2SK975	60	1.5	0.3	0.4
* 2SK680	UPAK	30	1	0.5	1.0					
* 2SK681	TO-92M	30	1	0.5	1.0	* 2SK975	60	1.5	0.3	0.4
* 2SK699	TO-126	100	2	0.8	1.2					
* 2SK700	TO-126	80	2	0.6	0.8					
* 2SK701	TO-126	60	2	0.4	0.6					
* 2SK702	TO-220AB	100	5	0.2	0.45					
* 2SK704	TO-220AB	60	5	0.11	0.25	* 2SK970	60	10	0.12	0.15
* 2SK705	TO-220FM	60	5	0.11	0.25	* 2SK1093	60	10	0.12	0.15
2SK707	TO-3P	250	25	0.12	0.15	2SK623	250	20	0.12	0.15
2SK719	TO-3P	900	5	3.2	4.0	2SK534 HS78139	800 900	5	3.0	4.0

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; NEC 2

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS}(on)$ (Ω) typ.	$R_{DS}(on)$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS}(on)$ (Ω) typ.	$R_{DS}(on)$ (Ω) max.
2SK720A	TO-3P	250	20	0.18	0.23	* 2SK1135	250	15	0.17	0.22
* 2SK736	TO-220FM	100	15	0.055	0.08	* HS76123	100	20	0.07	0.085
* 2SK737	TO-220FM	100	12	0.075	0.15	* HS76123	100	20	0.07	0.085
* 2SK738	DPAK	30	2	(0.11)	0.17	* 2SK974	60	3	0.15	0.18
* 2SK739	DPAK	60	2	(0.11)	0.25	* 2SK974	60	3	0.15	0.18
2SK773	TO-3P	500	12	0.47	0.60	2SK557	500	12	0.45	0.60
2SK774	TO-3P	500	18	0.35	0.45	2SK560	500	15	0.3	0.40
2SK784	TO-3P	450	20	0.25	0.35	2SK559 HS78101	450	15	0.25	0.36
2SK785	TO-3P	500	20	0.30	0.40	2SK560 HS78101A	500	15	0.30	0.40
2SK786	TO-220AB	900	3	6	7.5	2SK513 2SK1199	800 900	3 2	5 5	6 7
2SK787	TO-3P	900	8	1.25	1.6	2SK684 HS78143	800 900	7 8	1.0 1.2	1.5 1.6
* 2SK797	TO-3P	60	40	0.014	0.018	* HS78125	60	40	0.014	0.018
* 2SK798	TO-3P	100	40	0.022	0.031	HS78145	100	40	0.025	0.03
2SK799	TO-3P	450	12	0.4	0.5	2SK556	450	12	0.4	0.55
2SK800	TO-3P	450	18	0.32	0.38	2SK559	450	15	0.25	0.36
* 2SK801	DPAK	30	2	0.20	0.35	* 2SK973	60	3	0.25	0.35
* 2SK802	TO-126	30	2	0.20	0.35					
* 2SK810	TO-220AB	100	14	0.10	0.18	2SK740	150	10	0.12	0.15
* 2SK811	TO-220FM	100	12	0.10	0.18	HS76127	120	10	0.15	0.20
* 2SK812	TO-220AB	60	27	0.07	0.085	* 2SK971	60	15	0.055	0.065
* 2SK813	TO-220FM	60	21	0.07	0.085	* 2SK1094	60	15	0.055	0.065
* 2SK815	TO-220FM	100	21	0.06	0.085	* HS76123	100	20	0.07	0.085
* 2SK817	TO-220FM	60	26	0.03	0.055	* 2SK1095	60	25	0.033	0.04
2SK819	TO-3P	500	10	0.7	1.0	2SK642 HS78131A	500	10	0.7	1.0
2SK820	TO-3PFM	250	20	0.18	0.26					
2SK821	TO-3P	250	20	0.18	0.23	2SK1135	250	15	0.17	0.22
2SK822	TO-3PFM	250	25	0.12	0.15					
2SK823	TO-3P	250	25	0.12	0.15	2SK623	250	20	0.12	0.15
2SK824	TO-3PFM	450	15	0.4	0.5					
2SK825	TO-3P	450	15	0.4	0.5	2SK556 HS78099	450	12	0.4	0.55

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; NEC 3

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
2SK826	TO-3PFM	450	18	0.32	0.38					
2SK827	TO-3P	450	18	0.32	0.38	2SK559 HS78101	450	15	0.25	0.36
2SK828	TO-3PFM	500	15	0.47	0.60					
2SK829	TO-3P	500	15	0.47	0.60	2SK557 HS78099A	500	12	0.45	0.60
2SK830	TO-3PFM	500	18	0.35	0.45					
2SK831	TO-3P	500	18	0.35	0.45	2SK560 HS78101A	500	15	0.30	0.40
2SK832	TO-3PFM	900	5	3.2	4.0					
2SK833	TO-3P	900	5	3.2	4.0	2SK534 HS78139	800 900	5	3.0	4.0
2SK834	TO-3PFM	900	8	1.2	1.6					
* 2SK835	TO-3PFM	60	40	0.014	0.018	* HS78127	60	40	0.014	0.018
* 2SK836	TO-3PFM	100	40	0.022	0.031					
2SK837	TO-3PFM	450	20	0.25	0.35					
2SK838	TO-3PFM	500	20	0.3	0.4					
2SK854	TO-220AB	450	5	1.1	1.4	2SK552 HS76091	450	5	1.0	1.4
2SK855	TO-220AB	500	5	1.2	1.5	2SK553 HS76091A	500	5	1.2	1.5
2SK871	TO-3P	900	4		5.5	HS78149	900	4	4.0	5.5
2SK872	TO-3P	900	6		3.0	2SK695 HS78141	800 900	5 6	2.0	3.0
2SK873	TO-3P	450	8		1.1	2SK641 HS78131	450	10	0.6	0.8
2SK874	TO-3P	500	8		1.2	2SK642 HS78131A	500	10	0.7	1.0
2SK875	TO-3P	450	12		0.6	HS78097	450	11	0.55	0.75
2SK876	TO-3P	500	12		0.7	HS78097A	500	11	0.6	0.85
2SK946	TO-220FM	900	3		5.5					
2SK985	TO-220FM	900	2		7.5					
* 2SK991	TO-220AB	100	4		0.6					
* 2SK992	TO-220FM	100	4		0.6					
* 2SK993	TO-220AB	60	8		0.3					
* 2SK994	TO-220FM	60	8		0.3					

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; NEC 4

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS}(on)$ (Ω) typ.	$R_{DS}(on)$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS}(on)$ (Ω) typ.	$R_{DS}(on)$ (Ω) max.
* 2SJ128	DPAK	-100	-2	0.8	1.0					
* 2SJ132	DPAK	-30	-2		0.4					
* 2SJ133	DPAK	-60	-2		0.8					
* 2SJ134	TO-220AB	-100	-6		0.6					
* 2SJ135	TO-220FM	-100	-5		0.6					
* 2SJ136	TO-220AB	-60	-12		0.3	2SJ102	-60	-5	0.3	0.4
* 2SJ137	TO-220FM	-60	-10		0.3					
* 2SJ138	TO-220AB	-100	-12		0.3	2SJ127	-120	-10	0.2	0.25
* 2SJ139	TO-220FM	-100	-10		0.3					
* 2SJ140	TO-220AB	-60	-19		0.2	2SJ122 * HS76080	-60	-10 -15	0.15 0.09	0.20 0.11
* 2SJ141	TO-220FM	-60	-13		0.2	* HS76082	-60	-15	0.09	0.11
* 2SJ142	TO-220FM	-100	-13		0.2					
* 2SJ143	TO-220FM	-60	-16		0.15	* HS76082	-60	-15	0.09	0.11
* 2SJ151	TO-220AB	-100	-3		1.2					
* 2SJ152	TO-220FM	-100	-3		1.2					
* 2SJ153	TO-220AB	-60	-6		0.6					
* 2SJ154	TO-220FM	-60	-5		0.6					

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; MATSUSHITA 1

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
2SK742/A	TO-220FM	50/60	5		0.22	*2SK1093	60	10	0.12	0.15
2SK743/A	TO-220FM	50/60	8		0.15	*2SK1093	60	10	0.12	0.15
2SK744/A	TO-220FM	50/60	10		0.12	*2SK1093	60	10	0.12	0.15
2SK745/A	TO-3P	50/60	20		0.055					
2SK746/A	TO-3PFM	50/60	20		0.055					
2SK747/A	TO-220FM	100/120	5		0.55					
2SK748/A	TO-220FM	100/120	8		0.22	HS76127	120	10	0.15	0.20
2SK749/A	TO-220FM	100/120	10		0.18	HS76127	120	10	0.15	0.20
2SK750/A	TO-3P	100/120	20		0.08	*HS78147	100	30	0.05	0.06
2SK751/A	TO-3PFM	100/120	20		0.08					
2SK752	TO-220FM	160	3		1.0					
2SK753	TO-220FM	160	5		0.5					
2SK754	TO-220FM	160	10		0.22	2SK740	150	10	0.12	0.15
2SK755	TO-220FM	200	5		0.50	2SK741	250	7	0.40	0.55
2SK756	TO-220FM	200	8		0.53	2SK741	250	7	0.40	0.55
2SK757	TO-220FM	200	10		0.33	2SK741	250	7	0.40	0.55
2SK758	TO-220FM	250	5		0.70	2SK741	250	7	0.40	0.55
2SK759	TO-220FM	250	8		0.40	2SK741	250	7	0.40	0.55
2SK760	TO-3P	250	15		0.22	2SK1135	250	7	0.16	0.22
2SK761	TO-3PFM	250	15		0.22					
2SK762/A	TO-220FM	400/450	3		3.0	HS76079	450	3	1.8	2.8
2SK763/A	TO-220FM	400/450	5		1.4	HS76129	450	4	1.0	1.4
2SK764/A	TO-220FM	400/450	10		0.75	2SK554 HS76093	450	7 8	0.6 0.55	0.85 0.75
2SK765/A	TO-3PFM	400/450	10		0.75					
2SK766	TO-220FM	500	3		3.6	HS76079A	500	3	2.0	3.0
2SK767	TO-220FM	500	5		1.8	HS76129A	500	4	1.2	1.5
2SK768	TO-3P	500	10		1.0	HS78131A	500	10	0.7	1.0
2SK769	TO-3PFM	500	10		1.0					
2SK770	TO-220FM	600	2		5.0					
2SK782	N型	200	5		0.5					

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; MATSUSHITA 2

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
2SK795	I型	600	2		5.0					
2SK796/A	TO-3PFM	800/900	3		5.0	2SK1200	900	3	5	7
2SK803	TO-220FM	160	8		0.38					
2SK804	TO-3PFM	160	20		0.12					
2SK805	TO-3PFM	200	20		0.18					
2SK806	TO-220FM	600	3		2.7					
2SK807	TO-3PFM	600	5		1.7					
2SK808/A	TO-220FM	800/900	1		7.0	2SK513 2SK1199	800 900	3 2	5.0 5.0	6.0 7.0
2SK809/A	TO-3PFM	800/900	5		3.0					
2SK818/A	TO-3P	800/900	5		3.0	2SK695 HS78141	800 900	5 6	2.0	3.0
2SK863/A	TO-3P	50/60	30		0.05					
2SK864/A	TO-3P	50/60	50		0.04					
2SK865/A	TO-3P	100/120	30		0.065	* HS78147	100	30	0.05	0.06
2SK866/A	TO-3P	100/120	50		0.05	* HS78147	100	30	0.05	0.06
2SK867/A	TO-3P	400/450	15		0.45	2SK556 HS78099	450	12	0.40	0.55
2SK868/A	TO-3P	400/450	20		0.35	2SK559 HS78101	450	15	0.25	0.36
2SK869	TO-3P	500	15		0.50	2SK557 HS78099A	500	12	0.45	0.60
2SK870	TO-3P	500	20		0.40	2SK560 HS78101A	500	15	0.3	0.4
2SK996	TO-220FM	600	4		1.8					
2SK1030A	TO-220FM	900	3		5.0					
2SK1032A	TO-3P	900	8		1.8	HS78143	900	8	1.2	1.6
2SK1033A	TO-220FM	60	15		0.07	* 2SK1094	60	15	0.055	0.065
2SK1034	TO-220FM	100	15		0.12	* HS76123	100	20	0.07	0.085
2SJ156A	TO-220FM	-60	-5		0.22					
2SJ158A	TO-220FM	-100	-5		0.55					
2SJ159	TO-220FM	-160	-3		1.0					

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; Fuji Electronic 1

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
2SK562	TO-3P	50	39	0.035	0.04					
2SK562A	TO-3P	50	45		0.03					
2SK564	TO-3P	100	32	0.045	0.06	2SK622 *HS78147	150 100	20 30	0.06 0.05	0.075 0.06
2SK565	TO-3P	500	9.6	0.55	0.60	2SK557	500	12	0.45	0.60
2SK565A	TO-3P	500	8.3	0.7	0.8	2SK642	500	10	0.7	1.0
2SK566	TO-3P	800	2.9	3.5	4.0	2SK534	800	5	3.0	4.0
2SK566A	TO-3P	800	3.4	2.7	3.0	2SK695	800	5	2.0	3.0
2SK616	TO-3P	200	22	0.09	0.12	2SK623	250	20	0.12	0.15
2SK724	TO-3P	500	10	0.50	0.67	2SK557 HS78099A	500	12	0.45	0.60
2SK725	TO-3P	500	15	0.28	0.38	2SK560 HS78101A	500	15	0.30	0.40
2SK726	TO-3P	900	3	3.5	5.0	2SK534 HS78139	800 900	5	3.0	4.0
2SK727	TO-3P	900	5	2.0	2.5	2SK695 HS78141	800 900	5 6	2.0	3.0
2SK783	TO-3P	500	12	0.45	0.57	2SK557 HS78099A	500	12	0.45	0.60
2SK859	TO-3P	500	9	0.7	0.8	2SK683	500	12	0.45	0.60
2SK723	TO-3P	500	7		1.2	2SK642 HS78131A	500	10	0.7	1.0
2SK897	TO-220FM	550	4		1.5					
2SK899	TO-3P	500	18		0.33	HS78103A	500	20	0.22	0.27
2SK900	TO-220AB	200	12		0.3	2SK741	250	7	0.4	0.55
2SK901	TO-3P	250	20		0.15	2SK623	250	20	0.12	0.15
2SK902	TO-3P	250	30		0.1					
2SK903	TO-220FM	800	3		4.0					
2SK904	TO-220AB	800	3		4.0					
2SK905	TO-3P	50	45		0.03	*HS78125	60	40	0.015	0.018
2SK906	TO-3P	100	32		0.06	*HS78147	100	30	0.05	0.06
2SK949	TO-220FM	500	6		1.2	HS76129A	500	4	1.2	1.5
2SK950	TO-220AB	500	6		1.2	2SK553 HS76091A	500	5	1.2	1.5
2SK951	TO-220FM	800	2.5		7.0					
2SK952	TO-220AB	800	2.5		7.0	2SK513 2SK1199	800 900	3 2	5.0	6.0 7.0
2SK953	TO-3P	800	2.5		7.0	2SK415 2SK1200	800 900	3	5.0 5.5	6.0 7.0
2SK954	TO-3P	800	3		4.0	2SK534 HS78139	800 900	5	3.0	4.0

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; Fuji Electronic 2

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
2SK955	TO-3P	800	5		2.0	2SK695	800	5	2.0	3.0
2SK956	TO-3P	800	9		1.5	2SK684	800	7	1.0	1.5
2SK957	TO-220FM	900	2		8.5					
2SK958	TO-220AB	900	2		8.5	2SK1199	900	2	5.0	7.0
2SK959	TO-3P	900	2		8.5	2SK1200	900	2	5.5	7.0
2SK960	TO-220FM	900	3		5.0					
2SK961	TO-220AB	900	3		5.0	2SK1199	900	2	5.0	7.0
2SK962	TO-3P	900	8		2.0	HS78141	900	6	2.0	3.0
2SK1007	TO-220AB	450	5		1.6	2SK552 HS76091	450	5	1.0	1.4
2SK1008	TO-220AB	500	4.5		2.2	2SK553 HS76091A	500	5	1.2	1.5
2SK1009	TO-220AB	450	7		1.3	2SK552 HS76091	450	5	1.0	1.4
2SK1010	TO-220AB	500	6		1.6	2SK553 HS76091A	500	5	1.2	1.5
2SK1011	TO-3P	450	10		0.65	2SK641 HS78097	450	10 11	0.6 0.55	0.8 0.75
2SK1012	TO-3P	500	10		0.9	2SK642 HS78097A	500	10 11	0.7 0.6	1.0 0.85
2SK1013	TO-3P	450	13		0.6	2SK556 HS78099	450	12	0.4	0.55
2SK1014	TO-3P	500	12		0.74	2SK557 HS78099A	500	12	0.45	0.60
2SK1015	TO-3P	450	18		0.45	2SK556 HS89099	450	12	0.4	0.55
2SK1016	TO-3P	500	15		0.55	2SK557 HS78099A	500	12	0.45	0.60
2SK1017	TO-3P	450	20		0.35	2SK559 HS78101	450	15	0.25	0.36
2SK1018	TO-3P	500	18		0.42	2SK560 HS78101A	500	15	0.30	0.40
2SK1019	TO-3PL	450	35		0.20	HS78103	450	20	0.20	0.26
2SK1020	TO-3PL	500	30		0.25	HS78103A	500	20	0.22	0.27
2SK1021	TO-220AB	800	3		6.0	2SK513 2SK1199	800 900	3 2	5.0	6.0 7.0
2SK1022	TO-220AB	900	2.5		7.3	2SK1199	900	2	5.0	7.0
2SK1023	TO-220AB	800	4		4.5					
2SK1024	TO-220AB	900	3.5		5.5	2SK1199	900	2	5.0	7.0
2SK1081	TO-3P	800	7		2.2	2SK695	800	5	2.0	3.0
2SK1082	TO-3P	900	6		2.8	HS78141	900	6	2.0	3.0
*2SK1083	TO-220FM	60	8		0.22	*2SK1093	60	10	0.12	0.15
*2SK1084	TO-220FM	100	5		0.5					

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; Fuji Electronic 3

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
* 2SK1085	TO-220FM	150	3		0.9					
* 2SK1086	TO-220FM	60	20		0.07	* 2SK1094	60	15	0.055	0.065
* 2SK1087	TO-220FM	100	12		0.17					
* 2SK1088	TO-220FM	150	9		0.3					
* 2SK1089	TO-3P	60	35		0.035					
* 2SK1090	TO-3P	100	20		0.08	* HS78147	100	30	0.05	0.06
* 2SK1091	TO-3P	150	15		0.15					

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; MITSUBISHI

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
2SK728	SOT-89	300	0.3	15	30					
2SK729	TO-92M	300	0.3	15	30					
2SK730	DPAK	300	0.3	15	30	2SK384	500	0.3	25	50
2SK731	TO-220FM	300	0.3	15	30	2SK296	300	1	2.5	4.0
2SK732	TO-220FM	450	10	0.75	0.9	2SK554	450	7	0.6	0.85
2SK733	TO-3P	450	10	0.75	0.9	2SK641	450	10	0.6	0.8
2SK734	TO-3P	450	15	0.40	0.56	2SK556	450	12	0.40	0.55
2SK843	TO-220FM	60	10	0.10	0.13	* 2SK1093	60	10	0.12	0.15
2SK844	TO-220FM	100	8	0.15	0.20	HS76127	120	10	0.15	0.20
2SK845	TO-220FM	450	5	1.0	1.3	HS76129	450	4	1.0	1.4
2SK846	TO-220FM	900	3	3.0	4.0	2SK513 2SK1199	800 900	3 2	5.0	6.0 7.0
2SK847	TO-3P	900	3	3.0	4.0	2SK534 HS78139	800 900	5	3.0	4.0
2SK934	TO-220FM	250	8	0.4		2SK741	250	7	0.40	0.55
2SK935	TO-220FM	300	8	0.45	0.6	2SK741	250	7	0.40	0.55
2SK936	TO-220FM	50	30	0.03	0.04	* 2SK1095	60	25	0.033	0.04
2SK987	TO-220FM	500	5	1.2	1.6	HS76129A	500	4	1.2	1.5
2SK988	TO-220FM	500	10	0.7	0.9	2SK555	500	7	0.7	1.0
2SK989	TO-3P	500	10	0.7	0.9	2SK642 HS78097A	500	10 11	0.7 0.6	1.0 0.85
2SK990	TO-3P	500	15	0.5	0.65	2SK557 HS78099A	500	12	0.45	0.60
2SK1027	TO-3P	300	20	0.22	0.29	2SK1135	250	15	0.16	0.22
2SK1045	TO-3P	900	5	1.4	1.8	2SK684 HS78143	800 900	7 8	1.0 1.2	1.5 1.6
2SK1025	TO-220FM	50	20	0.08		* 2SK1094	60	15	0.055	0.065
2SK1026	TO-3P	250	20	0.2		2SK1135	250	15	0.16	0.22
2SK1044	TO-3P	800	5	1.3		2SK684	800	7	1.0	1.5
2SK1047	TO-3P	250	20	0.2		2SK1135	250	15	0.16	0.22
2SK1048	TO-3P	300	20	0.22						
2SK1049	TO-3P	450	15	0.5		2SK682	450	12	0.40	0.55
2SK1050	TO-3P	500	15	0.6		2SK683	500	12	0.45	0.60
2SK1051	TO-3P	50	40	0.03						

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; INTERNATIONAL RECTIFIER (IR) 1

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
IRF330	TO-3	400	5.5	0.8	1.0	2SK298	400	8	1.1	1.75
IRF331	TO-3	350	5.5	0.8	1.0	2SK298	400	8	1.1	1.75
IRF332	TO-3	400	4.5	1.0	1.5	2SK298	400	8	1.1	1.75
IRF333	TO-3	350	4.5	1.0	1.5	2SK298	400	8	1.1	1.75
IRF340	TO-3	400	10	0.47	0.55	2SK312	400	12	0.67	0.90
IRF341	TO-3	350	10	0.47	0.55	2SK312	400	12	0.67	0.90
IRF342	TO-3	400	8	0.68	0.80	2SK312	400	12	0.67	0.90
IRF343	TO-3	350	8	0.68	0.80	2SK312	400	12	0.67	0.90
IRF430	TO-3	500	4.5	1.3	1.5					
IRF431	TO-3	450	4.5	1.3	1.5	2SK299	450	8	1.1	1.75
IRF432	TO-3	500	4.0	1.5	2.0					
IRF433	TO-3	450	4.0	1.5	2.0	2SK299	450	8	1.1	1.75
IRF440	TO-3	500	8	0.8	0.85	2SK512	500	12	0.55	0.65
IRF441	TO-3	450	8	0.8	0.85	2SK313	450	12	0.67	0.90
IRF442	TO-3	500	7	1.0	1.1					
IRF443	TO-3	450	7	1.0	1.1	2SK313	450	12	0.67	0.90
IRF450	TO-3	500	13	0.3	0.4	2SK1064	500	15	0.3	0.4
IRF451	TO-3	450	13	0.3	0.4	2SK1063	450	15	0.25	0.36
IRF452	TO-3	500	12	0.4	0.5	2SK1064	500	15	0.3	0.4
IRF453	TO-3	450	12	0.4	0.5	2SK1063	450	15	0.25	0.36
IRF460	TO-3	500	21	0.24	0.27					
IRF462	TO-3	500	19	0.27	0.35					
IRFP130	TO-3P	100	14	0.14	0.18	2SK399	100	10	0.2	0.25
IRFP131	TO-3P	60	14	0.14	0.18	2SK399	100	10	0.2	0.25
IRFP132	TO-3P	100	12	0.20	0.25	2SK399	100	10	0.2	0.25
IRFP133	TO-3P	60	12	0.20	0.25	2SK399	100	10	0.2	0.25
IRFP140	TO-3P	100	27	0.07	0.085	2SK622	150	20	0.06	0.075
						*HS78147	100	30	0.05	0.06
IRFP141	TO-3P	60	27	0.07	0.085	2SK622	150	20	0.06	0.075
IRFP142	TO-3P	100	24	0.09	0.11					
IRFP143	TO-3P	60	24	0.09	0.11					

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; INTERNATIONAL RECTIFIER (IR) 2

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
IRFP150	TO-3P	100	40	0.045	0.055	2SK622 *HS78147	150 100	20 30	0.06 0.05	0.075 0.06
IRFP151	TO-3P	60	40	0.045	0.055	*HS78147	100	30	0.05	0.06
IRFP152	TO-3P	100	33	0.06	0.08	2SK622 *HS78147	150 100	20 30	0.06 0.05	0.075 0.06
IRFP153	TO-3P	60	33	0.06	0.08	*HS78147	100	30	0.05	0.06
IRFP230	TO-3P	200	9	0.25	0.4	2SK400	200	8	0.5	0.7
IRFP231	TO-3P	150	9	0.25	0.4	2SK414	160	8	0.4	0.5
IRFP232	TO-3P	200	8	0.4	0.6	2SK400	200	8	0.5	0.7
IRFP233	TO-3P	150	8	0.4	0.6	2SK414	160	8	0.4	0.5
IRFP240	TO-3P	200	18	0.14	0.18	2SK623 2SK1135	250	20 15	0.12 0.16	0.15 0.22
IRFP241	TO-3P	150	18	0.14	0.18	HS78157	150	15	0.12	0.15
IRFP242	TO-3P	200	16	0.20	0.22	2SK1135	250	15	0.16	0.22
IRFP243	TO-3P	150	16	0.20	0.22	HS78157	150	15	0.12	0.15
IRFP250	TO-3P	200	30	0.07	0.085					
IRFP251	TO-3P	150	25	0.07	0.085	2SK622	150	20	0.06	0.075
IRFP252	TO-3P	200	30	0.09	0.12	2SK623	250	20	0.12	0.15
IRFP253	TO-3P	150	25	0.09	0.12	2SK622	150	20	0.06	0.075
IRFP430	TO-3P	500	4.5	1.3	1.5					
IRFP431	TO-3P	450	4.5	1.3	1.5					
IRFP432	TO-3P	500	4.0	1.5	2.0					
IRFP433	TO-3P	450	4.0	1.5	2.0					
IRFP440	TO-3P	500	8	0.8	0.85	2SK642 HS78097A	500	10 11	0.7 0.6	1.0 0.85
IRFP441	TO-3P	450	8	0.8	0.85	2SK641 HS78097	450	10 11	0.6 0.55	0.8 0.75
IRFP442	TO-3P	500	7	1.0	1.1	2SK642 HS78097A	500	10 11	0.7 0.6	1.0 0.85
IRFP443	TO-3P	450	7	1.0	1.1	2SK641 HS78097	450	10 11	0.6 0.55	0.8 0.75
IRFP450	TO-3P	500	13	0.3	0.4	2SK560 HS78101A	500	15	0.30	0.40
IRFP451	TO-3P	450	13	0.3	0.4	2SK559 HS78101	450	15	0.25	0.36
IRFP452	TO-3P	500	12	0.4	0.5	2SK560 HS78101A	500	15	0.30	0.40
IRFP453	TO-3P	450	12	0.4	0.5	2SK559 HS78101	450	15	0.25	0.36
IRFP460	TO-3P	500	21	0.24	0.27	HS78103A	500	20	0.22	0.27
IRFP462	TO-3P	500	19	0.27	0.35	HS78103A	500	20	0.22	0.27

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; INTERNATIONAL RECTIFIER (IR) 3

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
IRF520	TO-220AB	100	8	0.25	0.3					
IRF521	TO-220AB	60	8	0.25	0.3	2SK346	60	5	0.3	0.45
IRF522	TO-220AB	100	7	0.3	0.4					
IRF523	TO-220AB	60	7	0.3	0.4	2SK346	60	5	0.3	0.4
IRF530	TO-220AB	100	14	0.14	0.18	2SK551	120	10	0.15	0.20
IRF531	TO-220AB	60	14	0.14	0.18	2SK549 * 2SK970	60	10	0.12	0.15
IRF532	TO-220AB	100	12	0.20	0.25	2SK551	120	10	0.15	0.20
IRF533	TO-220AB	60	12	0.20	0.25	2SK549 * 2SK970	60	10	0.12	0.15
IRF540	TO-220AB	100	27	0.07	0.085	* HS76121	100	20	0.07	0.085
IRF541	TO-220AB	60	27	0.07	0.085	* 2SK971	60	15	0.055	0.065
IRF542	TO-220AB	100	24	0.09	0.11	* HS76121	100	20	0.07	0.085
IRF543	TO-220AB	60	24	0.09	0.11	* 2SK971	60	15	0.055	0.065
IRF620	TO-220AB	200	5	0.5	0.8					
IRF621	TO-220AB	150	5	0.5	0.8					
IRF622	TO-220AB	200	4	0.8	1.2					
IRF623	TO-220AB	150	4	0.8	1.2					
IRF630	TO-220AB	200	9	0.25	0.4	2SK741	250	7	0.40	0.55
IRF631	TO-220AB	150	9	0.25	0.4	2SK741	250	7	0.40	0.55
IRF632	TO-220AB	200	8	0.4	0.6	2SK741	250	7	0.40	0.55
IRF633	TO-220AB	150	8	0.4	0.6	2SK741	250	7	0.40	0.55
IRF640	TO-220AB	200	18	0.14	0.18					
IRF641	TO-220AB	150	18	0.14	0.18	2SK740	150	10	0.12	0.15
IRF642	TO-220AB	200	16	0.20	0.22					
IRF643	TO-220AB	150	16	0.20	0.22	2SK740	150	10	0.12	0.15
IRF820	TO-220AB	500	2.5	2.5	3.0	HS76079A	500	3	2.0	3.0
IRF821	TO-220AB	450	2.5	2.5	3.0	HS76079	450	3	1.8	2.8
IRF822	TO-220AB	500	2.0	3.0	4.0	HS76079A	500	3	2.0	3.0
IRF823	TO-220AB	450	2.0	3.0	4.0	HS76079	450	3	1.8	2.8
IRF830	TO-220AB	500	4.5	1.3	1.5	2SK553 HS76091A	500	5	1.2	1.5
IRF831	TO-220AB	450	4.5	1.3	1.5	2SK552 HS76091	450	5	1.0	1.4

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; INTERNATIONAL RECTIFIER (IR) 4

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
IRF832	TO-220AB	500	4	1.5	2.0	2SK553 HS76091A	500	5	1.2	1.5
IRF833	TO-220AB	450	4	1.5	2.0	2SK552 HS76091	450	5	1.0	1.4
IRF840	TO-220AB	500	8	0.8	0.85	2SK555 HS76093A	500	7 8	0.7 0.6	1.0 0.85
IRF841	TO-220AB	450	8	0.8	0.85	2SK554 HS76093	450	7 8	0.6 0.55	0.85 0.75
IRF842	TO-220AB	500	7	1.0	1.1	2SK555 HS76093A	500	7 8	0.7 0.6	1.0 0.85
IRF843	TO-220AB	450	7	1.0	1.1	2SK554 HS76093	450	7 8	0.6 0.55	0.85 0.75
IRFZ20	TO-220AB	50	15	0.08	0.10	* 2SK970 * 2SK971	60	10 15	0.12 0.055	0.15 0.065
IRFZ22	TO-220AB	50	14	0.11	0.12	* 2SK970 * 2SK971	60	10 15	0.12 0.055	0.15 0.065
IRFZ30	TO-220AB	50	30	0.045	0.05	* 2SK971 * 2SK972	60	15 25	0.055 0.033	0.065 0.04
IRFZ32	TO-220AB	50	25	0.065	0.07	* 2SK971 * 2SK972	60	15 25	0.055 0.033	0.065 0.04
IRFZ40	TO-220AB	50	51	0.024	0.028	* HS76099	60	27	0.02	0.025
IRFZ42	TO-220AB	50	46	0.030	0.035	* HS76099	60	27	0.02	0.025
IRFZ34	TO-220AB	60	30	0.04	0.05	* 2SK972	60	25	0.033	0.04
IRFZ35	TO-220AB	60	25	0.05	0.07	* 2SK971	60	15	0.055	0.065
IRFZ44	TO-220AB	60	35	0.021	0.028	* HS76099	60	27	0.02	0.025
IRFZ45	TO-220AB	60	35	0.028	0.035	* HS76099	60	27	0.02	0.025
* IRLZ14	TO-220AB	60	7.8		0.3					
* IRLZ24	TO-220AB	60	13		0.15	* 2SK970	60	10	0.12	0.15
* IRLZ34	TO-220AB	60	23		0.07	* 2SK971	60	15	0.055	0.065
* IRLZ44	TO-220AB	60	35		0.04	* 2SK972	60	25	0.033	0.04
* IRLZ530	TO-220AB	100	13		0.22					
* IRLZ540	TO-220AB	100	24		0.11	* HS76121	100	20	0.07	0.085
IRBC30	TO-220AB	600	3.6	1.9	2.2					
IRBC32	TO-220AB	600	2.7	2.2	2.7					
IRBC40	TO-220AB	600	6.2	0.97	1.2					
IRBC42	TO-220AB	600	5.4	1.2	1.6					
IRFPE40	TO-3P	800	5.3	1.5	2.0	2SK695	800	5	2.0	3.0
IRFPE42	TO-3P	800	4.8	2.0	2.4	2SK695	800	5	2.0	3.0

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; INTERNATIONAL RECTIFIER (IR) 5

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
IRFPF40	TO-3P	900	4.7	2.1	2.5	HS78141	900	6	2.0	3.0
IRFPF42	TO-3P	900	4.3	2.5	3.0	HS78141	900	6	2.0	3.0
IRFPG40	TO-3P	1000	4.3	3.2	3.5	2SK696	1000	3	3.0	4.0
IRFPG42	TO-3P	1000	3.9	3.5	4.2	2SK696	1000	3	3.0	4.0
IRFPE50	TO-3P	800	7.8	0.93	1.2	2SK684	800	7	1.0	1.5
IRFPE52	TO-3P	800	7.2	1.2	1.4	2SK684	800	7	1.0	1.5
IRFPF50	TO-3P	900	6.8	1.3	1.6	HS78143	900	8	1.2	1.6
IRFPF52	TO-3P	900	6.2	1.6	1.9	HS78143	900	8	1.2	1.6
IRFPG50	TO-3P	1000	6.1	1.7	2.0	2SK685 HS78151	1000	5	1.5	2.0
IRFPG52	TO-3P	1000	5.5	2.0	2.4	2SK685 HS78151	1000	5	1.5	2.0
IRFS1Z0	TO-3P	100	0.9	2.2	2.4					
IRFS1Z3	UPAK	60	0.75	2.8	3.2					
IRFR/U220	DPAK	200	4.6	0.47	0.8					
IRFR/U210	DPAK	200	2.7	0.91	1.5					
IRFR/U120	DPAK	100	8.4	0.25	0.27	* HS72027	100	3	0.3	0.45
IRFR/U110	DPAK	100	4.7	0.41	0.54	* HS72027	100	3	0.3	0.45
IRFR/U121	DPAK	80	8.4	0.25	0.27	* HS72027	100	3	0.3	0.45
IRFR/U111	DPAK	80	4.7	0.41	0.54	* HS72027	100	3	0.3	0.45
IRFR/U020	DPAK	50	15	0.08	0.1	* 2SK974S/L	60	3	0.15	0.18
IRFR/U010	DPAK	50	14	0.1	0.2	* 2SK974S/L	60	3	0.15	0.18

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; INTERNATIONAL RECTIFIER (IR) 6

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
IRF9520	TO-220AB	-100	-6	0.5	0.6					
IRF9521	TO-220AB	-60	-6	0.5	0.6					
IRF9522	TO-220AB	-100	-5	0.6	0.8					
IRF9523	TO-220AB	-60	-5	0.6	0.8					
IRF9530	TO-220AB	-100	-12	0.25	0.3	2SJ127	-120	-10	0.20	0.25
IRF9531	TO-220AB	-60	-12	0.25	0.3	2SJ102	-60	-5	0.3	0.4
IRF9532	TO-220AB	-100	-10	0.3	0.4	2SJ127	-120	-10	0.20	0.25
IRF9533	TO-220AB	-60	-10	0.3	0.4	2SJ102	-60	-5	0.3	0.4
IRF9540	TO-220AB	-100	-19	0.15	0.2	2SJ127	-120	-10	0.20	0.25
IRF9541	TO-220AB	-60	-19	0.15	0.2	2SJ122	-60	-10	0.15	0.20
IRF9542	TO-220AB	-100	-15	0.22	0.3	2SJ127	-120	-10	0.20	0.25
IRF9543	TO-220AB	-60	-15	0.22	0.3	2SJ122	-60	-10	0.15	0.20
IRF9630	TO-220AB	-200	-6.5	0.5	0.8					
IRF9631	TO-220AB	-150	-6.5	0.5	0.8					
IRF9632	TO-220AB	-200	-5.5	0.8	1.2					
IRF9633	TO-220AB	-150	-5.5	0.8	1.2					
IRF9640	TO-220AB	-200	-11	0.35	0.5					
IRF9641	TO-220AB	-150	-11	0.35	0.5					
IRF9642	TO-220AB	-200	-9	0.55	0.7					
IRF9643	TO-220AB	-150	-9	0.55	0.7					
IRF9Z20	TO-220AB	-50	-9.7	0.20	0.28	2SJ122	-60	-10	0.15	0.20
IRF9Z22	TO-220AB	-50	-8.9	0.28	0.33	2SJ122	-60	-10	0.15	0.20
IRFR/U9220	DPAK	-200	-3.5		1.5					
IRFR/U9210	DPAK	-200	-1.75		3.0	2SJ130S/L	-300	-1	6.0	8.5
IRFR/U9120	DPAK	-100	-6		0.8					
IRFR/U9110	DPAK	-100	-3.2		1.2					
IRFR/U9121	DPAK	-80	-6		0.8					
IRFR/U9111	DPAK	-80	-3.2		1.2					
IRFR/U9020	DPAK	-50	-9.9		0.28					
IRFR/U9010	DPAK	-50	-5.3		0.50					

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; Siliconix 1

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
IRF130	TO-3	100	14	0.15	0.18	2SK308	120	10	0.2	0.3
IRF131	TO-3	60	14	0.15	0.18					
IRF132	TO-3	100	12	0.20	0.25	2SK308	120	10	0.2	0.3
IRF133	TO-3	60	12	0.20	0.25					
IRF230	TO-3	200	9	0.25	0.4	2SK401	250	10	0.3	0.4
IRF231	TO-3	150	9	0.25	0.4					
IRF232	TO-3	200	8	0.4	0.6	2SK401	250	10	0.3	0.4
IRF233	TO-3	150	8	0.4	0.6					
IRF330	TO-3	400	5.5	0.8	1.0	2SK298	400	8	1.1	1.75
IRF331	TO-3	350	5.5	0.8	1.0	2SK298	400	8	1.1	1.75
IRF332	TO-3	400	4.5	1.3	1.5	2SK298	400	8	1.1	1.75
IRF333	TO-3	350	4.5	1.3	1.5	2SK298	400	8	1.1	1.75
IRF430	TO-3	500	4.5	1.3	1.5					
IRF431	TO-3	450	4.5	1.3	1.5	2SK299	450	8	1.1	1.75
IRF432	TO-3	500	4.0	1.5	2.0					
IRF433	TO-3	450	4.0	1.5	2.0	2SK299	450	8	1.1	1.75
IRF440	TO-3	500	8	0.8	0.85	2SK512	500	12	0.55	0.65
IRF441	TO-3	450	8	0.8	0.85	2SK313	450	12	0.67	0.90
IRF442	TO-3	500	7	1.0	1.1					
IRF443	TO-3	450	7	1.0	1.1	2SK313	450	12	0.67	0.90
IRF450	TO-3	500	13	0.3	0.4	2SK1064	500	15	0.3	0.4
IRF451	TO-3	450	13	0.3	0.4	2SK1063	450	15	0.25	0.36
IRF452	TO-3	500	12	0.4	0.5	2SK1064	500	15	0.3	0.4
IRF453	TO-3	450	12	0.4	0.5	2SK1063	450	15	0.25	0.36
IRF520	TO-220AB	100	8	0.25	0.3	2SK551	120	7	0.15	0.20
IRF521	TO-220AB	60	8	0.25	0.3	2SK346	60	5	0.3	0.4
IRF522	TO-220AB	100	7	0.3	0.4	2SK551	120	7	0.15	0.20
IRF523	TO-220AB	60	7	0.3	0.4	2SK346	60	5	0.3	0.4
IRF530	TO-220AB	100	14	0.15	0.18	2SK551	120	10	0.15	0.20
IRF531	TO-220AB	60	14	0.15	0.18	2SK549 * 2SK970	60	10	0.12	0.15

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; Siliconix 2

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
IRF540	TO-220AB	100	27	0.07	0.085	*HS76121	100	20	0.07	0.085
IRF541	TO-220AB	60	27	0.07	0.085	*2SK971	60	15	0.055	0.065
IRF542	TO-220AB	100	24	0.07	0.11	*HS76121	100	20	0.07	0.085
IRF543	TO-220AB	60	24	0.09	0.11	*2SK971	60	15	0.055	0.065
IRF630	TO-220AB	200	9	0.25	0.4	2SK741	250	7	0.40	0.55
IRF631	TO-220AB	150	9	0.25	0.4	2SK741	250	7	0.40	0.55
IRF632	TO-220AB	200	8	0.4	0.6	2SK741	250	7	0.40	0.55
IRF633	TO-220AB	150	8	0.4	0.6	2SK741	250	7	0.40	0.55
IRF640	TO-220AB	200	18	0.14	0.18					
IRF641	TO-220AB	150	18	0.14	0.18	2SK740	150	10	0.12	0.15
IRF642	TO-220AB	200	16	0.20	0.22					
IRF643	TO-220AB	150	16	0.20	0.22	2SK740	150	10	0.12	0.15
IRF820	TO-220AB	500	2.5	2.5	3.0	HS76079A	500	3	2.0	3.0
IRF821	TO-220AB	450	2.5	2.5	3.0	HS76079	450	3	1.8	2.8
IRF822	TO-220AB	500	2.0	3.0	4.0	HS76079A	500	3	2.0	3.0
IRF823	TO-220AB	450	2.0	3.0	4.0	HS76079	450	3	1.8	2.8
IRF830	TO-220AB	500	4.5	1.3	1.5	2SK553 HS76091A	500	5	1.2	1.5
IRF831	TO-220AB	450	4.5	1.3	1.5	2SK552 HS76091	450	5	1.0	1.4
IRF832	TO-220AB	500	4.0	1.5	2.0	2SK553 HS76091A	500	5	1.2	1.5
IRF833	TO-220AB	450	4.0	1.5	2.0	2SK552 HS76091	450	5	1.0	1.4
IRF840	TO-220AB	500	8	0.8	0.85	2SK555 HS76093A	500	7 8	0.7 0.6	1.0 0.85
IRF841	TO-220AB	450	8	0.8	0.85	2SK554 HS76093	450	7 8	0.6 0.55	0.85 0.75
IRF842	TO-220AB	500	7	1.0	1.1	2SK555 HS76093A	500	7 8	0.7 0.6	1.0 0.85
IRF843	TO-220AB	450	7	1.0	1.1	2SK554 HS76093	450	7 8	0.6 0.55	0.85 0.75
VN0600D	TO-220AB	60	18	0.08	0.12	2SK549 *2SK970	60	10	0.12	0.15
VN0400D	TO-220AB	40	18	0.08	0.12	2SK549 *2SK970	60	10	0.12	0.15
VN0601D	TO-220AB	60	16	0.10	0.15	2SK549 *2SK970	60	10	0.12	0.15
VN0401D	TO-220AB	40	16	0.10	0.15	2SK549 *2SK970	60	10	0.12	0.15
VN1200D	TO-220AB	120	15	0.16	0.18	2SK551	120	10	0.15	0.20
VN1000D	TO-220AB	100	15	0.16	0.18	2SK551	120	10	0.15	0.20

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; Siliconix 3

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
VN0800D	TO-220AB	80	15	0.16	0.18	2SK551	120	10	0.15	0.20
VN1201A	TO-3	120	13	0.16	0.25	2SK308	120	10	0.2	0.3
VN1001A	TO-3	100	13	0.16	0.25	2SK308	120	10	0.2	0.3
VN0801A	TO-3	80	13	0.16	0.25	2SK308	120	10	0.2	0.3
VN1201D	TO-220AB	120	12	0.22	0.25	2SK551	120	10	0.15	0.20
VN1001D	TO-220AB	100	12	0.22	0.25	2SK551	120	10	0.15	0.20
VN0801D	TO-220AB	80	12	0.22	0.25	2SK551	120	10	0.15	0.20
VN4000A	TO-3	400	6.8	0.8	1.0	2SK298	400	8	1.1	1.75
VN3500A	TO-3	350	6.8	0.8	1.0	2SK298	400	8	1.1	1.75
VN4001A	TO-3	400	5.6	1.2	1.5	2SK298	400	8	1.1	1.75
VN3501A	TO-3	350	5.6	1.2	1.5	2SK298	400	8	1.1	1.75
VN4501A	TO-3	450	5.2	1.2	1.5	2SK299	450	8	1.1	1.75
VN4502A	TO-3	450	4.5	1.6	2.0	2SK299	450	8	1.1	1.75
VN4501D	TO-220AB	450	4.9	1.2	1.5	2SK552 HS76091	450	5	1.0	1.4
VN4502D	TO-220AB	450	4.2	1.6	2.0	2SK552 HS76091	450	5	1.0	1.4
VN5001D	TO-220AB	500	4.9	1.2	1.5	2SK553 HS76091A	500	5	1.2	1.5
VN5002D	TO-220AB	500	4.2	1.6	2.0	2SK553 HS76091A	500	5	1.2	1.5
VNE010D	TO-220AB	100	5	0.4	0.5	2SK295	100	5	0.4	0.56
VND010D	TO-220AB	80	5	0.4	0.5	2SK294	80	5	0.4	0.56
VNC010D	TO-220AB	60	5	0.4	0.5	2SK346	60	5	0.3	0.4
VNE011D	TO-220AB	100	5	0.4	0.5	2SK295	100	5	0.4	0.56
VND011D	TO-220AB	80	5	0.4	0.5	2SK294	80	5	0.4	0.56
VNC011D	TO-220AB	60	5	0.4	0.5	2SK346	60	5	0.3	0.4
VNP011A	TO-3	500	6.5	1.2	1.5					
VNN002A	TO-3	450	6.5	1.2	1.5	2SK299	450	8	1.1	1.75
VNS008D	TO-220AB	600	5.8	1.2	1.5					
VNS009D	TO-220AB	600	5.8	1.7	2.0					
2N6761	TO-3	450	4	1.5	2.0	2SK299	450	8	1.1	1.75
2N6762	TO-3	500	4.5	1.3	1.5					
2N6767	TO-3	350	12	0.3	0.4	2SK1063	450	15	0.26	0.36

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; Siliconix 4

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
2N6768	TO-3	400	14	0.25	0.3	2SK1063	450	15	0.25	0.36
2N6769	TO-3	450	11	0.4	0.5	2SK1063	450	15	0.25	0.36
2N6770	TO-3	500	12	0.3	0.4	2SK1064	500	15	0.3	0.4
BUP63	TO-3	400	5.6	1.2	1.5	2SK298	400	8	1.1	1.75
BUP61	TO-3	350	5.6	1.2	1.5	2SK298	400	8	1.1	1.75
BUP64	TO-3	450	5.2	1.2	1.5	2SK299	450	8	1.1	1.75
BUP65	TO-3	450	4.5	1.6	2.0	2SK299	450	8	1.1	1.75
BUZ10	TO-220AB	50	19		0.10	2SK549 * 2SK970	60	10	0.12	0.15
BUZ20	TO-220AB	100	14		0.20	2SK551	120	10	0.15	0.20
BUZ32	TO-220AB	200	9.5	0.35	0.4	2SK741	250	7	0.40	0.55
BUZ35	TO-3	200	9.9	0.35	0.4	2SK401	250	10	0.3	0.4
BUZ42	TO-220AB	500	4	1.8	2.0	2SK553 HS76091A	500	5	1.2	1.5
BUZ45	TO-3	500	10		0.6	2SK512	500	12	0.55	0.65
BUZ60	TO-220AB	400	5.5	0.8	1.0	2SK554 HS76115	450	7	0.6	0.85
BUZ64	TO-3	400	10.5		0.4	2SK1063	450	15	0.25	0.36
BUZ71	TO-220AB	50	12		0.1	* 2SK970	60	10	0.12	0.15
BUZ72A	TO-220AB	100	9	0.18	0.25	2SK551	120	10	0.15	0.20
BUZ74	TO-220AB	500	2.4	2.6	3.0	HS76079A	500	3	2.0	3.0
BUZ76	TO-220AB	400	3		1.8	2SK552 HS76091	450	5	1.0	1.4
SMP60N05	TO-220AB	50	60		0.023	* HS76099	60	27	0.02	0.025
SMP50N05	TO-220AB	50	50		0.028	* HS76099	60	27	0.02	0.025

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; MOTOROLA 1

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
MTH25N08	(TO-3P)	80	25	0.065	0.075					
MTH25N10	(TO-3P)	100	25	0.065	0.075					
MTH35N05	(TO-3P)	50	35	0.047	0.055					
MTH35N06	(TO-3P)	60	35	0.047	0.055					
MTP1N95	TO-220AB	950	1	6	10	2SK1199	900	2	5.0	7.0
MTP1N100	TO-220AB	1000	1	6	10					
MTP2N45	TO-220AB	450	2	3.5	4.0	HS76079	450	3	1.8	2.8
MTP2N50	TO-220AB	500	2	3.5	4.0	HS76079A	500	3	2.0	3.0
MTP2N85	TO-220AB	850	2	5.0	8.0	2SK513 2SK1199	800 900	3 2	5.0	6 7.0
MTP2N90	TO-220AB	900	2	5.0	8.0	2SK1199	900	3	5.0	7.0
MTP2P45	TO-220AB	-450	-2	4.0	6.0	2SJ117	-400	-2	5.0	7.0
MTP2P45	TO-220AB	-500	-2	4.0	6.0					
MTP3N35	TO-220AB	350	3	2.3	3.3	HS76079	450	3	1.8	2.8
MTP3N40	TO-220AB	400	3	2.3	3.3	HS76079	450	3	1.8	2.8
MTP3N55	TO-220AB	550	3	1.7	2.5					
MTP3N60	TO-220AB	600	3	1.7	2.5					
MTP3N75	TO-220AB	750	3	5.5	7.0	2SK513 HS76125	800	3	5.0 4.5	6.0
MTP3N80	TO-220AB	800	3	5.5	7.0	2SK513 HS76125	800	3	5.0 4.5	6.0
MTM4N45	TO-3	450	4	1.3	1.5	2SK299	450	8	1.1	1.75
MTM4N50	TO-3	500	4	1.3	1.5					
MTM5N35	TO-3	350	5	0.8	1.0	2SK298	450	8	1.1	1.75
MTM5N40	TO-3	400	5	0.8	1.0	2SK298	450	8	1.1	1.75
MTP4N45	TO-220AB	450	4	1.3	1.5	2SK552 HS76091	450	5	1.0	1.4
MTP4N50	TO-220AB	500	4	1.3	1.5	2SK553 HS76091A	500	5	1.2	1.5
MTP5N35	TO-220AB	350	5	0.8	1.0	2SK552 HS76091	450	5	1.0	1.4
MTP5N40	TO-220AB	400	5	0.8	1.0	2SK552 HS76091	450	5	1.0	1.4
MTP5N18	TO-220AB	180	5	0.75	1.0	2SK741	250	7	0.40	0.55
MTP5N20	TO-220AB	200	5	0.75	1.0	2SK741	250	7	0.40	0.55
MTP7N12	TO-220AB	120	7	0.45	0.7	2SK295	100	5	0.40	0.56
MTP7N15	TO-220AB	150	7	0.45	0.7					

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; MOTOROLA 2

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
MTH6N55	(TO-3P)	550	6	0.9	1.2					
MTH6N60	(TO-3P)	600	6	0.9	1.2					
MTP7N18	TO-220AB	180	7	0.5	0.7	2SK741	250	7	0.40	0.55
MTP7N20	TO-220AB	200	7	0.5	0.7	2SK741	250	7	0.40	0.55
MTP8N12	TO-220AB	120	8	0.43	0.5					
MTP8N15	TO-220AB	150	8	0.43	0.5					
MTM7N45	TO-3	450	7	0.65	0.8	2SK313	450	12	0.67	0.90
MTM7N50	TO-3	500	7	0.65	0.8					
MTM8N35	TO-3	350	8	0.45	0.55	2SK312	400	12	0.67	0.90
MTM8N40	TO-3	400	8	0.45	0.55	2SK312	400	12	0.67	0.90
MTH7N45	(TO-3P)	450	7	0.65	0.8	2SK641 HS78131	450	10	0.6	0.80
MTH7N50	(TO-3P)	500	7	0.65	0.8	2SK642 HS78097A	500	10 11	0.7 0.6	1.0 0.85
MTH8N35	(TO-3P)	350	8	0.45	0.55	HS78097	450	11	0.55	0.75
MTH8N40	(TO-3P)	400	8	0.45	0.55	HS78097	450	11	0.55	0.75
MTM8N08	TO-3	80	8	0.31	0.50	2SK308	120	10	0.2	0.3
MTM8N10	TO-3	100	8	0.31	0.50	2SK308	120	10	0.2	0.3
MTM10N05	TO-3	50	10	0.20	0.28	2SK308	120	10	0.2	0.3
MTM10N06	TO-3	60	10	0.20	0.28	2SK308	120	10	0.2	0.3
MTP8N08	TO-220AB	80	8	0.31	0.50	2SK294	80	5	0.40	0.56
MTP8N10	TO-220AB	100	8	0.31	0.50	2SK295	100	5	0.40	0.56
MTP10N05	TO-220AB	50	10	0.20	0.28	2SK346 * 2SK970	60	5 10	0.30 0.12	0.40 0.15
MTP10N06	TO-220AB	60	10	0.20	0.28	2SK346 * 2SK970	60	5 10	0.30 0.12	0.40 0.15
MTP8N18	TO-220AB	180	8	0.32	0.4	2SK741	250	7	0.40	0.55
MTP8N20	TO-220AB	200	8	0.32	0.4	2SK741	250	7	0.40	0.55
MTP8P08	TO-220AB	-80	-8	0.25	0.4					
MTP8P10	TO-220AB	-100	-8	0.25	0.4					
MTP10N08	TO-220AB	80	10	0.27	0.33	2SK551	120	10	0.15	0.20
MTP10N10	TO-220AB	100	10	0.27	0.33	2SK551	120	10	0.15	0.20
MTP10N12	TO-220AB	120	10	0.20	0.30	2SK551	120	10	0.15	0.20
MTP10N15	TO-220AB	150	10	0.20	0.30	2SK740	150	10	0.12	0.15

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; MOTOROLA 3

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
MTM10N25	TO-3	250	10	0.35	0.45	2SK401	250	10	0.3	0.4
MTP10N25	TO-220AB	250	10	0.35	0.45	2SK741	250	7	0.40	0.55
MTP12N05	TO-220AB	50	12	0.15	0.20	2SK549 * 2SK970	60	10	0.12	0.15
MTP12N06	TO-220AB	60	12	0.15	0.20	2SK549 * 2SK970	60	10	0.12	0.15
MTP12N08	TO-220AB	80	12	0.13	0.18	2SK551	120	10	0.15	0.20
MTP12N10	TO-220AB	100	12	0.13	0.18	2SK551	120	10	0.15	0.20
MTP15N05	TO-220AB	50	15	0.10	0.16	2SK549 * 2SK970	60	10	0.12	0.15
MTP15N06	TO-220AB	60	15	0.10	0.16	2SK549 * 2SK970	60	10	0.12	0.15
MTP12N18	TO-220AB	180	12	0.25	0.35	2SK741	250	7	0.40	0.55
MTP12N20	TO-220AB	200	12	0.25	0.35	2SK741	250	7	0.40	0.55
MTP15N12	TO-220AB	120	15	0.16	0.25	2SK740	150	10	0.12	0.15
MTP15N15	TO-220AB	150	15	0.16	0.25	2SK740	150	10	0.12	0.15
MTM15N35	TO-3	350	15	0.26	0.30	2SK1063	450	15	0.25	0.36
MTM15N40	TO-3	400	15	0.26	0.30	2SK1063	450	15	0.25	0.36
MTM15N45	TO-3	450	15	0.3	0.4	2SK1063	450	15	0.25	0.36
MTM15N50	TO-3	500	15	0.3	0.4	2SK1064	500	15	0.3	0.4
MTP20N08	TO-220AB	80	20	0.10	0.15	2SK551	120	10	0.15	0.20
MTP20N10	TO-220AB	100	20	0.10	0.15	2SK551	120	10	0.15	0.20
MTP25N05	TO-220AB	50	25	0.065	0.08	* 2SK971	60	15	0.055	0.065
MTP25N06	TO-220AB	60	25	0.065	0.08	* 2SK971	60	15	0.055	0.065
2N6759	TO-3	350	4.5	1.3	1.5	2SK298	400	8	1.1	1.75
2N6760	TO-3	400	5.5	0.8	1.0	2SK298	400	8	1.1	1.75
2N6761	TO-3	450	4.0	1.5	2.0	2SK299	450	8	1.1	1.75
2N6762	TO-3	500	4.5	0.8	1.5					
IRF520	TO-220AB	100	8	0.25	0.3	2SK551	120	10	0.15	0.20
IRF521	TO-220AB	60	8	0.25	0.3	2SK346 * 2SK970	60	5 10	0.30 0.12	0.40 0.15
IRF522	TO-220AB	100	7	0.3	0.4	2SK551	120	10	0.15	0.20
IRF523	TO-220AB	60	7	0.3	0.4	2SK346	60	5	0.3	0.4
IRF540	TO-220AB	100	27	0.07	0.085	* HS76121	100	20	0.07	0.085
IRF541	TO-220AB	60	27	0.00	0.085	* 2SK971	60	15	0.055	0.065

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; MOTOROLA 4

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
IRF542	TO-220AB	100	24	0.09	0.11	* HS76121	100	20	0.07	0.085
IRF543	TO-220AB	60	24	0.09	0.11	* 2SK971	60	15	0.055	0.065
IRF630	TO-220AB	200	9	0.25	0.40	2SK741	250	7	0.40	0.55
IRF631	TO-220AB	150	9	0.25	0.40	2SK741	250	7	0.40	0.55
IRF632	TO-220AB	200	8	0.40	0.60	2SK741	250	7	0.40	0.55
IRF633	TO-220AB	150	8	0.40	0.60	2SK741	250	7	0.40	0.55
IRF640	TO-220AB	200	18	0.14	0.18					
IRF641	TO-220AB	150	18	0.14	0.18	2SK740	150	10	0.12	0.15
IRF642	TO-220AB	200	16	0.20	0.22					
IRF643	TO-220AB	150	16	0.20	0.22	2SK740	150	10	0.12	0.15
IRF450	TO-3	500	13	0.3	0.4	2SK1064	500	15	0.30	0.40
IRF451	TO-3	450	13	0.3	0.4	2SK1063	450	15	0.25	0.36
MTP2N55	TO-220AB	550	2							
MTP2N60	TO-220AB	600	2							
MTH10N45	(TO-3P)	450	10			2SK641 HS78097	450	10 11	0.60 0.55	0.80 0.75
MTH10N50	(TO-3P)	500	10			2SK642 HS78097A	500	10 11	0.70 0.60	1.0 0.85
MTH5N100	(TO-3P)	1000	5		3.0	2SK696	1000	3	3.0	4.0
MTH5N95	(TO-3P)	950	5		3.0	2SK696	1000	3	3.0	4.0
MTH6N90	(TO-3P)	900	6		3.0	2SK695 HS78141	800 900	5 6	2.0	3.0
MTH6N85	(TO-3P)	850	6		3.0	2SK695 HS78141	800 900	5 6	2.0	3.0
MTH8N60	(TO-3P)	600	8		0.5					
MTH8N55	(TO-3P)	550	8		0.5					
MTH13N50	(TO-3P)	500	13	0.3	0.4	2SK560 HS78101A	500	15	0.3	0.40
MTH13N45	(TO-3P)	450	13	0.3	0.4	2SK559 HS78101	450	15	0.25	0.36
MTH15N20	(TO-3P)	200	15		0.16	2SK623	250	20	0.12	0.15
MTH30N20	(TO-3P)	200	30		0.08					
MTH15N18	(TO-3P)	180	15		0.16	2SK623	250	20	0.12	0.15
MTH30N18	(TO-3P)	180	30		0.08					
MTH20N15	(TO-3P)	150	20		0.12	HS78157	150	15	0.12	0.15
MTH35N15	(TO-3P)	150	35		0.06	2SK622	150	20	0.06	0.075

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; MOTOROLA 5

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
MTH20N12	(TO-3P)	120	20		0.12	HS78157	150	15	0.12	0.15
MTH35N12	(TO-3P)	120	35		0.06	2SK622	150	20	0.06	0.075
MTH40N10	(TO-3P)	100	40		0.04	* HS78145	100	40	0.025	0.03
MTH40N08	(TO-3P)	80	40		0.04	* HS78145	100	40	0.025	0.03
MTH40N06	(TO-3P)	60	40		0.028	* HS78125	60	40	0.014	0.018
MTH40N05	(TO-3P)	50	40		0.028	* HS78125	60	40	0.014	0.018
MTP8N50	TO-220AB	500	8	0.65	0.8	2SK555	500	7	0.70	1.0
						HS76093A		8	0.60	0.85
MTP8N45	TO-220AB	450	8	0.65	0.8	2SK554	450	7	0.60	0.85
						HS76093		8	0.55	0.75
MTP25N10	TO-220AB	100	25	0.07	0.085	* HS76121	100	20	0.07	0.085
MTP25N08	TO-220AB	80	25	0.07	0.085	* HS76121	100	20	0.07	0.085
MTP3055A	TO-220AB	60	12	0.10	0.15	* 2SK970	60	10	0.12	0.15
MTP3055E	TO-220AB	60	12	0.10	0.15	* 2SK970	60	10	0.12	0.15
MTP14N05A	TO-220AB	50	14	0.08	0.10	* 2SK970	60	10	0.12	0.15
MTP16N05A	TO-220AB	50	16		0.08	* 2SK971	60	15	0.055	0.065
BUZ11A	TO-220AB	50	25		0.06	* 2SK971	60	15	0.055	0.065
BUZ11	TO-220AB	50	30	0.03	0.04	* 2SK972	60	25	0.033	0.04
MTD4N20	DPAK	200	4		0.7					
MTD4N18	DPAK	180	4		0.7	2SK430	150	3	0.8	1.0
MTD6N15	DPAK	150	6		0.3					
MTD6N12	DPAK	120	6		0.3	* HS72027	100	3	0.3	0.45
MTD4P06	DPAK	-60	-4		0.6					
MTD5N06	DPAK	60	5		0.4	* 2SK973	60	2	0.25	0.35
MTD8N06	DPAK	60	8		0.15	* 2SK974	60	3	0.15	0.18
MTD4P05	DPAK	-50	-4		0.6					
MTD5N05	DPAK	50	5		0.4	* 2SK973	60	2	0.25	0.35
MTD10N05A	DPAK	50	10		0.1	* 2SK974	60	3	0.15	0.18
MTP8P10	TO-220AB	-100	-8		0.4	2SJ127	-120	-10	0.20	0.25
MTP12P10	TO-220AB	-100	-12		0.3	2SJ127	-120	-10	0.20	0.25
MTP8P08	TO-220AB	-80	-8		0.4	2SJ127	-120	-10	0.20	0.25
MTP12P08	TO-220AB	-80	-12		0.3	2SJ127	-120	-10	0.20	0.25

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; MOTOROLA 6

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
MTP7P06	TO-220AB	-60	-7		0.6	2SJ102	-60	-5	0.3	0.4
MTP12P06	TO-220AB	-60	-12		0.3	2SJ102	-60	-5	0.3	0.4
MTP20P06	TO-220AB	-60	-20		0.2	2SJ122	-60	-10	0.15	0.20
MTP7P05	TO-220AB	-50	-7		0.6	2SJ102	-60	-5	0.3	0.4
MTP12P05	TO-220AB	-50	-12		0.3	2SJ102	-60	-5	0.3	0.4
MTP8P20	(TO-3P)	-200	-7		0.7	2SJ114	-200	-8	0.6	0.8
MTP8P18	(TO-3P)	-180	-7		0.7	2SJ114	-200	-8	0.6	0.8
MTP20P10	(TO-3P)	-100	-20		0.15					
MTP20P08	(TO-3P)	-80	-20		0.15					
MTP25P06	(TO-3P)	-60	-25		0.14					
MTP25P05	(TO-3P)	-50	-25		0.14					

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER: SIEMENS 1

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS}(on)$ (Ω) typ.	$R_{DS}(on)$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS}(on)$ (Ω) typ.	$R_{DS}(on)$ (Ω) max.
BUZ10	TO-220AB	50	12	0.085	0.1	2SK549 * 2SK970	60	10	0.12	0.15
BUZ10A	TO-220AB	50	12	0.11	0.12	2SK549 * 2SK970	60	10	0.12	0.15
BUZ11	TO-220AB	50	30	0.035	0.04	* 2SK972	60	25	0.033	0.04
BUZ11A	TO-220AB	50	25	0.05	0.06	* 2SK971	60	15	0.055	0.065
BUZ14	TO-3	50	39	0.035	0.04					
BUZ15	TO-3	50	45	0.025	0.03					
BUZ20	TO-220AB	100	12	0.15	0.20	2SK551	120	10	0.15	0.20
BUZ21	TO-220AB	100	19	0.09	0.10	* HS76121	100	20	0.07	0.085
BUZ23	TO-3	100	10	0.15	0.20	2SK308	100	10	0.2	0.3
BUZ24	TO-3	100	32	0.055	0.06					
BUZ25	TO-3	100	19	0.09	0.10					
BUZ30	TO-220AB	200	7	0.45	0.75	2SK741	250	7	0.40	0.55
BUZ31	TO-220AB	200	12.5	0.17	0.20					
BUZ32	TO-220AB	200	9.5	0.35	0.40	2SK741	250	7	0.40	0.55
BUZ33	TO-3	200	7.2	0.5	0.75					
BUZ34	TO-3	200	14	0.17	0.20					
BUZ35	TO-3	200	9.9	0.35	0.40	2SK401	250	10	0.3	0.4
BUZ36	TO-3	200	22	0.09	0.12					
BUZ40	TO-220AB	500	2.5	3.5	4.5	HS76079A	500	3	2.0	3.0
BUZ41A	TO-220AB	500	4.5	1.4	1.5	2SK553 HS76091A	500	5	1.2	1.5
BUZ42	TO-220AB	500	4.0	1.6	2.0	2SK553 HS76091A	500	5	1.2	1.5
BUZ43	TO-3	500	2.8	3.0	4.5					
BUZ44A	TO-3	500	4.8	1.4	1.5	2SK299	450	8	1.1	1.75
BUZ45	TO-3	500	9.6	0.55	0.60	2SK512	500	12	0.55	0.65
BUZ45A	TO-3	500	8.3	0.7	0.8	2SK313	450	12	0.67	0.90
BUZ45B	TO-3	500	10	0.48	0.5	2SK512	500	12	0.55	0.65
BUZ46	TO-3	500	4.2	1.8	2.0	2SK299	450	8	1.1	1.75
BUZ50A	TO-220AB	1000	2.5	4.5	5.0	2SK1199	900	2	4.5	7.0
BUZ50B	TO-220AB	1000	2	6.5	8.0	2SK1199	900	2	4.5	7.0
BUZ53A	TO-3	1000	2.6	4.5	5.0					

* 4 V Gate Drive Device

POWER MOSFET Cross Reference List

MAKER; SIEMENS 2

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
BUZ54	TO-3	1000	5.3	1.7	2.0					
BUZ54A	TO-3	1000	4.6	2.2	2.6					
BUZ60	TO-220AB	400	5.5	0.9	1.0	2SK554 HS76115	450	7	0.60	0.85
BUZ60B	TO-220AB	400	4.5	1.2	1.5	2SK552 HS76091	450	5	1.0	1.4
BUZ63	TO-3	400	5.9	0.9	1.0	2SK312	400	12	0.67	0.90
BUZ63B	TO-3	400	4.5	1.2	1.5	2SK298	400	8	1.1	1.75
BUZ64	TO-3	400	10.5	0.35	0.4	2SK1063	450	15	0.25	0.36
BUZ71	TO-220AB	50	12	0.09	0.1	* 2SK970	60	10	0.12	0.15
BUZ71A	TO-220AB	50	12	0.10	0.12	* 2SK970	60	10	0.12	0.15
BUZ72A	TO-220AB	100	9	0.20	0.25	2SK551	120	10	0.15	0.20
BUZ73A	TO-220AB	200	5.8	0.45	0.60	2SK741	250	7	0.40	0.55
BUZ74	TO-220AB	500	2.4	2.6	3.0	HS76079A	500	3	2.0	3.0
BUZ74A	TO-220AB	500	2.0	3.6	4.0	HS76079A	500	3	3.0	4.0
BUZ76	TO-220AB	400	3.0	1.6	1.8	2SK552 HS76091	450	5	1.0	1.4
BUZ76A	TO-220AB	400	2.6	2.2	2.5	HS76079	450	3	1.8	2.8
BUZ80	TO-220AB	800	2.6	3.5	4.0	2SK513 HS76125	800	3	5.0 4.5	6.0
BUZ80A	TO-220AB	800	3.0	2.7	3.0					
BUZ83	TO-3	800	2.9	3.5	4.0					
BUZ83A	TO-3	800	3.4	2.7	3.0	2SK351	800	5	1.7	3.0
BUZ84	TO-3	800	5.3	1.6	2.0	2SK351	800	5	1.7	3.0
BUZ84A	TO-3	800	6.0	1.3	1.5					
BUZ11S2	TO-220AB	60	30		0.04	* 2SK972	60	25	0.033	0.04
BUZ205 注1)	TO-220AB	400	6		1.0					
BUZ206 注1)	TO-220AB	400	5		1.5					
BUZ215 注1)	TO-220AB	500	5		1.5					
BUZ216 注1)	TO-220AB	500	4.4		2.0					
BUZ90	TO-220AB	600	4.0		2.0					
BUZ90A	TO-220AB	600	3.5		2.5					
BUZ78	TO-220AB	800	1.5		8.0	2SK513 HS76125	800	3	5.0 4.5	6.0
BUZ347	TO-3P	50	42	0.025	0.03					

* 4 V Gate Drive Device Note1) Fast Recovery Diode Type(FRED－FET)

POWER MOSFET Cross Reference List

MAKER; SIEMENS 3

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
BUZ348	TO-3P	50	39	0.03	0.04					
BUZ349	TO-3P	100	32	0.055	0.06	*HS78147	100	30	0.05	0.06
BUZ350	TO-3P	200	22	0.09	0.12	2SK622 2SK623	150 250	20	0.06 0.12	0.075 0.15
BUZ326	TO-3P	400	9.5		0.5	2SK556 HS78099	450	12	0.40	0.55
BUZ351	TO-3P	400	11.5	0.35	0.4	2SK559 HS78101	450	15	0.26	0.36
BUZ382 注1)	TO-3P	400	12.5	0.35	0.4	2SK682	450	12	0.40	0.55
BUZ383 注1)	TO-3P	400	11.5		0.5	2SK682	450	12	0.40	0.55
BUZ330	TO-3P	500	9.5		0.6	2SK557 HS78099A	500	12	0.45	0.60
BUZ331	TO-3P	500	8.0		0.8	2SK642 HS78097A	500	10 11	0.70 0.60	1.0 0.85
BUZ384 注1)	TO-3P	500	10.5		0.6	2SK683	500	12	0.45	0.60
BUZ385 注1)	TO-3P	500	9.0		0.8	2SK683	500	12	0.45	0.60
BUZ307	TO-3P	800	3.0	2.7	3.0	2SK695	800	5	2.0	3.0
BUZ308	TO-3P	800	2.6	3.5	4.0	2SK534 HS78139	800 900	5	3.0	4.0
BUZ355	TO-3P	800	6.0	1.3	1.5	2SK684	800	7	1.0	1.5
BUZ356	TO-3P	800	5.0	1.6	2.0	2SK695	800	5	2.0	3.0
BUZ310	TO-3P	1000	2.5	4.5	5.0	2SK696	1000	3	3.0	4.0
BUZ311	TO-3P	1000	2.3		6.0	2SK696	1000	3	3.0	4.0
BUZ357	TO-3P	1000	5.0	1.7	2.0	2SK685	1000	5	1.5	2.0
BUZ358	TO-3P	1000	4.5	2.2	2.6	2SK685	1000	5	1.5	2.0
BUZ201 注1)	TO-3	400	12.5		0.4					
BUZ202 注1)	TO-3	400	11.5		0.5					
BUZ210 注1)	TO-3	500	10.5		0.6					
BUZ211 注1)	TO-3	500	9.0		0.8					
BUZ171	TO-220AB	-50	-7.0		0.4	2SJ102	-60	5	0.3	0.4

* 4 V Gate Drive Device Note1) Fast Recovery Diode Type(FRED-FET)

POWER MOSFET Cross Reference List

MAKER; RCA 1

Industry Part No.	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	HITACHI Equivalent	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.
RFP3N45	TO-220AB	450	3	2.0	3.0	HS76079	450	3	1.8	2.8
RFP3N50	TO-220AB	500	3	2.0	3.0	HS76079A	500	3	2.0	3.0
RFP8N18	TO-220AB	180	8	0.36	0.5	2SK741	250	7	0.40	0.55
RFP8N20	TO-220AB	200	8	0.36	0.5	2SK741	250	7	0.40	0.55
RFK10N45	TO-3	450	10	0.40	0.85	2SK313	450	12	0.67	0.90
RFK10N50	TO-3	500	10	0.40	0.85	2SK512	500	12	0.55	0.65
RFM10N12	TO-3	120	10	0.25	0.3	2SK308	120	10	0.2	0.3
RFM10N15	TO-3	150	10	0.25	0.3	2SK308	120	10	0.2	0.3
RFP10N12	TO-220AB	120	10	0.25	0.3	2SK551	120	10	0.15	0.20
RFP10N15	TO-220AB	150	10	0.25	0.3	2SK551	120	10	0.15	0.20
RFP12N08	TO-220AB	80	12	0.16	0.2	2SK551	120	10	0.15	0.20
RFP12N10	TO-220AB	100	12	0.16	0.2	2SK551	120	10	0.15	0.20
RFP12P08	TO-220AB	-80	-12	0.16	0.3	2SJ127	-120	-10	0.20	0.25
RFP12P10	TO-220AB	-100	-12	0.16	0.3	2SJ127	-120	-10	0.20	0.25
RFP12N18	TO-220AB	180	12	0.13	0.25					
RFP12N20	TO-220AB	200	12	0.13	0.25					
RFP15N05	TO-220AB	50	15	0.09	0.15	* 2SK970	60	10	0.12	0.15
RFP15N06	TO-220AB	60	15	0.09	0.15	* 2SK970	60	10	0.12	0.15
RFP15N12	TO-220AB	120	15	0.12	0.15	2SK740	150	10	0.12	0.15
RFP15N15	TO-220AB	150	15	0.12	0.15	2SK740	150	10	0.12	0.15
RFP18N08	TO-220AB	80	18	0.07	0.12	* HS76121	100	20	0.07	0.085
RFP18N10	TO-220AB	100	18	0.07	0.12	* HS76121	100	20	0.07	0.085
* RFP15N05L	TO-220AB	50	15	0.09	0.15	* 2SK970	60	10	0.12	0.15
* RFP15N06L	TO-220AB	60	15	0.09	0.15	* 2SK970	60	10	0.12	0.15

* 4 V Gate Drive Device

POWER MOS FET Cross Reference List

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